CURRICULUM VITAE

Zhao Zhang

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RESEARCH INTERESTS

Computer architecture and parallel and distributed systems, with specialties in memory system design, memory system reliability, multi-core cache management, architectural support for computer security, energy-efficiency in parallel computing, and security and privacy in peer-to-peer and grid/cloud computing.

EDUCATION

Ph.D. in Computer Science, College of William and Mary, July 2002.
Thesis Topic: Memory latency reduction and access scheduling for ILP processors.
Advisor: Xiaodong Zhang

M.S. in Computer Science, Huazhong University of Science and Technology, May 1994.
Advisor: Zhengding Lu

B.S. in Computer Science, Huazhong University of Science and Technology, May 1991.

PROFESSIONAL EXPERIENCE

Associate Professor, August 2009 – present, Iowa State University.

Assistant Professor, August 2002 – August 2009, Iowa State University.

Research Intern, Summer 2000, Hewlett-Packard Laboratories, Palo Alto, CA.

Research Assistant, Department of Computer Science, College of William and Mary, 1997–2002.

AWARDS AND HONORS

Best paper award, "Reflections on Implementing and Teaching an Advanced Undergraduate Course in Embedded Systems." International Conference on Microelectronic Systems Education, 2007.

Top Ten Final List (World-Wide), IEEE Computer Society International Design Competition (CSIDC), Team Co-mentor, 2005.

STUDENTS

Yanan Cao, PhD student, 2011–present.

Qilin Li, MS student, 2013–2014.

Long Chen, PhD 2014, "Energy-efficient and cost-effective reliability design in memory systems" (with Research Excellence Award). First position: Senior Computer Architecture Engineer, Nvidia.

Vaibhav Sundriyal, PhD 2013, "Automatic Energy Schemes for High Performance Applications." First position: Postdoctoral at DoE Ames Laboratory. (Co-advised with Masha Sosonkina of Ames Lab and Old Dominion University).

Sparsh Mittal, PhD 2013, "Dynamic cache reconfiguration based techniques for improving cache energy efficiency." First Position: Postdoctoral at DoE Oak Ridge National Laboratory.

Peter Scott, MS, 2011.

Yong-Joon Park, PhD 2010. First Position: Research Staff at Intel Portland, OR.

Lakshminarasimhan Seshagiri, MS, 2009.

Jeffrey Schmidt, MS, 2009.

Jiang Lin, PhD 2008, "Thermal modeling and management of DRAM memory systems" (with Research Excellence Award). First position: Postdoctoral at IBM Austin Research Laboratory.

Souvik Ray, PhD 2008, "Design and analysis of privacy preserving mechanisms for emerging distributed applications." First position: Ask.com.

Meng-Shiou Wu, PhD 2005, "ATCOM: Automatically tuned collective communication system for SMP clusters." First position: Postdoctoral at DoE Ames Laboratory. (Co-advised with Ricky A. Kendall of Ames Lab).

REFEREED PUBLICATIONS

Refereed Journal Magazine Publications

[1] Heng He, Ruixuan Li, Xinhua Dong, and Zhao Zhang. "Secure, Efficient and Fine-grained Data Access Control Mechanism for P2P Storage Cloud." In *IEEE Transactions on Cloud Computing*, vol. 2, no. 4, pp. 471–484, Dec. 2014.

[2] Sparsh Mittal and Zhao Zhang. "EnCache: A Dynamic Profiling-Based Reconfiguration Technique for Improving Cache Energy Efficiency." *Journal of Circuits, Systems and Computers*, vol. 23, no. 10, Dec. 2014.

[3] Sparsh Mittal, Yanan Cao, and Zhao Zhang. "MASTER: A Multicore Cache Energy Saving Technique Using Dynamic Cache Reconfiguration." *IEEE Transactions on VLSI* (TVLSI), vol. 22, no. 8, Aug. 2014, pp. 1653–1665.

[4] Kun Fang, Hongzhong Zheng, Jiang Lin, Zhao Zhang, and Zhichun Zhu. "Mini-Rank: A Power-Efficient DDRx DRAM Memory Architecture." *IEEE Transactions on Computers*, vol. 63, no. 6, pp. 1500–1512, June 2014.

[5] Songqing Chen, Lei Liu, Xinyuan Wang, Xinwen Zhang, and Zhao Zhang. "A Host-based Approach for Unknown Fast Spreading Worm Detection and Containment." *ACM Transactions on Autonomous and Adaptive Systems*, vol. 8, no. 4, article no. 21, Jan. 2014.

[6] Long Chen, Yanan Cao, and Zhao Zhang. "E^{3}CC: A Memory Error Protection Scheme with Novel Address Mapping for Sub-Ranked and Low-Power Memories." *ACM Transactions on Architecture and Code Optimization* (TACO), vol. 10, issue 4, article no. 32, pp. 32:1–32:22, Dec. 2013.

[7] Jiang Lin, Hongzhong Zheng, Zhichun Zhu, and Zhao Zhang. "Thermal Modeling and Management of DRAM Systems." *IEEE Transactions on Computers*, vol. 62, no. 10, pp. 2069–2082, Oct. 2013.

[8] Vaibhav Sundriyal, Alexander Gaenko, Masha Sosonkina, and Zhao Zhang. "Energy Saving Strategies for Parallel Applications with Point-to-Point Communication Phases." *Journal of Parallel and Distributed Computing*, vol. 73, issue 8, pp. 1157–1169, August 2013.

[9] Vaibhav Sundriyal, Masha Sosonkina, and Zhao Zhang. "Achieving Energy Efficiency During Collective Communications." *Concurrency and Computation: Practice and Experience*, vol. 25, no. 15, pp. 2140–2156, Oct. 2013.

[10] Songqing Chen, Shiping Chen, Xinyuan Wang, Zhao Zhang, and Sushil Jajodia. "An Application Level Data Transparent Authentication Scheme Without Communication Overhead." *IEEE Transactions on Computers*, vol. 59, no. 7, pp. 943–954, 2010.

[11] Diane Rover, Ramon A. Mercado, Zhao Zhang, Mack Shelley, and Daniel S. Helvick. "Reflections on Teaching and Learning in an Advanced Undergraduate Course in Embedded Systems." *IEEE Transactions on Education*, vol. 51, no. 3, pp. 400–412, 2008.

[12] Yong-Joon Park, Gyungho Lee, and Zhao Zhang. "Microarchitectural protection against buffer overflow attack." *IEEE Micro*, vol. 26, no. 4, pp. 62–71, 2006.

[13] Rohit Gupta, Souvik Ray, Arun K. Somani and Zhao Zhang. "Utilizing node's selfishness for providing complete anonymity in peer-to-peer based grids." *Multiagent and Grid Systems*, vol. 2, no. 1, pp. 11–27, 2006.

[14] Zhao Zhang, Zhichun Zhu, and Xiaodong Zhang. "Design and optimization of large size and low overhead off-chip caches." IEEE Transactions on Computers, vol. 53, no. 7, pp. 843–855, 2004.

[15] Zhao Zhang, Zhichun Zhu, and Xiaodong Zhang. "Cached DRAM: A simple and effective technique for memory access latency reduction on ILP processors." IEEE Micro, vol. 21, No. 4, pp. 22–32, 2001.

[16] Zhao Zhang and Xiaodong Zhang. "Fast bit-reversals on uniprocessors and shared-memory multiprocessors." SIAM Journal on Scientific Computing (SISC), vol. 22, no. 6, pp. 2113–2134, 2001.

[17] Zhao Zhang, Zhichun Zhu, and Xiaodong Zhang. "Breaking address mapping symmetry at multilevels of memory hierarchy to reduce DRAM row-buffer conflicts." Journal of Instruction-level Parallelism (JILP), vol. 3, 2001.

[18] Yong Yan, Xiaodong Zhang and Zhao Zhang. "Cacheminer: A runtime approach to exploit cache locality on SMP." IEEE Transactions on Parallel and Distributed Systems (TPDS), vol. 11, no. 4, pp. 357–374, 2000.

Refereed Conference Publications

[1] Yanan Cao, Long Chen, and Zhao Zhang. "Memory Design for Selective Error Protection." To appear in *Proceedings of the 33rd IEEE International Conference on Computer Design* (ICCD), New York, NY, Oct. 18-21, 2015.

[2] Yanan Cao, Long Chen, and Zhao Zhang. "Flexible Memory: A Novel Main Memory Architecture with Block-level Memory Compression." To appear in *Proceedings of the 10th IEEE International Conference on Networking, Architecture, and Storage* (NAS), Boston, MA, Aug. 6–7, 2015.

[3] Long Chen and Zhao Zhang. "MemGuard: A Low Cost and Energy Efficient Design to Support and Enhance Memory System Reliability". In *Proceedings of the 41st International Symposium on Computer Architecture* (ISCA), Minneapolis, MN, Jun. 14–18, 2014, pp. 49–60.

[4] Long Chen, Yanan Cao, and Zhao Zhang. "Free ECC: An Efficient Error Protection for Compressed Last-Level Caches." In *Proceedings of the 31st IEEE International Conference on Computer Design* (ICCD), Asheville, NC, Oct. 6–9, 2013, pp. 278–285.

[5] Sparsh Mittal, Zhao Zhang, and Jeffrey Vetter. "FlexiWay: A Cache Energy Saving Technique Using Fine-grained Cache Reconfiguration." In *Proceedings of the 31st IEEE International Conference on Computer Design* (ICCD), Asheville, NC, Oct. 6–9, 2013, pp. 100–107.

[6] Sparsh Mittal, Zhao Zhang and Yanan Cao. "CASHIER: A Cache Energy Saving Technique for QoS Systems." In *Proceedings of the 26th International Conference on VLSI Design* (VLSID), Pune, India, 2013, pp. 43–38.

[7] Yong Li, Dan Feng, Zhan Shi, and Zhao Zhang. "Disk Array Performance Prediction With CART-MARS Hybrid Models." In *2012 Digest APMRC, Asia-Pacific Magnetic Recording Conference* (APMRC), Signapore, Oct. 31 – Nov. 2, 2012, pp. 1–4.

[8] Sparsh Mittal and Zhao Zhang. "EnCache: Improving Cache Energy Efficiency Using A Software-Controlled Profiling Cache." In *Proceedings of 2012 IEEE International Conference on Electro/Information Technology*, Indianapolis, IN, May 6–8, 2012.

[9] Sparsh Mittal and Zhao Zhang. " Integrating Sampling Approach with Full System Simulation: Bringing Together the Best of Both." In *Proceedings of 2012 IEEE International Conference on Electro/Information Technology*, Indianapolis, IN, May 6–8, 2012.

[10] Kun Fang, Long Chen, Zhao Zhang, and Zhichun Zhu. "Memory Architecture for Integrating Emerging Memory Technologies." In *Proceedings of the 12th International Conference on Parallel Architectures and Compilation Techniques* (PACT), Galveston Island, Texas, September 19–23, 2011, pp. 403–412.

[11] Yong-Joon Park, Zhao Zhang, Songqing Chen. "Run-Time Detection of Malwares via Dynamic Control-Flow Inspection" (poster paper). In *Proceedings of the 20th IEEE International Conference on Application-specific Systems, Architectures and Processors* (ASAP09), Boston, MA, July 7–9, 2009, pp. 223–226.

[12] Jiang Lin, Qingda Lu, Xiaoning Ding, Zhao Zhang, Xiaodong Zhang, and P. Sadayappan. "Enabling Software Multicore Cache Management with Lightweight Hardware Support." In *Proceedings of Supercomputing'09* (SC), Portland, Oregon, Nov. 14–20, 2009, pp. 14:1–14:12.

[13] Qingda Lu, Jiang Lin, Xiaoning Ding, Zhao Zhang, Xiaodong Zhang, and P. Sadayappan. "Soft-OLP: Improving Hardware Cache Performance Through Software-Controlled Object-Level Partitioning." In *Proceedings of the 10th Parallel Architectures and Compilation Techniques* (PACT), Raleigh, North Carolina, Sept. 12–16, 2009, pp. 246–257.

[14] Hongzhong Zheng, Jiang Lin, Zhao Zhang, Zhichun Zhu. "Decoupled DIMM: Building High-Bandwidth Memory System from Low-Speed DRAM Devices." In *Proceedings of the 36th International Symposium on Computer Architecture* (ISCA-36), Austin, TX, June 20–24, 2009, pp. 255–266.

[15] Lakshminarasimhan Seshagiri, Masha Sosonkina, and Zhao Zhang. "Electronic Structure Calculations and Adaptation Scheme in Multi-core Computing Environments." In *Proceedings of 2009*

International Conference on Computational Science (ISC), Baton Rouge, Louisiana, May 25–27, 2009, pp. 3–12.

[16] Hongzhong Zheng, Jiang Lin, Zhao Zhang, Eugene Gorbatov, Howard David, and Zhichun Zhu. "Mini-Rank: Adaptive DRAM Architecture for Improving Memory Power Efficiency." In *Proceedings of the 41st Annual IEEE/ACM International Symposium on Microarchitecture*, Lake Como, Italy, Nov. 8–12, 2008, pp. 210–221.

[17] Qingda Lu, Jiang Lin, Xiaoning Ding, Zhao Zhang, Xiaodong Zhang, and P. Sadayappan. "Profile-Guided Object-level Cache Partitioning" (poster paper). In *Proceedings of Supercomputing 2008* (SC'08), Austin, Texas, Nov. 15–21, 2008, pp. 15–21.

[18] Lei Liu, Songqing Chen, Guanhua Yan, and Zhao Zhang. "BotTracer: Execution-based Bot-like Malware Detection". In *Proceedings of the 11th Information Security Conference* (ISC 2008), Taipei, Taiwan, September 15–18, 2008, pp. 97–113.

[19] Hongzhong Zheng, Jiang Lin, Zhao Zhang, and Zhichun Zhu. "Memory Access Scheduling Schemes for Systems with Multi-Core Processors." In *Proceedings of the 2008 International Conference on Parallel Processing* (ICPP-08), Portland, Oregon, Sep. 8–12, 2008, pp. 406–413.

[20] Jiang Lin, Hongzhong Zheng, Zhichun Zhu, Eugene Gorbatov, Howard David, and Zhao Zhang. "Software Thermal Management of DRAM Memory for Multicore Systems." In *Proceedings of the International Conference on Measurement and Modeling of Computer Systems*, Annapolis, Maryland, Jun. 2–6, 2008, pp. 337–348.

[21] Jiang Lin, Qingda Lu, Xiaoning Ding, Zhao Zhang, Xiaodong Zhang, and P. Sadayappan. "The Impact of Multi-Core Cache Partitioning on Performance, Fairness and QoS: Bridging the Gap between Simulation and Real Systems." In *Proceedings of the 14th International Symposium on High-Performance Computer Architecture*, Salt Lake City, Utah, Feb. 16–20, 2008, pp. 367–378.

[22] Xinwen Zhang, Dongyu Liu, Songqing Chen, Zhao Zhang, and Ravi Sandhu. "Towards Digital Rights Protection in BitTorrent-like P2P Systems". In *Proceedings of the 15th ACM/SPIE Multimedia Computing and Networking* (MMCN 2008), San Jose, CA, Jan. 30–31, 2008.

[23] Rouvik Ray, Giora Slutzki, and Zhao Zhang. "Incentive-Driven P2P Anonymity System: A Game-Theoretic Approach." In *Proceedings of the 2007 International Conference on Parallel Processing* (ICPP-07), XiAn, China, Sep. 10–14, 2007.

[24] Souvik Ray and Zhao Zhang. "An Information-theoretic framework for analyzing leak of privacy in Distributed Hash Tables." In *Proceedings of the Seventh IEEE International Conference on Peer-to-Peer Computing* (P2P 2007), Galway, Ireland, Sep. 2–5, 2007, pp. 27–36.

[25] Souvik Ray and Zhao Zhang. "SCUBE: A DoS-Resistant Distributed Search Protocol." In *Proceedings of the 16th International Conference on Computer Communications and Networks* (ICCCN 2007), Honolulu, Hawaii, Aug. 13–16, 2007, pp. 128–134.

[26] Yong-Joon Park, Zhao Zhang, and Gyungho Lee. "An Efficient Hardware Support for Control Data Validation." In *Proceedings of the 18th IEEE International Conference on Application-specific Systems, Architectures and Processors* (ASAP07), Montreal, Canada, Jul. 8–11, 2007, pp. 409–414.

[27] Jiang Lin, Hongzhong Zheng, Zhichun Zhu, Howard David, and Zhao Zhang. "Thermal Modeling and Management of DRAM Memory Systems." In *Proceedings of the 34th International Symposium on Computer Architecture*, San Diego, California, Jun. 9–13, 2007, pp. 312–322.

[28] Daniel Helvick, Ramon Mercado, Zhao Zhang, and Diane Rover. "Reflections on Implementing and Teaching an Advanced Undergraduate Course in Embedded Systems." In *Proceedings of the 2007 International Conference on Microelectronic Systems Education* (MSE 2007), San Diego, California, Jun. 2–4 2007, pp. 5–6. **Best paper award.**

[29] Jiang Lin, Hongzhong Zheng, Zhichun Zhu, Zhao Zhang, and Howard David. "DRAM-Level prefetching for fully-buffered DIMM: Design, performance and power saving." In *Proceedings of the 2007 IEEE International Symposium on Performance Analysis of Systems and Software* (ISPASS-2007), San Jose, California, Apr. 25–27, 2007, pp. 94–104.

[30] Songqing Chen, Xinyuan Wang, Lei Liu, Xinwen Zhang, and Zhao Zhang. "WormTerminator: An effective containment of unknown and polymorphic fast spreading worms." In *Proceedings of the 2nd ACM/IEEE Symposium on Architectures for Networking and Communications Systems* (ANCS), San Jose, California, Dec. 3–5, 2006, pp. 173–182.

[31] Mikel Bezdek, Daniel Helvick, Ramon Mercado, Diane Rover, Akhilesh Tyagi, and Zhao Zhang. "Developing and Teaching an Integrated Series of Courses in Embedded Computer Systems. In *Proceedings of the 36th Frontier in Education Conference* (FIE 2006), San Diego, CA, Oct. 28–31, 2006, pp. 19–24.

[32] Tien N. Nyugen and Zhao Zhang. "Component-oriented version management for hardware software co-design" (short paper). In *Proceedings of the 2006 conference of the Center for Advanced Studies on Collaborative research* (CASCON'06), Markham, Ontario, Canada, Oct. 16–19, 2006.

[33] Meng-Shiou Wu, Ricky A. Kendall, Zhao Zhang, and Kyle Wright. "Performance modeling and tuning strategies of mixed mode collective communications." In *Proceedings of Supercomputing 2005* (SC'05), Nov. 12–18, 2005, Seattle, WA, pp. 45:1–45:12.

[34] Wei Huang, Jiang Lin, Zhao Zhang, and J. Morris Chang. "Towards pairing Java applications on SMT Processors." In *Proceedings of the 2005 IEEE International Symposium on Modeling,*

Analysis, and Simulation of Computer and Telecommunication Systems (MASCOTS), Oct. 7–14, 2005, Atalanta, Georgia, pp. 7–14.

[35] Joseph Schneider, Mikel Bezdek, Ziyu Zhang, Zhao Zhang, and Diane Rover. "A Platform FPGA-based hardware-software undergraduate laboratory." In *Proceedings of the 2005 International Conference on Microelectronic Systems Education* (MSE-2005), Anaheim, California, Jun. 12–13, 2005, pp. 53–54.

[36] Wei Huang, Jiang Lin, Zhao Zhang, and J. Morris Chang. "Performance Characterization of Java Applications on SMT Processors." In *Proceedings of the IEEE International Symposium on Performance Analysis of Systems and Software* (ISPASS 2005), Austin, Texas, Mar. 20–22, 2005, pp. 102–111.

[37] Zhichun Zhu and Zhao Zhang. "A performance comparison of DRAM memory system optimizations for SMT processors." In *Proceedings of the 8th International Symposium on High Performance Computer Architecture*, San Francisco, California, Feb. 12–16, 2005, pp. 213–224.

[38] Souvik Ray and Zhao Zhang. "An efficient anonymity protocol in grid computing." In *Proceedings of the 5th IEEE/ACM International Workshop on Grid Computing* (Grid 2004), Pittsburgh, Pennsylvania, Nov. 8, 2004, pp. 200–207.

[39] Zhichun Zhu, Zhao Zhang, and Xiaodong Zhang. "Fine-grain priority scheduling on multi-channel memory systems." In *Proceedings of the 8th International Symposium on High Performance Computer Architecture*, Cambridge, Maryland, Feb. 2–6, 2002, pp. 107–116.

[40] Zhao Zhang, Zhichun Zhu, and Xiaodong Zhang. "A permutation-based page interleaving scheme to reduce row-buffer conflicts and exploit data locality." In *Proceedings of the 33rd Annual IEEE/ACM International Symposium on Microarchitecture*, Monterey, California, Dec. 10–13, 2000, pp. 32–41.

[41] Zhao Zhang and Xiaodong Zhang. "Cache-optimal methods for bit-reversals." In *Proceedings of ACM/IEEE Supercomputing Conference* (SC'99), Portland, Oregon, November 1999, pp. 26:1–26:18.

[42] Yong Yan, Xiaodong Zhang, and Zhao Zhang. "A memory-layout oriented run-time technique for locality optimization." In *Proceedings of the 1998 International Conference on Parallel Processing* (ICPP'98), Minneapolis, Minnesota, August 1998, pp. 189–196.

FUNDED PROPOSALS

[1] Zhao Zhang. "SHF: Medium:Collaborative Research: Architectural and System Support for Building Versatile Memory Systems." NSF, $375,000, 07/01/2015 – 06/31/2019. Total funding $900,000, in collaboration with OSU and UIC.

[2] Zhao Zhang. "CSR: Small: Software Cache Memory Managements with Reconfigurable Hardware Emulators." NSF, $360,345, 08/01/2011 – 07/31/2015.

[3] Zhao Zhang. REU, "Collaborative Research: CSR-PSCE, TM: Effective Resource Sharing and Coordination inside Multicore Processors for High Throughput Computing." NSF, $12,000, 07/17/2009 – 08/31/2011.

[4] Zhao Zhang. REU, "Collaborative Research: CSR-PSCE, SM: Memory Thermal Management for Multi-Core Systems." NSF, $12,000, 07/17/2009 – 08/31/2011.

[5] Zhao Zhang. "Collaborative Research: CSR-PSCE, TM: Effective Resource Sharing and Coordination inside Multicore Processors for High Throughput Computing" NSF, $179,999, 09/01/2008 – 08/31/2011. Total funding $521,999, in collaboration with OSU.

[6] Zhao Zhang. "Collaborative Research: CSR-PSCE, SM: Memory Thermal Management for Multi-Core Systems." NSF, $160,000, 09/01/2008 – 08/31/2011. Total funding $320,000, in collaboration with UIC.

[7] Tien Nguyen, Zhao Zhang, Diane Rover, and Mack Shelley. "Improving Embedded System Education with Software Engineering Methodologies." NSF, $149,999, 03/10/2008 – 03/09/2010.

[8] Zhao Zhang. "Collaborative Research: CSR-SMA: Thermal Modeling, Simulation and Management of Memory Subsystems for Multi-Core Systems." NSF, $40,000, 08/01/2007 – 07/31/2008. Total funding $80,000, in collaboration with UIC.

[9] Zhao Zhang. "Collaborative research: Memory Access Throttling for Highly Multithreaded Processors." NSF, $180,000, 05/01/2006 – 05/01/2009. Total funding $360,000, in collaboration with UIC.

[10] Zhao Zhang. "SGER: Fast and scalable simulation for multicore and multithreaded processor by using commodity FPGA boards." NSF, $100,947, 09/15/05 – 11/31/06.

[11] Srikanta Tirthapura (PI) and Zhao Zhang (PI). "A theoretical foundation for job scheduling in grid computing." University Research Grant, Iowa State University, $18,000 (share $9,000), 09/01/04 – 09/01/05.

TEACHING EXPERIENCES

CprE 288, Introduction to Embedded Systems, Iowa State University, Fall 2014

CprE/ComS 681, Advanced Topics in Computer Architecture, Spring 2014

CprE 381, Computer Organization and Assembly Level Programming, Iowa State University, Fall 2013

CprE 288, Introduction to Embedded Systems, Iowa State University, Fall 2013

CprE 381, Computer Organization and Assembly Level Programming, Iowa State University, Fall 2012

CprE 288, Introduction to Embedded Systems, Iowa State University, Fall 2012

CprE 488, Embedded Systems Design, Iowa State University, Spring 2012

CprE/ComS 681, Advanced Topics in Computer Architecture, Spring 2012

CprE 288, Introduction to Embedded Systems, Iowa State University, Fall 2011

CprE 488, Embedded Systems Design, Iowa State University, Spring 2011

CprE 288, Introduction to Embedded Systems, Iowa State University, Fall 2010

CprE 581, Computer Systems Architecture, Iowa State University, Fall 2010

CprE 488, Embedded Systems Design, Iowa State University, Spring 2010

CprE 288, Introduction to Embedded Systems, Iowa State University, Spring 2010

CprE 581, Computer Systems Architecture, Iowa State University, Fall 2009.

CprE 488, Embedded Systems Design, Iowa State University, Spring 2009.

CprE 288, Introduction to Embedded Systems, Iowa State University, Spring 2009.

CprE 581, Computer Systems Architecture, Iowa State University, Fall 2008.

CprE 288, Introduction to Embedded Systems, Iowa State University, Spring 2008.

CprE 581, Computer Systems Architecture, Iowa State University, Fall 2007.

CprE 488, Embedded Systems Design, Iowa State University, Fall 2007.

CprE 211, Microcontrollers and Digital Systems Design, Iowa State University, Spring 2007.

CprE 581, Computer Systems Architecture, Iowa State University, Fall 2006.

CprE 488X, Embedded Systems Design, Iowa State University, Fall 2006.

CprE 211, Microcontrollers and Digital Systems Design, Iowa State University, Spring 2006.

CprE 581, Computer Systems Architecture, Iowa State University, Fall 2005.

CprE 488X, Embedded Systems Design, Iowa State University, Fall 2005.

CprE 211, Microcontrollers and Digital Systems Design, Iowa State University, Summer 2005.

CprE 585, Advanced Computer Architecture, Iowa State University, Fall 2004.

CprE 211, Microcontrollers and Digital Systems Design, Iowa State University, Spring 2004.

CprE 585, Advanced Computer Architecture, Iowa State University, Fall 2003.

CprE 305, Computer Organization and Design, Iowa State University, Spring 2003.

CprE 585, Advanced Computer Architecture, Iowa State University, Fall 2002.

PROFESSIONAL ACTIVITIES

[1] Editorial Board, Parallel and Distributed Computing and Networks, ACTA Press, 2011-present.

[2] Program Co-Chair, *The 9th IEEE International Conference on Networking, Architecture, and Storage* (NAS 2014), Tianjin, China, August 6-8, 2014.

[3] Program Committee, *The 14th IEEE/ACM International Symposium on Cluster, Cloud and Grid Computing* (CCGrid), Chicago, IL., May 26-29, 2014.

[4] NSF Panelist, March 2014.

[5] NSF Panelist, March 2013.

[6] Program Committee, *The 2013 IEEE/ACM International Conference on Green Computing and Communication* (GreenCom), Beijing, China, August 20-23, 2013.

[7] Program committee, the Fifth International Conference on Evolving Internet (INTERNET 2013), Nice, France, July 21 - 26, 2013.

[8] Vice program chair for the Architecture Track, *The 8th IEEE International Conference on Networking, Architecture, and Storage* (NAS 2013), Xi'an, Shaanxi, China, July 10-12, 2013.

[9] NSF Panelist, September 2012.

[10] Program Committee, *The 2011 IEEE International Symposium on Performance Analysis of Systems and Software* (ISPASS), Austin, TX, April 10-12, 2011.

[11] Program Committee, *The Sixth Annual Workshop on the Interaction between Operating Systems and Computer Architecture* (WIOSCA), Saint-Malo, France, June 2010.

[12] NSF Panelist, CISE/CNS/CSR (Computer Systems Research), May 2010.

[13] Program Committee Member, *The Fifth IEEE International Symposium on Embedded Computing* (SEC 2008), Beijing, China, October 6-8, 2008.

[14] Program Committee Member, *The 2008 IEEE International Conference on Networking, Architecture, and Storage*, Chongqing, Sichuan, China, June 12-14, 2008.

[15] Program Committee Member, *The 2008 International Conference on Embedded Software and Systems*, Chengdu, Sichuan, China, July 29-31, 2008.

[16] Program Committee Member and Session Chair, *The 12th International Conference on Parallel and Distributed Systems* (ICPADS), Minneapolis, Minnesota, July 12-15, 2006.

[17] Program Committee Member, *The 2006 International Conference On Parallel Processing* (ICPP-06), Columbus, Ohio, August 14-18, 2006.

[18] NSF Panelist, October 2005.

[19] NSF Reviewer, November 2005.

[20] Program Committee Member, *The 2nd International Conference on Embedded Software and Systems* (ICESS-2005), Xi'an, China, December 16-18, 2005.

[21] Program Committee Member, *The 9th Annual Workshop on Interaction between Compilers and Computer Architectures* (Interact-9), San Francisco, California, February 2005.

[22] Program Committee, *The 8th Annual Workshop on Interaction between Compilers and Computer Architectures* (Interact-8), Madrid, Spain, February 2004.

[23] Program Committee, *The 2004 International Conferences on Parallel and Distributed Systems* (ICPADS 2004), Newport Beach, California, July 2004.

[24] Reviewer for IEEE Transactions on Parallel and Distributed Systems, IEEE Transactions on Computers, IEEE Transactions on Signal Processing, IEEE Micro, Journal of Parallel and Distributed Computing, Microprocessors and Microsystems (Elsevier).