HVDC-Learn: Modular Education & Workforce Training in High Voltage Direct Current Electric Transmission Application

Topic 3d

Modular multilevel converter as HVDC converter interface and its control

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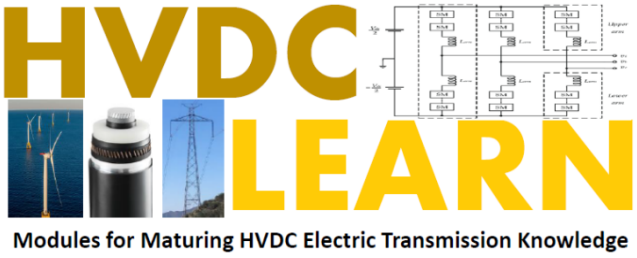

3.d. Modular multilevel converter as HVDC converter interface and its control

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Prerequisite Competencies:	1. VSC-HVDC converter station technologies – Module 2b 2. Power electronics 101: fundamentals of switching power converters – Module 3b 3. Operation of thyristors and IGBTs in converters – Module 3c
Module Objectives:	1. Understand the advantages and disadvantages of using multilevel converters for VSC-based HVDC interfaces. 2. Know the fundamental operating principals of individual levels/modules in a MMC and overall converter. 3. Identify some of the common PWM techniques to control a MMC. 4. Demonstrate knowledge of the process to determine module number, submodule capacitance, and arm inductance in an MMC. 5. Understand the need for submodule voltage balancing, circulating current suppression, and startup schemes in MMCs.

Abstract

This section explores the design of modular multilevel converters (MMC), which are critical in HVDC systems for handling high voltage levels using low-voltage power electronic devices like Insulated Gate Bipolar Transistors (IGBTs). Topics include the structure and operation of MMCs, submodule functions, equivalent circuit derivation, and operation principles. Various modulation methods are covered, such as nearest level control and different pulse width modulation (PWM) techniques. The section also addresses design challenges such as submodule capacitance and arm inductance requirements, capacitor balancing, circulating current control, and startup scheme.

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List of Acronyms

APOD	Alternating phase opposition displacement
CDSM	Clamp double submodule
CHB	Cascaded H-bridge
CLS-PWM	Carrier level shifted pulse width modulation
CPS-PWM	Carrier phase shifted pulse width modulation
DSP	Digital signal processor
FPGA	Field programmable gate array
GSCC	Grouping sequentially charge control
HVAC	High voltage alternating current
HVDC	High voltage direct current
IGBT	Insulated gate bipolar transistor
KVL	Kirchoff's voltage law
LCC	Line commutated converter
MOSFET	Metal oxide semiconductor field effect transistor
MTDC	Multiterminal direct current
GA	Genetic algorithm
MMC	Modular multilevel converter
NLM	Nearest level modulation
PD-PWM	Phase displacement pulse width modulation
PS-PWM	Phase shift pulse width modulation
POD	Phase opposition displacement
PSO	Particle swarm optimization
PWM	Pulse width modulation
SHE	Selective harmonic elimination
SiC	Silicon carbide
SM	Submodule
SPWM	Sinusoidal pulse width modulation
THD	Total harmonic distortion
TH-PWM	Third harmonic injection pulse width modulation
VSC	Voltage source converter

Nomenclature

C_{sub}	submodule capacitance
D	diode, many times used in antiparallel with IGBT or MOSFET
e_j	inner electromotive force (voltage) in phase leg j where j = a, b, c
f_c	carrier frequency
i_{circ}	circulating current – current that flows in upper and lower arm
i_j	phase j output current where j = a, b, c
i_n	current in lower arm of MMC converter
i_p	current in upper arm of MMC converter
L	inductor
m_a	amplitude modulation index
R	resistor
T_x	converter switching device – typically IGBT
u_c	voltage across MMC submodule capacitor
u_{comj}	phase j common voltage (voltage common to upper and lower arm)
u_n	lower arm voltage
u_p	upper arm voltage
u_{sm}	submodule output voltage
v^*	voltage reference or modulation voltage
V_c	voltage across submodule capacitor
V_{dc}	HVDC voltage

1 Introduction

Multilevel converters have enabled relatively low voltage power electronic devices such as IGBTs to be connected in a modular way to form converters that can span the high voltages needed to interface between ac high voltage (HV) transmission systems and HVDC transmission systems. Voltage source converters (VSCs) connected in a multilevel modular fashion have now become a primary option to line commutated converters (LCCs) especially at voltages up to 400 kV.

The concept of multilevel converters has been introduced since 1975 [1]. The term multilevel began with the three-level converter [2]. Subsequently, several multilevel converter topologies have been developed [3]-[10]. The basic concept of a multilevel inverter to achieve higher power is to use a series of power semiconductor switches with several lower voltage dc sources to perform the power conversion by synthesizing a staircase voltage waveform that approximates a sinewave. Capacitors, batteries, and renewable energy voltage sources can be used for these multiple dc voltage sources. The commutation of the power switches aggregates these multiple dc sources to achieve high voltage at the output; however, the rated voltage of the power semiconductor switches depends only on the rating of the dc voltage sources to which they are connected. One unique aspect of multilevel converters is their ability to share the voltage blocking needed to span the HVDC, but not have them all commutate at the same instant as the case in LCC type converters where the series connected devices need to all switch at the same time.

VSC-HVDC converter stations may contain several MMCs in series and/or in parallel to achieve total system dc voltage ratings of up to 1,100 kV. In VSC-HVDC converter stations, the MMC can be built with anywhere from 200 to 400 levels [11]. An HVDC system includes at least one MMC operating as a rectifier (converting the HVAC to HVDC) and at least another one operating as an inverter (converting HVDC to HVAC). The MMC operating as a rectifier will convert the power from an ac grid to the dc network, while the MMC operating as the inverter will convert the power from the dc network to another, second ac grid. Typical two-terminal HVDC systems will have two converter stations and transfer the power between these two stations through a hvdc line. Multi-terminal direct current (MTDC) systems may contain several converter stations and coordinate the power transfer across all converter stations over the dc grid [12]. Much of the content in this module is drawn from a book chapter and dissertations written by the authors which can be found in the bibliography section at the end of the module.

INDUSTRY INSIGHT

The first MMC-based HVDC system, Trans Bay Cable project [13], was completed in 2010 in San Francisco. The Trans Bay Cable is an underwater electric transmission interconnection between San Francisco, California and Pittsburg, California [14]. The 53-mile cable under San Francisco Bay and through the Carquinez Strait can transmit 400 MW of power at a dc voltage of ±200 kV, enough to provide 40% of San Francisco's peak power needs [15]. MMC-based HVDC systems are also widely used in offshore wind farm integration [16]. Ultra-high voltage DC projects have also been proposed that use a combination of full-bridges and half-bridges for the MMC modules.

2 Operating Principle of MMC

2.1 Circuit Configuration

The modular multilevel converter (MMC) was first introduced by Marquardt in 2001 [17]. The configuration of a MMC is shown in Figure 1(a). Each phase leg of the MMC consists of one upper and one lower arm connected in series between the dc terminals. N series-connected submodules (SMs) and one arm inductor L_{arm} form an arm. Each SM can be realized by a half-bridge [18], [19] (Figure 1(b)), H-bridge [20], [21] (Figure 1(c)), or clamp-double [22] circuit (Figure 1(d)).

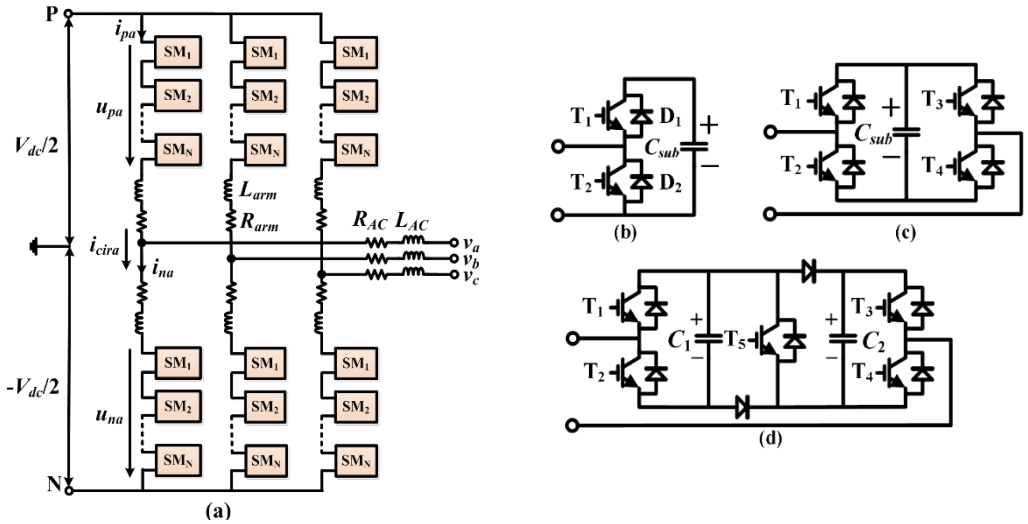

Figure 1. (a) Circuit configuration of a MMC with (b) half-bridge cell, (c) full-bridge cell, and (d) clamp-double cell.

INDUSTRY INSIGHT

The MMC with half-bridge SM does not have any intrinsic fault current-limiting or current-blocking capability. Under a dc short-circuit fault, the fault current can flow from the ac side to the faulted dc side through the anti-paralleled diodes of the controllable power switches, even though these switches are turned off. Therefore, fast-acting dc breakers are necessary to protect the system from damage. These dc circuit breakers are expensive and difficult to manufacture at the moment. On the other hand, the full-bridge (also called H-bridge) SM can generate negative capacitor voltage, which can be used to block the fault current; thus these converters do not require dc circuit breakers for fault protection. However, compared with the half-bridge SM, the H-bridge MMC has twice the number of semiconductor devices, leading to higher cost and operating losses. However, the inherent fault current limiting ability in the H-bridge has made this the more widely used circuit by industry in their HVDC interface units deployed to date. For the clamp-double SM in Figure 1(d), power device T_5 always conducts under normal operation conditions, making the clamp-double SM equivalent to two series-connected half-bridge SMs. Under a dc side fault, T_5 is turned off, and dc voltage is inserted by both capacitors to minimize the dc fault current. Compared with the H-bridge SM, the output voltage of clamp-double SM can be doubled, with additional conduction loss of T_5.

Due to its lower cost and higher efficiency, the MMC with half-bridge SMs is also used in commercial HVDC projects [23]. Therefore, the basic operation principle of an MMC with half bridge will be introduced in this section [23]. As illustrated in Figure 2, each half-bridge SM contains two silicon IGBTs (or in the future could be high voltage (10 kV) silicon carbide MOSFETs or other similar wide bandgap (WBG) power electronic switches) as switching elements and a DC storage capacitor C_{sub}. If the lower switch is open and the upper switch is closed, the SM (capacitor voltage) is inserted (Figure 2(b)) into the MMC arm, while the SM is bypassed if the lower switch is closed and the upper switch is open (Figure 2(c)). Three different states are relevant for the proper operation of an SM, as illustrated in Figure 2. Note that for each of the three states, the current flow direction will determine which power electronic elements are conducting and whether the capacitor will be charging, discharging, or be bypassed.

1. Both IGBTs are switched off (Figure 2(a)). This case does not occur during normal operation with power transfer, but it is typically used for two conditions: (1) startup and charging of the MMC's capacitors or (2) during a sustained line fault and the need to stop power flow. If the current flows from the AC terminal to the dc side during this state, the flow passes through diode D_1 and charges the capacitor. When it flows in the opposite direction, the freewheeling diode D_2 conducts and bypasses the capacitor.

2. IGBT1 (T_1) is switched on, and IGBT2 (T_2) is switched off (Figure 2(b)). Irrespective of the current flow direction, the voltage of the storage capacitor is applied to the terminals of the SM. This is referred to as "inserting" the module's voltage into the overall dc link voltage. Depending on the current direction, the current either flows through D_1 and charges the SM capacitor or flows through T_1 and discharges the SM capacitor.

3. IGBT1 is switched off, and IGBT2 is switched on (Figure 2(c)). No voltage is inserted from this SM into the overall dc link voltage. In this case, the current flows through either T_2 or D_2 depending on its direction, which ensures that zero voltage is applied to the terminals of the SM. The voltage in the capacitor remains unchanged.

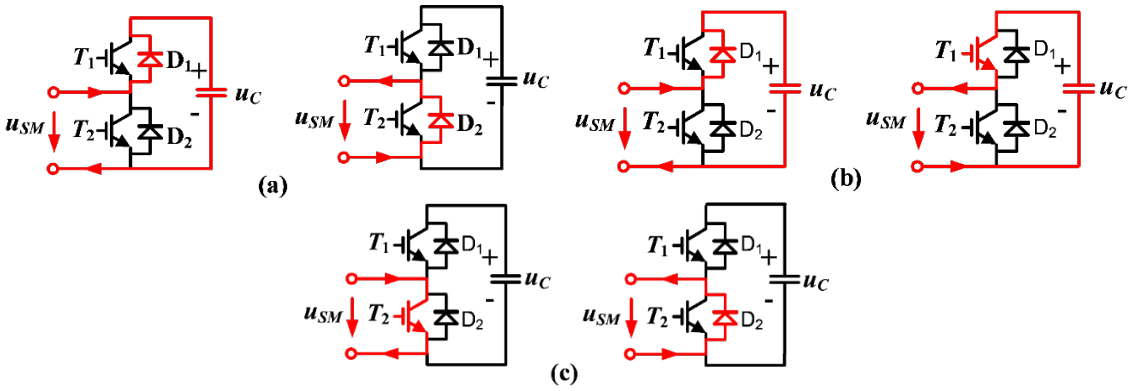

Figure 2. States and current paths of a SM in the MMC converter, (a) Startup or fault protection state: Both IGBTs are switched off, (b) Insert state: IGBT1 is switched on, IGBT2 is switched off, (c) Bypass state: IGBT1 is switched off, IGBT2 is switched on.

2.2 Equivalent Circuit

Each of the individual SMs in a converter leg can be separately and selectively controlled. In principle, the two converter arms of each phase represent a controllable voltage source. In this arrangement, the total voltage generated by the upper and lower arm SMs in one phase unit should be equal to the dc link voltage. By adjusting the output voltage of SMs in both arms, that is, inserting and bypassing of SM capacitors according to a switching pattern created by a modulator, the desired sinusoidal voltage at the AC terminal can be achieved through a staircase approximation.

Figure 3 illustrates the equivalent single-phase circuit of the MMC. L and R are the arm inductance and equivalent arm resistance, respectively. V_{dc} and I_{dc} are the total hvdc bus voltage and individual dc current. v_j is the ac terminal voltage of phase j ($j = a, b, c$), whereas i_j is the corresponding ac line current for each phase j.

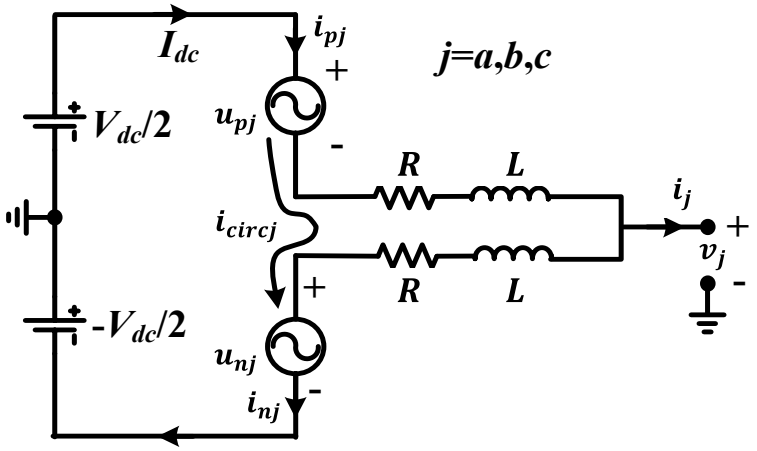

Figure 3. Single phase equivalent circuit of the MMC.

The arm voltages generated by the cascaded SMs are expressed as u_{pj} and u_{nj}, where the subscripts p and n denote the upper (positive) and lower (negative) arms, respectively. i_{pj} and i_{nj} are the corresponding arm currents, which can be expressed as

$$\begin{aligned} i_{pj} &= \frac{i_j}{2} + i_{circj} \\ i_{nj} &= \frac{i_j}{2} - i_{circj} \end{aligned} \tag{1}$$

where i_{circj} denotes the inner common mode circulating current, which flows through both the upper and lower arms and is given as

$$i_{circj} = \frac{i_{pj}+i_{nj}}{2} \tag{2}$$

According to [24], the MMC can be characterized by the following equations:

$$v_j = e_j - \frac{R}{2} \cdot i_j - \frac{L}{2} \cdot \frac{di_j}{dt} \tag{3}$$

$$R \cdot i_{circj} + L \cdot \frac{di_{circj}}{dt} = \frac{V_{dc}}{2} - \frac{u_{nj}+u_{pj}}{2} \tag{4}$$

where e_j in (3) is the inner electromotive force (EMF) generated in phase j and

$$e_j = \frac{u_n - u_p}{2} \tag{5}$$

According to (3), when u_j is regarded as the ac network voltage, the current i_j can be controlled directly by regulating the control variable e_j.

The inner dynamic performance of the MMC is characterized by (4) and can be redefined as

$$u_{com} = \frac{u_{nj}+u_{pj}}{2} = \frac{V_{dc}}{2} - R \cdot i_{circ} + L \cdot \frac{di_{circ}}{dt} \tag{6}$$

where u_{comj} is the common mode voltage of upper and lower arm in phase j. According to (6), the circulating current i_{circj} can be controlled by regulating the common mode voltage u_{comj}.

Combining (5) and (6), the arm voltage references are

$$\begin{aligned} u_{pj} &= u_{comj} - e_j \\ u_{nj} &= u_{comj} + e_j \end{aligned} \tag{7}$$

Because the same voltage u_{comj} is subtracted from u_{pj} and u_{nj}, according to (3) and (5), the resulting e_j will not change, and thus, the ac side dynamics are not affected. As previously described, the reference of e_j is generated from the traditional system control loops, whereas the inner unbalance voltage u_{comj} can be used to control the MMC inner dynamic performance including the three-phase inner circulating currents, which will be further introduced in Section 4.2.

2.3 Modulation Methods

Numerous multilevel modulation methods can be applied to MMC, and each multilevel modulation scheme has its own uniqueness, making it more suitable for specific applications. In general, low switching frequency modulation methods are preferred for high-power applications due to lower switching loss, while high switching frequency algorithms enable better output power quality and higher bandwidth and thus are more suitable for high-dynamic-range applications.

In general, multilevel converter modulation strategies can be classified according to switching frequency as shown in Figure 4. Two widely used low frequency, or fundamental frequency (60 Hz), modulations are nearest level modulation (NLM) and selective harmonic elimination (SHE). These two modulation strategies will be discussed in Section 2.3.1. For MMCs in HVDC applications, which typically consist of hundreds of SMs, the NLM method is commonly employed to minimize switching losses and generate a staircase waveform that closely approximates a sinewave.

For the high-frequency multilevel modulation methods, pulse-width modulation (PWM) strategies used in a conventional two-level inverter can be modified to use in multilevel

converters. The most discussed multilevel PWM methods in the literature have been multilevel carrier-based PWM, selective harmonic elimination PWM, and multilevel space vector PWM, which are all extensions of traditional two-level PWM strategies to several levels. Among the three aforementioned multilevel PWM methods, carrier-based PWM methods are typically applied in MMCs with a smaller number of SMs, such as those in motor drive applications, which will be discussed in Section 2.3.2.

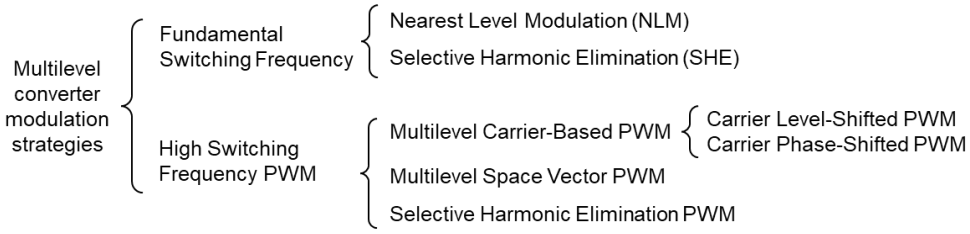

Figure 4. Classification of multilevel converter modulation strategies.

2.3.1 Fundamental Frequency Switching Methods

2.3.1.1 Nearest Level Modulation

Nearest Level Modulation (NLM) is the simplest and most widely used modulation method for multilevel converters. The basic idea of NLM is to choose the discrete voltage level that is the closest to the voltage reference, as illustrated in Figure 5, wehre v^* is the sinusoidal reference voltage and v is the staircase output voltage of the MMC. The switching states and dwell times are directly computed from the reference phase voltage. This scheme is easy to implement in digital controllers, and therefore, is the most practical PWM method for high voltage applications such as HVDC systems. The NLM method suffers high total harmonic distortion (THD) when the voltage levels and/or modulation indexes are low, which is typically not the case in HVDC interface converters. Thus, the unfiltered THD is typically less than 2% in HVDC output voltages.

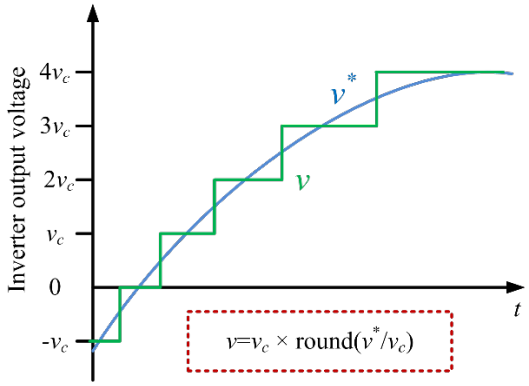

Figure 5. Waveform synthesis using nearest level modulation (NLM).

The basic idea of NLM is to first calculate how many SMs should be inserted to provide the reference voltage (summation of the inserted individual SM capacitor voltages), and then to determine which SMs will be used by capacitors' voltage sorting and the direction of the arm

current. If we assume that the output voltage reference is v^* and the output SM voltage has a step value equal to v_c. The expected output voltage can be calculated as

$$v = v_c \cdot \text{round}_{0.5}\left(\frac{v^*}{v_c}\right) \tag{8}$$

The round function $\text{round}_{0.5}(x)$ refers to a function that will round x to the nearest integer. Once the output voltage level is determined, the converter controller will determine the feasible switching patterns (which particular SMs to insert) to realize the calculated voltage level.

A N-level MMC contains $2(N-1)$ submodules without redundant submodules. (Most MMCs also have a few redundant submodules that can be used in case of a failure and bypass of the failed SM). The average voltage of the submodules is V_c. Assume that the output voltage is expected to be mV_c, where m is the level of output voltage. To realize this output voltage, m submodules from the MMC lower arm will be in the inserting mode, whereas a complementary $(N-1-m)$ submodules from the MMC upper arm will be in the inserting mode. The MMC controller will measure the arm current direction and sort the submodules by their capacitor voltage values, and determine which m submodules from the lower arm and $(N-1-m)$ submodules from the upper arm will be inserted. The MMC controller determines the optimal switching patterns that meet the output voltage level command and secure the safe operation for the MMC at the same time.

2.3.1.2 Selective Harmonic Elimination

The selective harmonic elimination method is also called fundamental switching frequency method based on the harmonic elimination theory proposed by Patel and Hoft [25], [26]. A typical 11-level multilevel converter output with fundamental frequency switching scheme is shown in Figure 6.

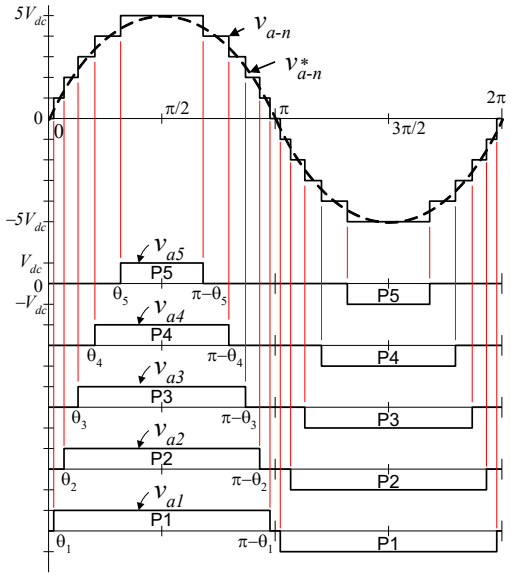

Figure 6. Output 11-level phase voltage waveform of an MMC with 5 SMs in one arm (*N*=5).

The Fourier series expansion of the output voltage waveform as shown in Figure 6 can be expressed as follows:

$$V(\omega t) = \frac{4V_{\mathrm{dc}}}{\pi}\sum_n[cos(n\theta_1) + cos(n\theta_2) + \cdots + cos(n\theta_{\mathrm{s}})]\frac{sin(n\omega t)}{n}, \text{ where } n = 1, 3, 5, 7, \ldots \quad (9)$$

From (9), the magnitudes of the Fourier coefficients when normalized with respect to V_{dc} are as follows:

$$H(n) = \frac{4}{\pi n}[cos(n\theta_1) + cos(n\theta_2) + \cdots + cos(n\theta_{\mathrm{s}})], \text{ where } n = 1, 3, 5, 7, \ldots \quad (10)$$

The conducting angles, $\theta_1, \theta_2, \ldots, \theta_s$, can be chosen such that the voltage total harmonic distortion is a minimum. Normally, these angles are chosen so as to cancel the predominant lower frequency harmonics [27] and then small filters can be used if needed for the residual higher frequency harmonics.

For the 11-level case ($N = 5$) in Figure 6, the 5th, 7th, 11th, and 13th harmonics can be eliminated with the appropriate choice of the conducting angles. One degree of freedom is used so that the magnitude of the fundamental waveform corresponds to the reference waveform's amplitude or modulation index, m_a, which is defined as V_L^*/V_{Lmax}. V_L^* is the amplitude command of the inverter for a sine wave output phase voltage, and V_{Lmax} is the maximum attainable amplitude of the converter, i.e. $V_{Lmax} = N \cdot V_{dc}$. Equations for deciding the conducting angles can be derived from Eq. (10) as follows:

$$\begin{gathered}
\cos(5\theta_1) + \cos(5\theta_2) + \cos(5\theta_3) + \cos(5\theta_4) + \cos(5\theta_5) = 0 \\
\cos(7\theta_1) + \cos(7\theta_2) + \cos(7\theta_3) + \cos(7\theta_4) + \cos(7\theta_5) = 0 \\
\cos(11\theta_1) + \cos(11\theta_2) + \cos(11\theta_3) + \cos(11\theta_4) + \cos(11\theta_5) = 0 \\
\cos(13\theta_1) + \cos(13\theta_2) + \cos(13\theta_3) + \cos(13\theta_4) + \cos(13\theta_5) = 0 \\
\cos(\theta_1) + \cos(\theta_2) + \cos(\theta_3) + \cos(\theta_4) + \cos(\theta_5) = 5m_a
\end{gathered} \quad (11)$$

The above equations are nonlinear transcendental equations that can be solved by an iterative method such as the Newton–Raphson method. For example, using an amplitude modulation index of 0.8 obtains the following: $\theta_1 = 6.57°, \theta_2 = 18.94°, \theta_3 = 27.18°, \theta_4 = 45.14°, \theta_5 = 62.24°$. Thus, if the inverter output is symmetrically switched during the positive half cycle of the fundamental voltage to $+V_{dc}$ at 6.57°, $+2V_{dc}$ at 18.94°, $+3V_{dc}$at 27.18°, $+4V_{dc}$ at 45.14°, and $+5V_{dc}$ at 62.24°, and similarly in the negative half cycle to $-V_{dc}$ at 186.57°, $-2V_{dc}$ at 198.94°, $-3V_{dc}$ at 207.18°, $-4V_{dc}$ at 225.14°, $-5V_{dc}$ at 242.24°, the 11-level output voltage will not contain the 5th, 7th, 11th, and 13th harmonic components [28]. Other methods to solve these equations include using genetic algorithms [29], particle swarm optimization (PSO) [30], and resultant theory [31].

Practically, the pre-calculated switching angles are stored as data in memory (look-up table). Therefore, a microcontroller could be used to generate the PWM gate drive signals. More recent methods have been developed that can generate switching angles in real time using genetic algorithms (GAs). The calculated angles using GAs may not completely eliminate low frequency harmonics, but these values would be so low that they would have little negative consequences on the system [29], [31].

2.3.2 Carrier-based PWM Techniques

Several different two-level, carrier-based PWM techniques have been extended to multiple levels as a means for controlling the active devices in a multilevel converter. The most popular and easiest technique to implement uses several triangle carrier signals and one reference, or modulation, signal per phase. The multicarrier techniques have been successfully extended for MMC and other multilevel topologies by using multiple carriers to control power switches of the converter topologies. It is mainly divided into two types: (1) carrier level-shifted PWM (CLS-PWM) and (2) carrier phase-shifted PWM (CPS-PWM) [33], [34].

- **Carrier Level-Shifted PWM**

Figure 7 illustrates three major multicarrier techniques used in a conventional inverter that can be applied in a multilevel inverter: sinusoidal PWM (SPWM), third-harmonic injection PWM (TH-PWM), and space vector PWM (SVM). SPWM is a very popular method in industrial applications, which is shown in Figure 7(a). To increase the linear modulation region (and avoid over-modulation or pulse dropping when operating at high voltage amplitude modulation indices), it is possible to add a third harmonic to the reference waveform for three-phase three-wire systems. This can yield an increase of up to 15% in the linear modulation region and is similar to what is achieved with space vector PWM [35]-[38]. As can be seen in Figure 7(b) and (c), the reference signals have some margin at unity amplitude modulation index. Obviously, the dc utilization of TH-PWM and SVM are better than SPWM in the linear modulation region. The dc utilization means the ratio of the output fundamental voltage to the dc link voltage.

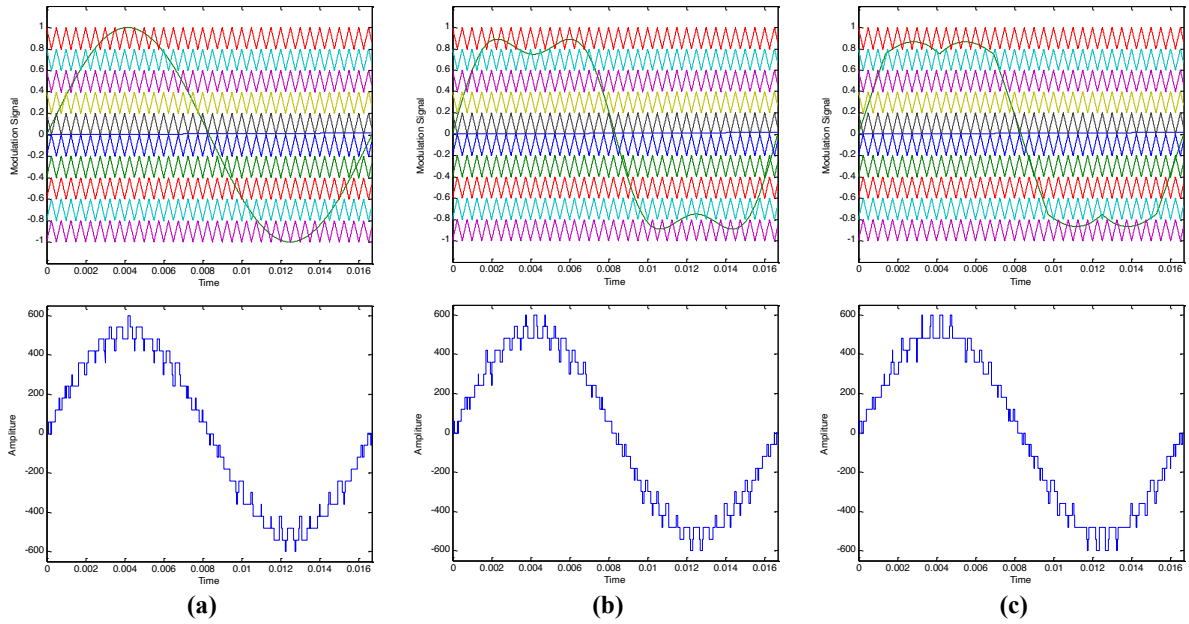

Figure 7. Modulation signals and their line–line output voltage with three major conventional carrier-based PWM techniques at unity modulation index and 2-kHz carrier frequency: (a) SPWM; (b) TH-PWM; and (c) SVM.

The carriers can be arranged with shifts in amplitude, relating each carrier with the corresponding individual output voltage level generated by the multilevel inverter, which is the

so-called carrier level-shifted PWM (CLS-PWM). Depending on the disposition of the carriers, three types of CLS-PWM have been developed: phase disposition (PD), phase opposition disposition (POD), and alternate phase opposition disposition (APOD), as shown in Figure 8 [39].

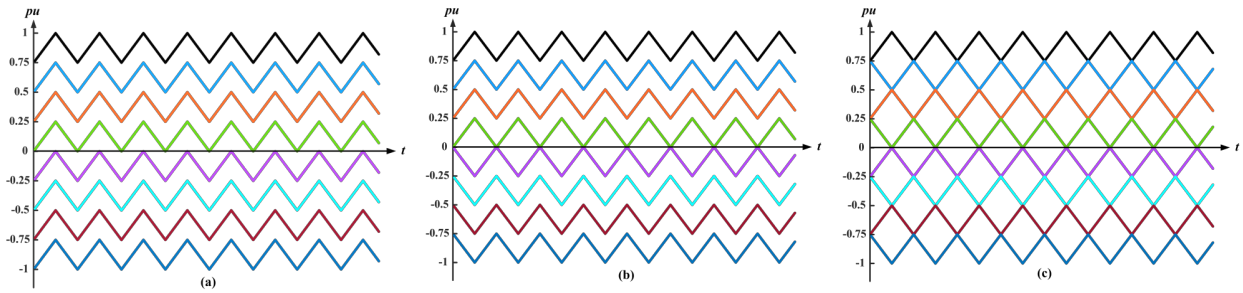

Figure 8. Carrier waves for CLS-PWM: (a) PD, (b) POD, (c) APOD.

The PD-PWM method is realized through a comparison between a sinusoidal reference wave with vertically shifted carrier waves. N carrier signals will be created to generate an output voltage with N+1 levels. The carrier signals have the same amplitude and frequency, and all signals are in phase. In the POD-PWM method, all carrier signals above the zero axis (positive region) are in phase, and those below zero axis (negative region) are also in phase but 180 degrees phase shifted from the carrier waves in the positive region. The APOD-PWM scheme uses $N-1$ carrier signals with alternating phase shift of 180 degrees from each other.

The CLS-PWM methods can be adopted for any multilevel converter topology. However, they cannot directly apply to CHB (cascaded H-bridge converter) and MMC inverters. According to the modulation principle, the uppermost SMs will be inserted for a short time, while the middle ones insert for most of the time during a fundamental cycle, producing an uneven power dissipation and large capacitor voltage differences among the SMs. Methods have been developed for more even sharing of power among the levels though this adds a slight complexity to the control algorithms [40], [41].

- **Carrier Phase-Shifted PWM**

For an MMC with $2N$ cells, the carrier waves (either sawtooth or triangular waveforms) with a phase shift of $360°/N$ or $180°/N$ can be employed to generate the staircase multilevel output waveform with low distortion. This technique is referred to as carried phase-shifted PWM (CPS-PWM) or more simply PS-PWM. The modulation and output voltage waveforms for N+1 and $2N$+1 levels ($N = 4$) using PS-PWM are given in Figure 9 and Figure 10, respectively.

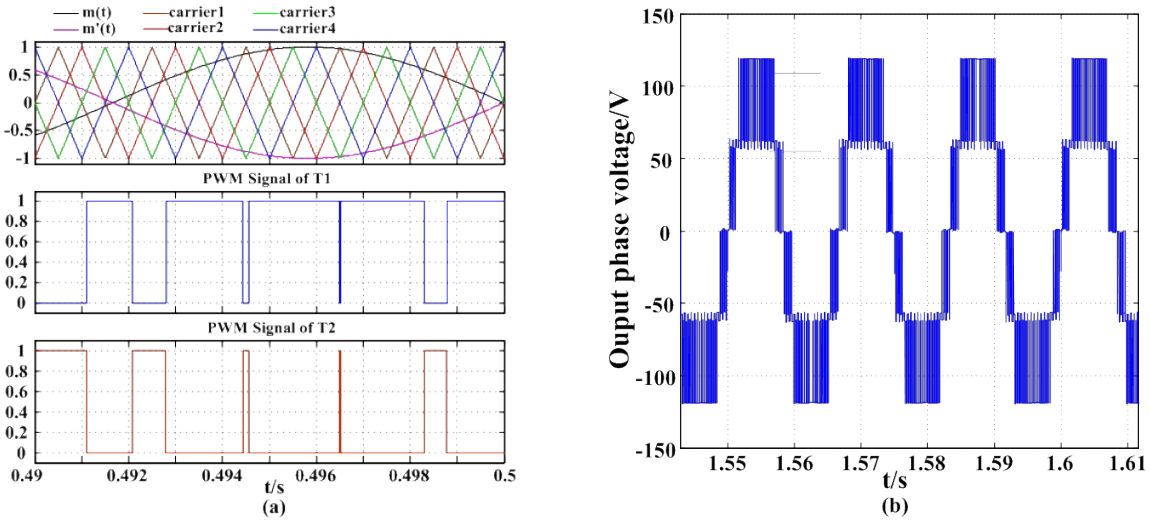

Figure 9. Four cells in series connection with 360°/N phase displacement in the carriers (N+1 PS-PWM): (a) modulation waves and PWM signal for switches of the first SM, (b) simulation waveform of the output phase voltage.

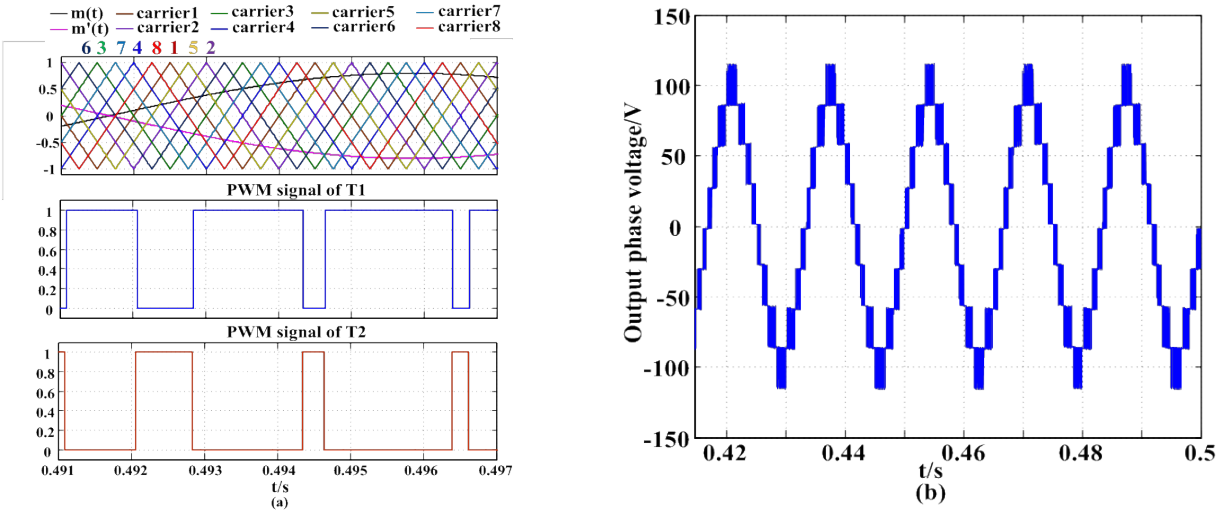

Figure 10. Four cells in series connection with 180°/N phase displacement in the carriers (2N+1 PS-PWM: (a) Modulation waves and PWM signal for switches of the first SM, (b) Simulation waveform of the output phase voltage.

With $N+1$ level modulation scheme (phase shift of $360°/N$ among carriers), N SMs per phase are inserted at all times, leading to a balanced capacitor voltage. In contrast, if $2N+1$ level modulation scheme (phase shift of $180°/N$ among carriers) is used, $N+1$ or $N-1$ SMs will be inserted at certain time, causing issues with the capacitor voltage self-balancing algorithm and requiring additional balancing control. Using PS-PWM modulation algorithm, the effective switching frequency of the load voltage will be much higher than that of each cell (Nf_c for $N+1$ level and $2Nf_c$ for $2N+1$ level, where f_c is the carrier frequency). This property allows low switching frequency of each SM while still obtaining an effectively high switching frequency in the output voltage, thus reducing switching losses. In addition, it enables a high degree of linearity, outstanding control performance, and other advantages.

- **Comparison of PD-PWM and PS-PWM in MMC**

A detailed performance comparison between phase disposition PWM (PD-PWM) and phase shift PWM (PS-PWM) schemes under normal condition, overmodulation, as well as carrier non-synchronization condition can be found in [42]. Typically, 2N+1 level modulation scheme [43] is employed because of its superior performance over N+1 level modulation, e.g. lower output voltage distortion, smaller output filter size, etc.

The THD and capacitor voltage balancing with the PS-PWM modulation and PD-PWM modulation are compared under the same number of switching transitions. More sub-modules per arm introduce high complexity of control implementation. For simplicity and without loss of generality, a system with 4 sub-modules per arm was built in Matlab/Simulink. The rated SM voltage is 1.25 kV. For exclusive modulation scheme comparison, MMC works as an inverter under open-loop condition (with fixed amplitude modulation index of 0.9). To observe the capacitor voltage self-balancing capability with the different modulation schemes, no additional control schemes are adopted to regulate capacitor voltage or circulating current in the simulation.

To make the comparison more persuasive, the carrier frequency of PD-PWM modulation is adjusted to achieve the same number of switch transitions as that of PS-PWM over each fundamental cycle, i.e., f_{sPDPWM} is 4 times of f_{sPSPWM} in this case. Moreover, in order to minimize the effect of capacitor voltage deviation caused by the uneven distribution of switching signals, carrier rotation techniques in [44] are employed. Compared to the carrier rearrangement introduced in [45], triangular carriers are rotated among levels every fundamental period instead of each switching period, contributing to a fairly low complexity in implementation.

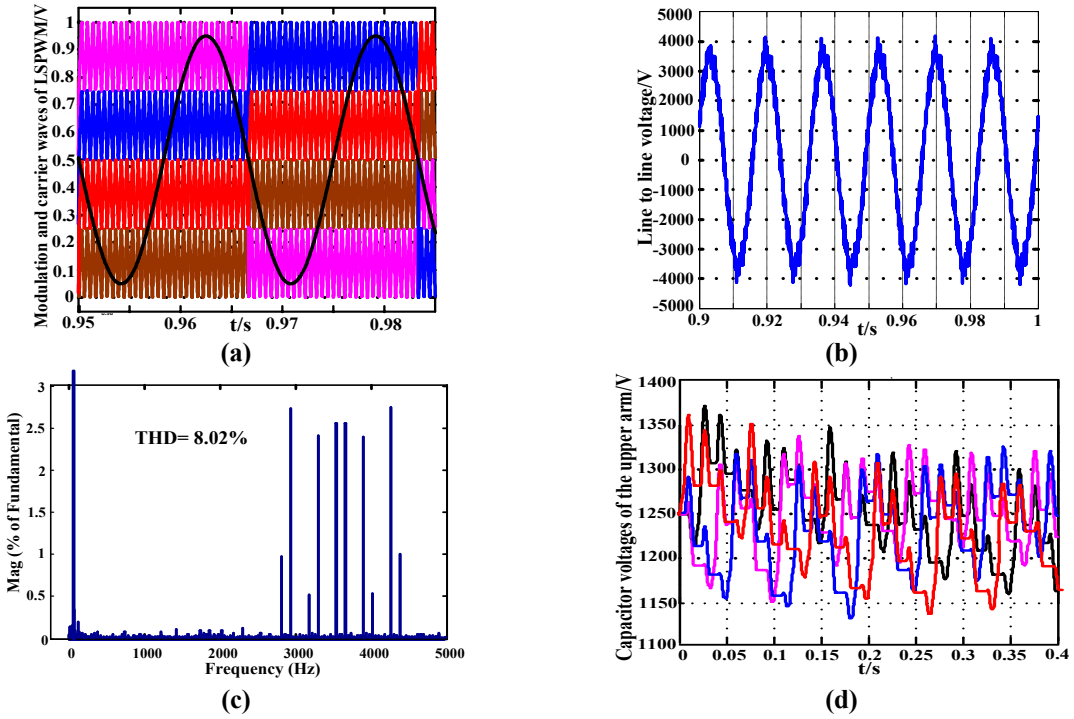

Figure 11. Waveforms with PD-PWM 2N+1 modulation. (a) Target waveform generation. (b) line-to-line voltage. (c) Analytical spectrum of line-to-line voltage. (d) Upper arm individual SM capacitor voltages.

During normal operation: Figure 11 describes the PD-PWM modulation with the given parameters. Carriers move to their next levels at the beginning of each fundamental period, hence it spends N fundamental cycles to complete the rotation loop. The THD of the line-to-line voltage is 8.02%. Although the capacitor voltages do not overlap, and the ripples are higher compared to those with PS-WPM modulation, they are much smaller than the ripples without the carrier rotation scheme.

Figure 12 describes the PS-PWM modulation with the given parameters. To generate the 2N+1 output waveform, a phase shift of 180°/ N is introduced across each carrier, i.e., $\alpha_{i+1}=\alpha_i+90°$ for i =1, 2, …, N-1 and i =N+1, N+2, …, 2N-1, while $\alpha_{j+N} = \alpha_j + 45°$ for j = 1, 2…N, where $\alpha_{i,j}$ represents the initial phase angle of the carrier for the i, j sub-module in each phase. Obtained from FFT analysis, the THD of the line-to-line voltage is 8.14 %, with the most significant harmonic concentrated at 3.6 kHz. The capacitor voltages are well balanced due to the inherent even power distribution among the SMs.

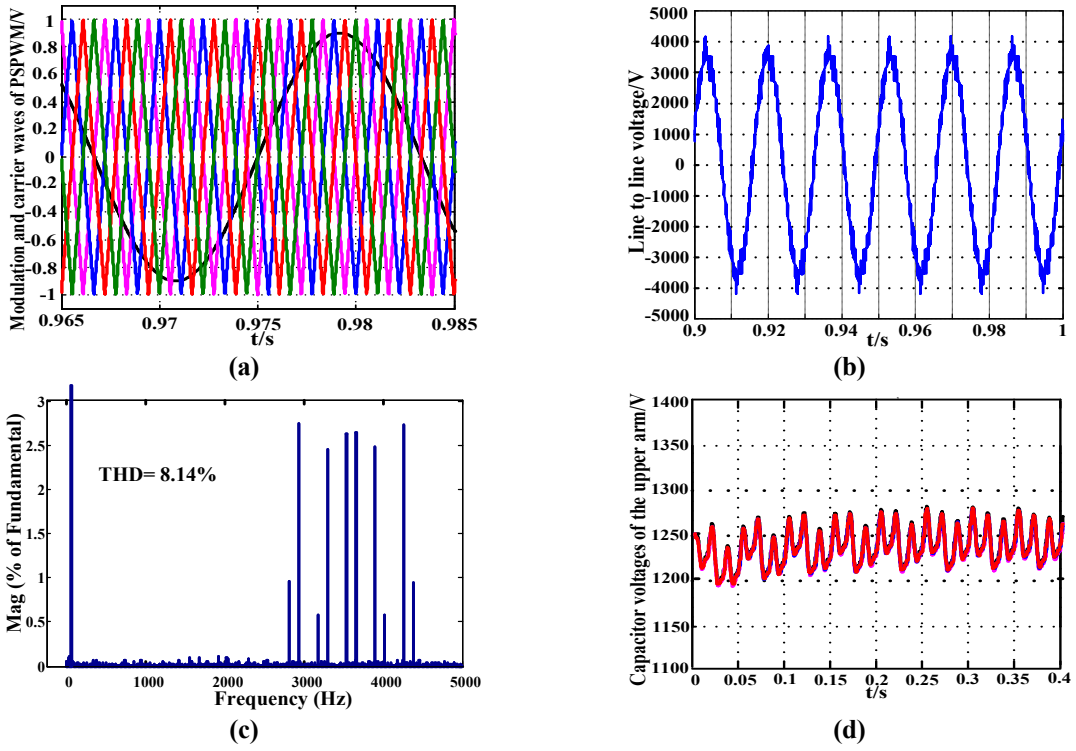

Figure 12. Waveforms with PS-PWM 2N+1 modulation. (a) Target waveform generation. (b) line-to-line voltage. (c) Analytical spectrum of line-to-line voltage. (d) Upper arm individual SM capacitor voltages.

During overmodulation: The case of m_a =1.5 is applied to investigate the overmodulation scenario for the MMC. For the PD-PWM, as shown in Figure 13, although the THD is reduced because of larger fundamental component compared to normal condition, low frequency harmonics, primarily the 5th, 7th, and 11th harmonics, are created because of the nonlinear characteristics. In addition, due to different harmonic cancellation between phases, harmonic power concentrates on new sidebands instead of the second carrier frequency and sidebands.

With the carrier rotation, no switch is kept open or closed all the time, leading to relatively even power distribution among SMs. In spite of larger ripples as well as average voltage variation among SMs, regulation of capacitor voltages is maintained without apparent deviation under over-modulation condition.

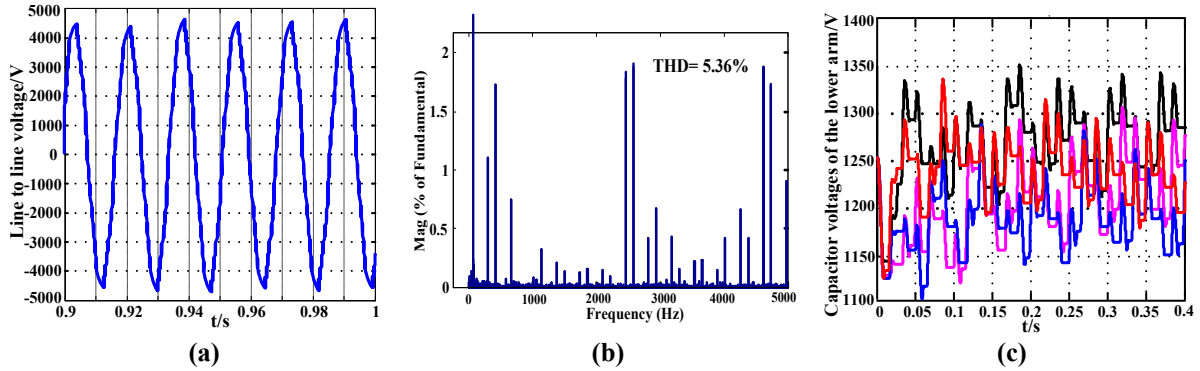

Figure 13. Waveforms with PD-PWM when m_a=1.5. (a) line-to-line voltage. (b) Analytical spectrum of line-to-line voltage. (c) Upper arm individual SM capacitor voltages.

For PS-PWM, as shown in Figure 14, during overmodulation the waveform has the same harmonic distribution but a higher magnitude of sideband components, and a slightly larger THD of line-to-line voltage is achieved. Simulation results show an increasing deviation among capacitor voltages, which indicates the requirement of an additional capacitor voltage balancing control under this condition. During the overmodulation period, according to the gate signal generation, some switches will remain open while the others keep closed, and thus the capacitor of each SM is charged or discharged unevenly, leading to obvious voltage deviation.

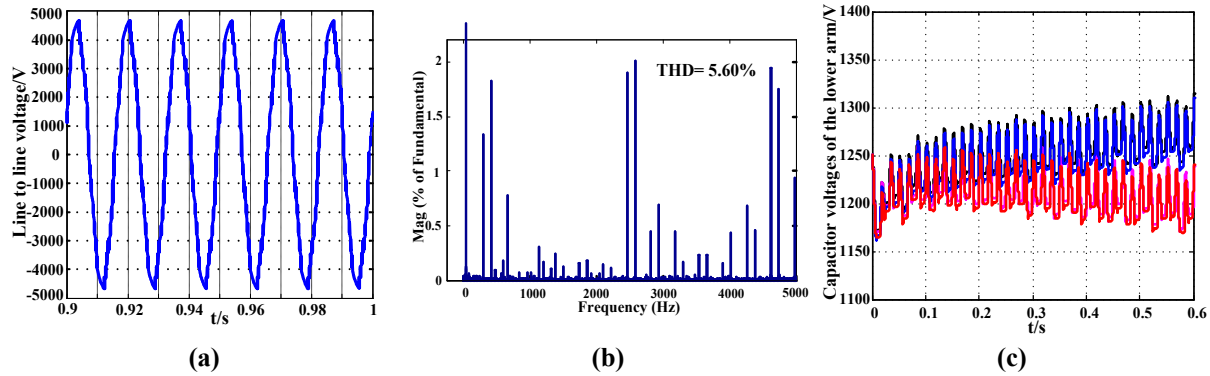

Figure 14. Waveforms with PS-PWM when m_a=1.5. (a) line-to-line voltage. (b) Analytical spectrum of line-to-line voltage. (c) Upper arm individual SM capacitor voltages.

Synchronization errors: It is well known that both PD-PWM and PS-PWM modulation schemes require accurate synchronization among the multiple carriers to achieve optimal harmonic cancellation. However, this requirement is difficult to meet in practice because of unavoidable computational errors, memory limitation, sampling errors and communication delay. Three cases of different synchronization errors are investigated in [42] including: *Case 1*: Phase error between carriers for the upper power bridges and those for the lower bridges; *Case 2*: Phase error among the carriers in the upper or lower arms. *Case 3*: Phase error between three-phase carrier waves. Varying degrees of output THD increase can be observed in each case for both

modulation methods, but an evident deviation of SM capacitor voltage only occurs in Case 2 with PS-PWM.

In conclusion, compared with the PS-PWM strategy, the PD-PWM with rotated carriers has smaller line-to-line voltage distortion under both normal and overmodulation conditions. In addition, higher capacitor voltage self-balancing capability is achieved with the adopted PD-PWM modulation. For both modulation strategies, system performance shows significant degradation under three different non-synchronization cases. With phase error among carriers, besides higher voltage distortion, the capacitor voltage may not converge, and thus deliberate consideration is required in hardware implementation to avoid synchronization failures.

3 Components Design of MMC

3.1 SM Number

The number of SMs in each arm depends on the HVDC voltage level and individual IGBT device voltage. Considering that the maximum arm voltage equals the dc-link voltage V_{dc}, and the SM voltage is V_C which is determined by the rated voltage of IGBT device along with some safety margin (typically at least 25%), the minimum SM number should be

$$N = \frac{V_{dc}}{V_C} \tag{12}$$

Given that the medium voltage SiC MOSFET devices or Si IGBT ratings are in kV level and HVDC rating is typically in hundreds of kV, often several hundred SMs are used for one MMC [46]. Typically, to account for failures within modules, there are generally some redundant levels (additional modules) in each phase leg that can be bypassed so that the converter can continue to work even with the failure of a switch or capacitor in a submodule.

3.2 SM Capacitance

The SM capacitor is a key component in MMC, and a driving factor on the converter size, weight, and cost. The capacitor need of MMC is much higher than that of the 2-level converter; it could be even 10 times higher. So, it is important to select the minimum capacitor size while still satisfying all the criteria. Maximum voltage, voltage ripple and current ripple are three main design criteria for submodule capacitor in MMC [47]. Typically, the maximum voltage and voltage ripple are linked together, as the maximum voltage is the normal capacitor voltage plus voltage ripple. Tang et al. [47] demonstrated that the capacitance needed to satisfy voltage ripple requirements is usually larger than that to satisfy ripple current requirements, which makes the voltage ripple the main design criteria for submodule capacitor.

Based on the operating principles of MMCs, the energy fluctuation of an arm within one fundamental frequency cycle can be obtained by integrating the instantaneous power of the arm between two zero-crossing points. Omitting the overmodulation cases, the arm voltage will keep positive, and the zero-crossing points of instantaneous power correspond to those of the arm current, which can be derived from (1) as

$$x_1, x_2 = \left[\frac{\pi}{2} \pm \arcsin\left(-\frac{m\cos\varphi}{2}\right) - \varphi\right]/\omega \tag{13}$$

where $m = \frac{V_{ac}}{V_{dc}/2}$ is the modulation index, $\cos\varphi$ is the power factor of the connected ac system, and ω is the angular frequency of the connected ac system.

Assuming that an effective SM capacitor voltage balancing strategy is applied, the energy fluctuation of the arm can be evenly distributed in each SM. The SM capacitor energy fluctuation within a fundamental period can be derived as

$$\Delta W_c = \frac{\Delta W_{arm}}{N} = \frac{2}{3}\frac{S}{mN\omega}\left[1 - \left(\frac{m\cos\varphi}{2}\right)^2\right]^{\frac{3}{2}} \tag{14}$$

where ΔW_C is the SM capacitor energy fluctuation, ΔW_{arm} is the arm stack energy fluctuation, S is the rated power of the three-phase MMC. Considering the SM voltage varies around its rated voltage V_C by $\pm\varepsilon$%, the SM energy fluctuation can be expressed as

$$\Delta W_c = \frac{1}{2}C[V_C(1+\varepsilon)]^2 - \frac{1}{2}C[V_C(1-\varepsilon)]^2 = 2\varepsilon C V_C^2 \tag{15}$$

Combining (14) and (15), the SM capacitance can be determined by the operating point of the MMC and the allowed SM capacitor voltage ripple, which can be written as

$$C = \frac{S}{3mN\omega\varepsilon V_C^2}\left[1 - \left(\frac{m\cos\varphi}{2}\right)^2\right]^{\frac{3}{2}} \tag{16}$$

The required SM capacitance can be roughly estimated by (16), ignoring the unbalanced voltage among SMs. However, some studies [48] noted that the unbalance among SMs could be significant enough that it cannot be neglected. The unbalanced voltage of MMC depends on the voltage-balancing control, which essentially manipulates the currents flowing into the different submodule capacitors to achieve balanced voltages, by adjusting the inserting instant and duration for each submodule. An effective voltage-balancing control can result in a smaller unbalanced voltage but at the cost of higher switching frequency, which directly influences the converter efficiency. The design of submodule capacitance and converter switching frequency is interconnected. Hassanpoor et al. [49] evaluated the maximum unbalanced voltage at different switching frequencies through simulation, and Li [50] further derived the analytical relationship between the unbalanced voltage and the switching frequency to more precisely design the submodule capacitance.

3.3 Arm Inductance

The value of the arm inductance should be considered from three perspectives: (a) The arm inductor is a part of the phase inductor between the MMC and the ac system, which affects the power transfer capability and serves as an output filter in normal operation, as well as suppresses the negative sequence current in unbalanced or fault operation. (b) The arm inductor needs to suppress the inner circulating current, and the value of it should avoid resonances with the equivalent capacitance of the SMs in the arm. (c) The arm inductor needs to suppress the SM discharging current when the dc-side short circuit fault happens.

INDUSTRY INSIGHT

For a MMC system, the phase inductance is the combination of the leakage inductance of the transformer and 1/2 of the arm inductance. This phase inductance affects the speed of the ac current control (a phase inductance value near 0.1 p.u. provides a simpler control in most applications [51]) and has an impact on limiting the negative-sequence currents [52]. It also serves as a filter to reduce the harmonic content introduced by the converter. In MMCs for HVDC applications, the high number of submodules leads to a moderate filter requirement, thus, a moderate value of phase inductance [51]. The value of inductance required for harmonic filtering is given in [53] and it corresponds to 0.125 p.u. for the considered case study. The phase inductance also creates an ac voltage drop when transmitting active and reactive power at the point of common coupling (PCC). For a defined ac voltage, if the inductance is too high, the given DC voltage may not be sufficient to modulate the required ac waveform to transmit the desired active and reactive power [51].

In normal operation, the submodule's capacitor is expected to perform as a constant dc voltage source, but as mentioned in (14) and (15), the SM capacitor voltages actually fluctuate due to ac current flowing through the capacitor. For modulation method which assumes a constant dc capacitor voltage, like the direct modulation in [54], the summation of upper and lower arm stack voltages would not be constant, causing the circulating current flowing in the dc loop. This circulating current increases the converter power loss and thus should be limited. Rohner et al. [55] showed that the dominant component of the circulating current is second-order harmonic. When direct modulation is applied without the ac circulating suppressor, a relatively large arm inductance is required to limit the peak of the circulating current and to avoid resonances with the submodules capacitances [56]-[58]. However, when a circulating current suppressor is considered [59], [60], the second-order harmonic current can be effectively limited. As a result, the arm inductance can be significantly reduced and is no longer the primary determining factor in the design of arm inductors. This circulating current suppressor can be either based in software [60] or in hardware, for instance by adding a capacitor between the two arm inductors [61].

During DC fault conditions, the arm inductor limits the di/dt of the fault current, meaning that the inductor can be designed to protect the semiconductors in the submodules [62]. Half-bridge submodules are the most common type of SM employed in HVDC-MMCs. They have a low component count and lower conduction losses than full-bridge submodules, but they lack the ability to stop DC fault currents and the AC breaker is relied upon to stop the current during DC faults. A DC pole-to-pole fault is identified as the most severe external fault in terms of the fault current [63]. Consequently, several papers propose simplified models to calculate the fault currents of an MMC under a DC pole-to-pole short-circuit, which can provide the specifications of the arm inductor. Analytical expressions that describe the fault currents during different stages of the fault are derived in [64]-[66]. Other works employ simplified state-space representations of the MMC and calculate the fault currents numerically [67]-[69]. The aim of both approaches is to calculate the fault currents without needing to rely on time consuming detailed simulations [70]. Usually, the peak current limit of the IGBTs in the submodules before their blocking (turn off) is defined as one of the criteria to choose the arm inductor [71], [72]. Some works consider the peak current of the bypass thyristor [63] and the let-through energy of the lower diode in the submodules [66], [73] to define the arm inductance value, taking into account also the stages after blocking the converter.

Further, in order to reduce the size, weight and cost of magnetic components, coupled inductors can be employed instead of separate ones. Reference [74] applies a single coupled buffer inductor with inductance only to the circulating current. Without inductance to the differential components, harmonics and switching ripples contained in the output current cannot be suppressed, leading to a large total harmonic distortion (THD). This worsens in the case for MMCs with low number of sub-modules and/or non-inductive loads. To suppress the common mode circulating current in the parallel connected converters, an integrated inductor is proposed in [75], which combines the merits of interphase and filter inductors. Both inductances can be adjusted independently and precisely by changing the air gap between the two cores. Reference [76] presents another integrated inductor for differential mode and common mode noise suppression. The current rating is small to keep the toroidal cores from saturation.

4 Control of MMC

Unlike two-level VSCs, MMCs combine a large number of SMs rather than chained IGBTs, which brings superior flexibility and adaptability but also introduces the difficulty of control. For the output current control, techniques have been well established and implemented in the stationary-*abc*, the stationary-*αβ*, and the synchronous-*dq* reference frames [77] for classic two-level or three-level converters, which can be directly applied to the MMC. This section will focus more on the characteristic control in MMC introduced by the modular structure, including the SM voltage balancing control, inner circulating current suppression, and startup schemes.

4.1 SM Voltage Balancing Control

The arm current in an MMC will only flow through the SM capacitor when the upper switch turns on and the SM is inserted. However, as determined by various modulation schemes, the switching state for SMs is different from each other, leading to different charging/discharging times of the SM capacitors and thus voltage deviations. These unbalanced SM capacitor voltages generate output voltage distortion and bring high-voltage stress to SM capacitors, as illustrated in Figure 15. To address this issue, numerous voltage-balancing control schemes have been proposed, and a comprehensive review of SM balancing methods can be found in [78], which classifies the methods into two categories: closed-loop methods and open-loop self-balancing methods.

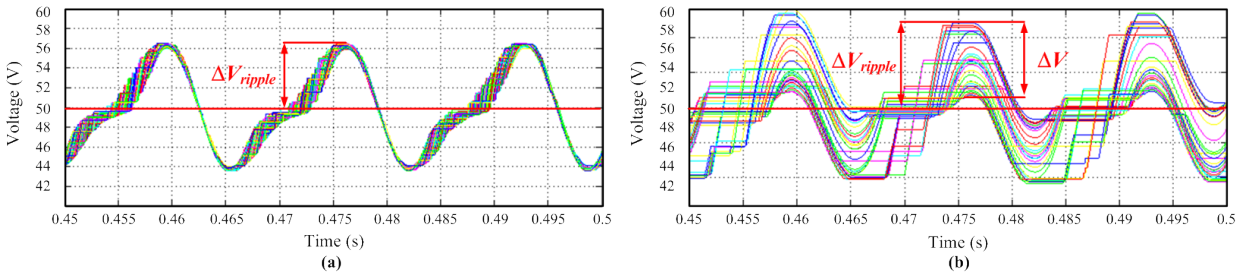

Figure 15. SM capacitor voltages in well and poorly balanced conditions, (a) Well balanced capacitor voltage, (b) Unbalanced capacitor voltage.

4.1.1 Closed-loop SM Balancing Methods

(a) Closed-loop SM balancing in this section indicates that the balancing is achieved by adjusting the SM driving signals based on the real-time feedback of each SM voltage. According to the implementation method of the closed-loop control, it can be categorized into two types of structures including the centralized control shown in (b)

(b) Figure 16(a) and the distributed control shown in (b)

Figure 16(b). The former one uses the central controller of the MMC to sort the SM voltages and assign the driving signals, which demands the coordination of DSP and FPGA to realize complex calculations and high-frequency communication. The latter one relies on the local controller of each SM to follow the voltage reference, which relieves the control burden of the central controller and enables to decrease the communication frequency between the central and local controllers.

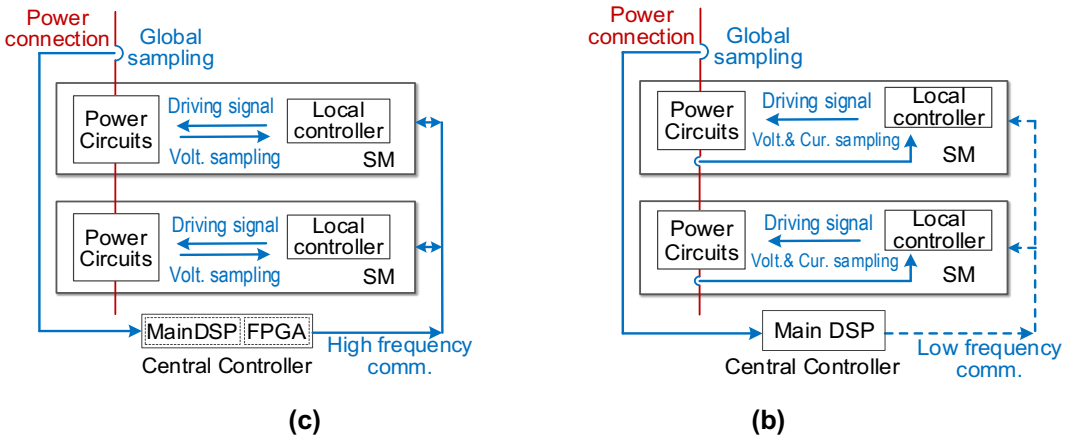

Figure 16. Two types of closed-loop SM voltage balancing control structures, (a) Centralized control structure, (b) Distributed control structure.

- **Centralized Closed-loop SM Balancing Methods**

Figure 17 illustrates the classic closed-loop centralized balancing method [79] that is widely applied in MMCs. SM balancing is achieved by sampling and sorting all the real-time SM voltages in the central controller, then assigning the switching patterns to charge those SMs with lower voltage and discharge the SMs with higher voltage. Specifically, if the arm current is charging the capacitors, the SMs with the lowest capacitor voltages will be inserted. On the other hand, if the arm current is discharging the capacitors, the SMs with the highest capacitor voltages will be inserted. With this algorithm, the SM capacitor voltages can be well balanced. Here, the total SMs that need to be inserted can be calculated based on different modulation schemes introduced earlier.

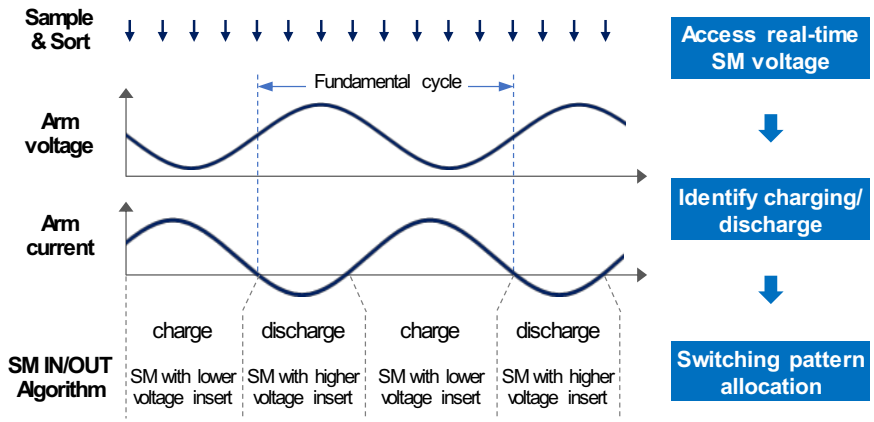

Figure 17. Classic closed-loop SM voltage balancing method for MMCs under grid frequency operation.

This classic SM balancing method can be generalized as three steps including accessing real-time SM voltages, identifying charging/discharging capability of the switching patterns, and switching pattern allocation. Many methods have been proposed to improve these three steps aiming on higher converter switching efficiency, lower SM voltage ripple, less complexity, lower implementation costs, wider adaptability, and many other purposes, which are shown in Table I.

- **Distributed Closed-loop SM Balancing Methods**

(d) The distributed SM voltage balancing methods are generally combined with the PWM modulation by adding an adjustable DC component to the modulation wave of each SM based on its voltage deviation. Then the SMs will track the same reference capacitor voltage to achieve the balancing [109]-[111]. Compared with the centralized SM voltage control in (b) (e) Figure 16(a), the control structure shown in (b)

Figure 16(b) illustrates that the distributed balancing control is achieved in the local controller of each SM. This can help to avoid the sorting process, mitigate the high-frequency unidirectional data transmission, and share the control burden of the central controller. Further, the distributed balancing improves the modularity and expansibility of the MMC. However, it is analyzed in [112] that the local controller clock discrepancy and asynchrony could result in the increase of output THD and the saturation of balancing controller. And the communication adaptability considering both the normal operation and the fault response is another main concern for the distributed balancing control structure.

Table I – Comparison of Closed-loop Centralized SM Voltage Balancing Methods in MMCs

Steps	Methods	Merits	Demerits
SM real-time voltage obtain	Real-time SM voltage sampling [79]	• Accurate data • Wide adaptability for different topologies and operating conditions	• High hardware costs • High frequency data transfer
	Model-based estimation [80]-[87]	• Reduced number of sensors	• High complexity, limited application with fewer SMs • Rely on accurate modeling & sampling • Relatively large error in transient process
Charging/ discharging identification	Real-time arm current sampling [79]	• Wide adaptability for grid frequency operation	• Current sensor needed in each arm
	Model-based arm current direction [88], [89]	• Eliminate arm current sampling	• Phase delay, sampling noise sensitive • High complexity considering digital filter demanded
	Offline net-charge change prediction [90]-[93]	• Reduced sampling costs • Reduced real-time calculation burden	• Specified for each modulation • Less reliable in dynamic conditions
Switching pattern allocation	Reverse correspondence of SM voltages and switching pattern charging capability [79]	• Wide adaptability	• High SM switching frequency • High complexity for sorting
	Non-global sorting and non-global pattern update [94]-[98]	• Reduced control burden • Reduced SM switching frequency	• Relatively high SM ripple
	Variable frequency switching [99], [100]	• Reduced SM capacitor ripple • Reduced capacitor volume	• Most methods focus on single operating condition • Increased control burden
	Optimization of sorting process [101], [102]	• Reduced complexity of sorting process	• Trade-off between calculation speed and register occupation
	Model predictive control [103]-[108]	• Realize multiple objectives together	• High computational burden • Difficulty in multi-objective weighting factor design • Rely on accurate modeling

4.1.2 Open-loop Self-balancing Methods

Self-balancing indicates that the SM voltages are naturally self-regulated at the balancing state without voltage feedback and real-time switching patterns allocation, which is an ideal characteristic that can significantly reduce the demand of high-speed sampling and bi-directional communication, relieve the control burden for online switching pattern allocation, reduce the implementation costs, and increase system reliability [113]. According to the different balancing principles, three kinds of self-balancing methods can be summarized as follows.

Auxiliary Balancing Loop Construction: By adding the auxiliary balancing circuits shown in Figure 18, a direct energy transfer loop between adjacent SMs is built allowing the capacitors to operate in a parallel state [114]. The charge will automatically transfer from the SM capacitor with higher voltage to that with lower voltage resulting in self-balancing. The auxiliary circuit mainly includes a diode or an IGBT to passively or actively control the balancing current direction, as well as the passive components to limit the balancing current amplitude and construct the soft-switching conditions.

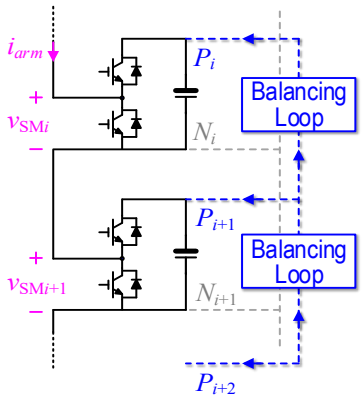

Figure 18. Auxiliary circuits based open-loop balancing method.

Neutral Pattern Set Rotation: The SM capacitor voltage or charge change can be predicted based on the steady-state operation. Further, it is proven in [115], [116] that the summation of all the SM capacitors' charge change equals zero in an ac cycle. Therefore, a set of n switching patterns can be rotated among n SMs in one stack, and the SM voltage should return to its initial value after finishing the rotation within n ac cycles, which guarantees SM voltage balancing [116], [117]. Since the charging capability of the switching pattern is predicted before the pattern sequence design, these kind of methods usually can help to reduce the SM capacitor voltage ripple [117], [118] or eliminate the selected harmonics of the output voltage [116].

Full-rank Switching Matrix: When the submodules are inserted in and bypassed from the circuit with a time-varying switching function, a series of voltage equations for SM voltages can be written. The switching matrix can be extracted from the series of KVL equations, and the full-rank switching matrix indicates that the number of linearly independent constraints provided by the set of switching actions is equal to the SM number, which guarantees the inherent SM balancing. Inspired by the self-balancing of clamping capacitors in multilevel switch capacitor converters [119], the Y-matrix modulation is proposed in [120], [121] that designs a full-rank switching matrix for the MMC and proves its full-rank feature. Ref. [122] proves that for arbitrary n, $\boldsymbol{Y}$ is a full-rank matrix, and [120]-[122] explains the principle of steady-state SM balancing under the full-rank switching matrix, and [123] further analyzes the SM voltage ripple and circulating current under the Y-matrix modulation in steady-state operation.

4.2 Circulating Current Suppression

According to Eq.(4), if the SM capacitor voltage equals to V_{dc}/N (V_{dc} is dc link voltage, and N is SM number per arm) all the time, no circulating current will be generated. However, in a real MMC converter, low-frequency voltage ripple exists due to alternating arm current. The

circulating current will not affect the ac output voltage and currents. However, if it is not effectively suppressed, it increases the peak and RMS values of the arm currents, leading to high power losses and large SM capacitor voltage ripple. Under normal operation conditions, the dominant circulating current is a negative sequence with second-order harmonic frequency [124], [125].

Although the circulating current can be effectively mitigated by increasing the arm inductance, active suppression control schemes are preferred for lower converter volume and cost. A comparative experimental result with and without circulating current suppression control is given in Figure 19 as an example.

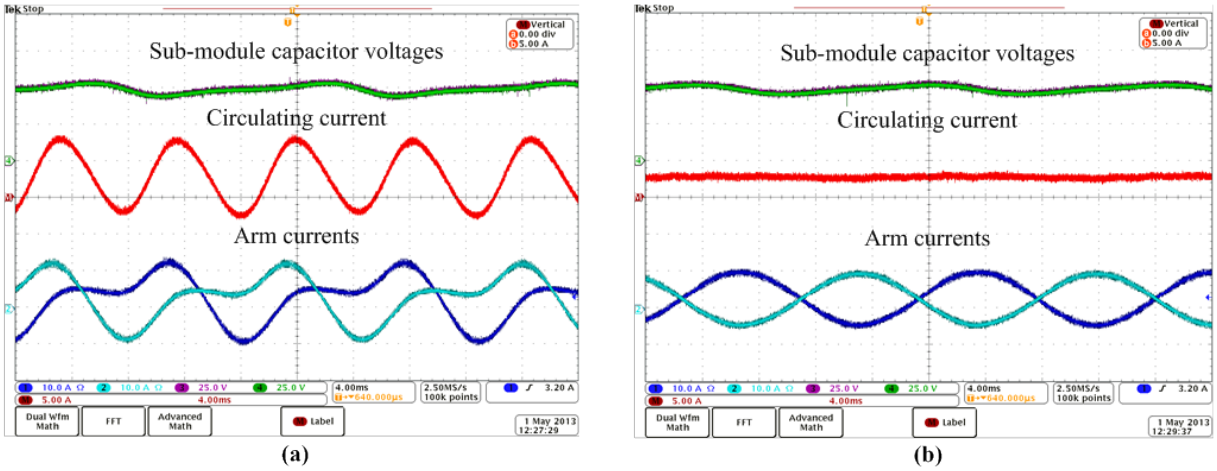

Figure 19. Experimental results showing the effectiveness of active suppression control schemes (a) circulating current suppressing control disabled, (b) circulating current suppressing control enabled.

In [126] and [127], the open-loop methods are presented for the circulating current control and harmonic suppression. These methods are very sensitive to parameter variation. Instead, the synchronous-*dq* reference frame-based control approach is widely used for the complete elimination of circulating current as shown in Fig. 12. In this approach, the circulating currents in the stationary-*abc* frame are transformed into the synchronous-*dq* frame rotating at twice the fundamental frequency. In the synchronous-*dq* frame, the double line frequency circulating current component becomes a dc signal. The dc signals are easily controlled using a simple PI regulator [128], [129].

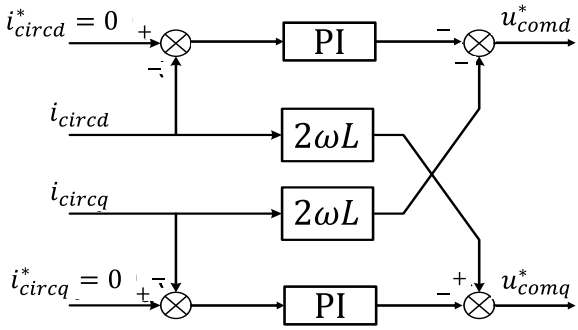

Figure 20. Synchronous-*dq* frame-based circulating current suppression control.

The resonant regulators can be also employed to control the circulating current in the stationary-*abc* frame. In this approach, the resonant regulators are designed to eliminate the specific dominant harmonic frequency component such as second- and fourth-order harmonic components from the circulating currents [130]-[132]. In [133], a parallel combination of repetitive and PI regulator is used to eliminate multiple harmonics in the circulating currents. The parallel combination imposes a limitation on the PI regulator performance, and it complicates the design of the repetitive controller. To overcome these problems, a cascade structure of repetitive controller and a PI regulator is presented in [134]. The repetitive controller improves the bandwidth and dynamic performance of the circulating current control and the THD of the output voltage.

During unbalanced operating conditions, the circulating current consists of positive and zero sequence components besides the negative sequence components at twice the line frequency [135]. The positive and negative sequence components flow through the converter legs. On the contrary, the zero sequence circulating current flows through the dc-bus and the converter legs, leading to a ripple in the dc-bus power. These ripples appear in the dc-bus current, considering that the dc-bus voltage is stiff [135]. The dc-bus current ripple increases the SM capacitor voltage ripple and the magnitude of arm current, which has a cascade effect on the device voltage stress and the conduction losses.

In [135], the proportional integral resonant regulator is employed to control the positive, negative, and zero sequence circulating currents. In [136], the proportional resonant (PR) regulator based on the instantaneous power theory is designed to suppress the zero sequence circulating currents. Thereby, the power fluctuations on the dc side are minimized. In [137], the suppression of the circulating currents in the stationary-$\alpha\beta 0$ frame is discussed. In this approach, the high-pass filter is used to extract the double line frequency component from the circulating currents, which affects the dynamic performance of the controller. A nonideal PR regulator is presented to adapt the grid frequency variation and to minimize the circulating current during unbalanced conditions [138]. In [139], the circulating currents are controlled using a PR regulator, where the PR regulator is designed to control the fundamental and double line frequency components.

Alternatively, the circulating currents are separated into the positive, negative, and zero sequence components in the synchronous-$dq0$ frame and are controlled using a simple PI regulator [140]. In [141], the decoupled double synchronous-$dq0$ frame-based current control is presented to control the sum and the differential energy of each converter leg. The stationary-*abc* frame-based control method is presented in [142], where the combination of the PI regulator and vector PI regulator is used in the current control. On the other hand, the dc-bus current or SM capacitor voltage ripple is directly controlled using a PR regulator. Therefore, the magnitude of zero sequence circulating current is minimized [143]. This controller generates a zero-sequence voltage command, which is added to the reference modulation signals. The performance of classical control methods is greatly limited by the parameters of the current controller, switching frequency, and the type of PWM scheme.

4.3 Startup Scheme of MMC

Different from two-level converters, distributed SM capacitors induce a more complicated startup process and the distinct behaviors of an MMC under different operation conditions. In order to ensure smooth and fast energization, deliberate startup schemes are crucial in an MMC-based HVDC system.

4.3.1 Startup with External DC Source

A dc circuit breaker and an external dc source with its voltage equal to the nominal voltage of each submodule's (SM) capacitor are utilized in [126] and [145] to avoid large inrush current in a MMC inverter during the pre-charge process. In spite of its easy implementation, this solution leads to additional costs, especially in high power applications. Also, because of the nonzero voltage ramp time and impedance of a non-ideal dc voltage source, there are substantive requirements for the charging time and time interval between charging pulses. To deal with this issue, a charging circuit that consists of an auxiliary dc source and two thyristors for each submodule is proposed in [146]. By triggering the thyristors synchronously, all SM capacitors can be charged together, thus accelerating the startup procedure. Nevertheless, it still causes high control complexity and additional cost to the system.

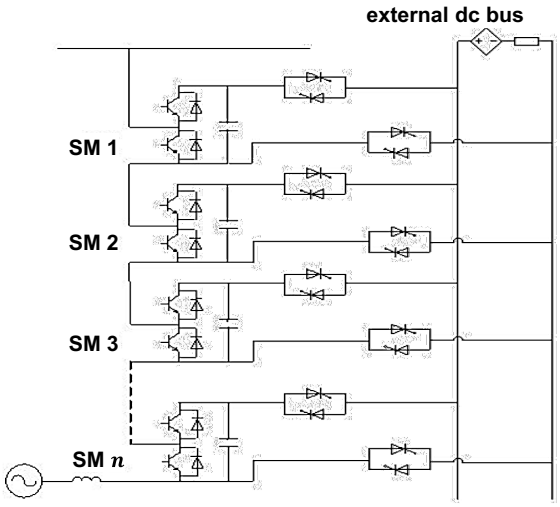

Figure 21. Precharge circuits proposed in [146].

4.3.2 Passive Startup with DC-Link Voltage and Inrush Current Limiter

As a more cost-effective way, the main dc voltage is used in [147] to charge the capacitors. However, an additional inrush arm current limiting resistor is connected in series with the SMs in each arm and should be bypassed after the charging process. With inrush current limiting resistor in the dc bus, a grouping sequentially controlled charge (GSCC) method is proposed in [148] for a three-phase clamp double submodule (CDSM) MMC. Despite its easy implementation, the group number needs to be carefully selected, and deviation among the capacitor voltages due to capacitance tolerance becomes a concern. Similar to CDSM MMC, a group charging scheme is applied to a half bridge MMC in [149] by charging upper and lower arms separately. However, the injected passive resistance and associated bypass switches also lead to additional cost.

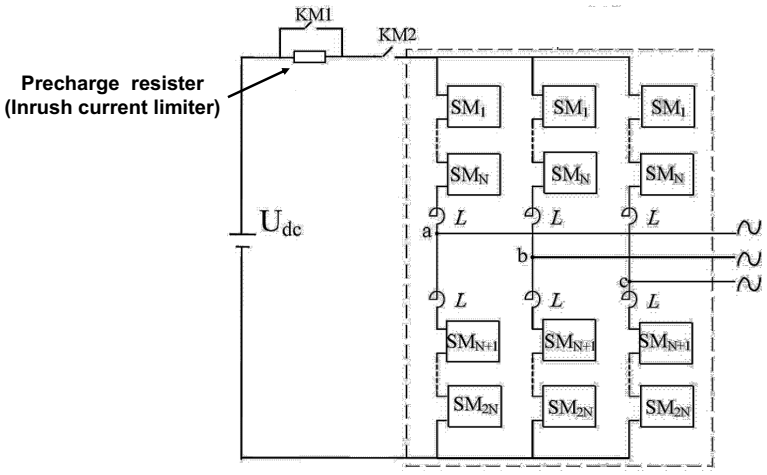

Figure 22. Precharge circuits with inrush current limiter [149].

4.3.3 Analyses of Uncontrolled Pre-charge Process

This part briefly introduces the charging loops of an MMC rectifier and an MMC inverter during an uncontrolled precharge stage, as illustrated in Figure 23. It clarifies the necessity of an active charging current control in the MMC inverter.

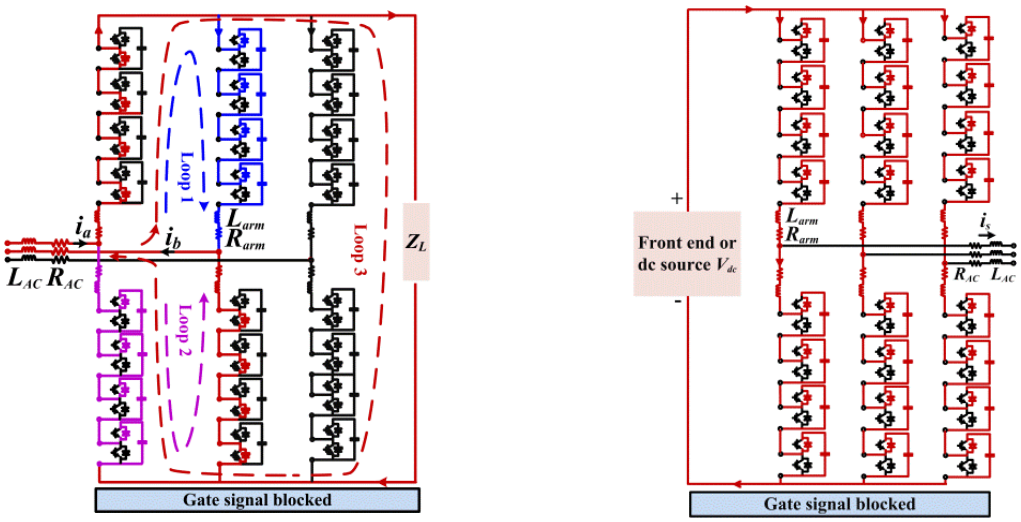

Figure 23. Charging loops during uncontrolled pre-charge stage.
(a) between phase A and B in a MMC rectifier when i_a>0, i_b<0, (b) in a MMC inverter[156].

- **Uncontrolled Pre-charge Process of a MMC Rectifier**

Considering different phase current directions, one of the possible capacitor charging loops between phase A and B during the uncontrolled pre-charge stage ($N = 4$) is shown in Figure 23(a), with conducting devices highlighted by different colors. Among the denoted three loops, current in loop 1 and loop 2 charge the upper and lower arm capacitors respectively, while loop 3 only supplies current for the passive load. In most applications, the load impedance in loop 3 is much higher than the equivalent impedance in loop 1 and loop 2, and thus the phase current will charge the SM capacitors first until the sum of their voltages reaches the peak value of the line to

line ac voltage. Then, loop 1 and loop 2 are blocked and the phase current starts to flow through the load.

As illustrated in Figure 23(a), with a positive phase current i_j (j = a, b, c) (defined as flowing from ac side to dc side), capacitors in the upper arm of the phase are bypassed, while those in the lower arm get charged. On the contrary, with a negative phase current, capacitors in the upper arm are charged and those in the lower arm are bypassed. This process is valid for all combinations of the three phase currents. For example, if $i_a > 0$, $i_b < 0$, $i_c > 0$, i_a and i_c will charge all upper arm capacitors in phase B together and charge their own lower arm capacitors separately. Working as a diode rectifier, at the end of this uncontrolled pre-charge period, the average capacitor voltage of all SM capacitors will reach $2.34V_{ph} / N$ with heavy load or $\sqrt{6}V_{ph} / N$ with no load (V_{ph} is the RMS value of the phase voltage).

If N + 1 level modulation schemes such as phase shift PWM (PS-PWM), level shift PWM (LS-PWM), nearest level control (NLC), etc., are adopted [150], N SM capacitors (with a voltage of V_c for each SM) in each phase will be inserted during normal operation. Meanwhile, according to the above analysis, at the end of the uncontrolled pre-charge period, the dc voltage can be built to NV_c. Consequently, the difference between dc voltage and the inserted SM capacitor voltage is zero ($Nv_c(t) = v_{dc}(t)$), and rated capacitor voltage is not necessary before dc voltage regulation is activated. However, the inrush arm current still exists because of the difference between the peak value of line-to-line voltage and dc voltage, especially when the rectifier is heavily loaded.

- **Uncontrolled Pre-charge Process of a MMC Inverter**

In a MMC inverter, all capacitors will be inserted into the charging loop during the pre-charge period, as shown in Figure 23(b), and the conducting devices are highlighted in red. Being charged synchronously by the dc source, the capacitor voltage is $V_{dc} / 2N$ when this stage ends. The charging current flows only between dc voltage and each arm, and no phase current is generated.

At the end of the uncontrolled pre-charge period, the total equivalent capacitor voltage is $V_{dc} / 2$ assuming N SMs are inserted in each phase (no redundant SMs). Therefore, the other $V_{dc} / 2$, i.e., the difference between the equivalent capacitor voltage and constant dc bus voltage, will apply on the arm inductors as well as their ESRs, leading to a significant inrush current in the charging loops (even higher with more redundant SMs). Therefore, in a MMC inverter, dc loop resistors or fully charged capacitors are necessary before normal operation (power or current control) starts.

4.3.4 Active Startup with Charging Current Control

After the uncontrolled pre-charge period, reference [151] presents an active capacitor charging scheme for a MMC inverter. This scheme helps to establish the capacitor voltages from $V_{dc} / 2N$ (V_{dc} represents the rated dc voltage; N is submodule number per arm) to V_{dc} / N by gradually decreasing the number of inserted SMs from $2N$ to N in each phase-leg. Nonetheless, the working state of submodules in this method should be frequently swapped to maintain balanced capacitor voltages, making its implementation quite complicated, especially in three phase systems with a large number of SMs.

Different from the "open loop" charging strategy, reference [152] proposes a closed loop pre-charge control by regulating a constant charging current during both dc-side and ac-side startup process. SM capacitors can be linearly charged through this method, independent of SM numbers. However, this method requires complex and specially designed capacitor balancing as well as reference generation algorithms, and demands a fast transition between startup and normal operation to avoid capacitors over-charging.

The averaging capacitor voltage control proposed in [153] is utilized in [154] to gradually increase capacitor voltage during startup (self-start) and guarantee an average capacitor voltage of V_{dc} / N during the normal conditions. Nevertheless, the modelling and design of the averaging capacitor voltage control are still missing, which may cause system instability during the variation of operation conditions, control parameters, and system parameters. Additionally, the dynamic performance is not evaluated and unable to be predicted without a valid startup model.

The energy-based control is used in [155] for a desirable startup process of MMC. As a comprehensive control scheme, this control scheme is capable of controlling both the total and differential energy stored in the upper and lower arm capacitors. By properly regulating the arm energies, a gradual and symmetrical capacitor charging is achieved during startup process. However, because of the cascaded control diagrams, its implementation is fairly complicated.

Furthering the research efforts, reference [156] presents a detailed design procedure of the capacitor charging control with desirable steady-state and dynamic performance. To achieve this goal, a small-signal model of the capacitor voltage and the circulating current loops during startup is first derived according to the unique capacitor charging loops and operation conditions, and then, the detailed controller design considerations are presented based on the derived model. Furthermore, the limiting factor of the dynamic response of the averaging capacitor voltage control is identified. It is shown that the resonance between the arm inductance and the SM capacitors will constrain the overall bandwidth of a capacitor voltage charging loop, leading to an unsatisfactory dynamic response. To address this issue, a capacitor voltage feedforward control is proposed, which can operate together with the averaging control to achieve a fast dynamic response without compromising the system stability margin and the implementation complexity.

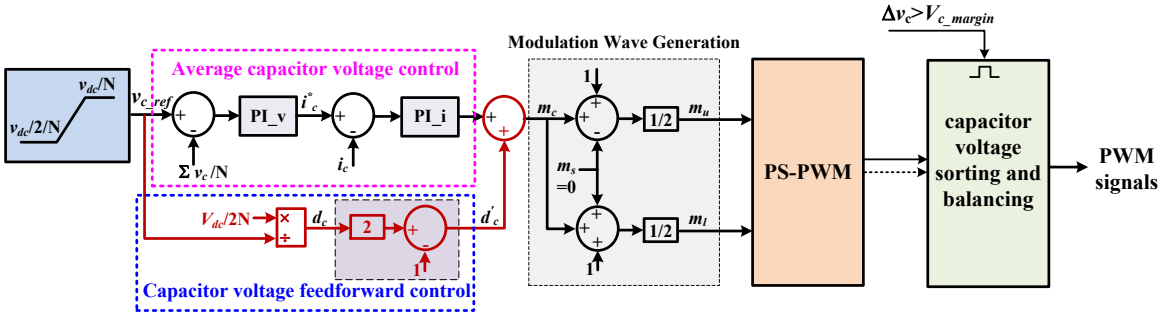

Figure 24. The active capacitor charging control proposed in [156].

5 Advantages and Disadvantages of MMC in HVDC

5.1 Advantages

The series-connected SM configuration in MMCs eliminates the need of direct series connection of devices as that in two- and three-level converters, which significantly reduced the difficulty of implementation. Further, with a MMC as the HVDC interface, there will be higher quality ac voltage produced by the converter with increasing number of levels. With a higher number of SMs in each arm, the output phase voltage of MMC becomes much more sinusoidal (Figure 25(c)), which enables smaller ac filters and compact converter footprint.

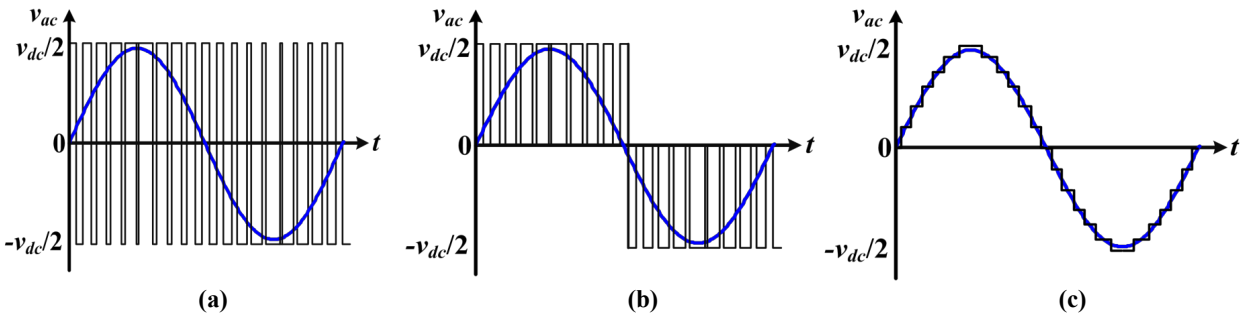

Figure 25. Output ac voltage of a (a) two-level converter, (b) three-level converter, and (c) MMC.

MMC used as a HVDC interface typically has low switching frequency and high efficiency. The series connection of N SMs per arm can achieve an equivalent switching frequency of Nf_c (where f_c represents carrier frequency of each device) in the output voltage. In practical applications, the average device switching frequency is generally below 200 Hz. Consequently, state-of-the-art MMC-HVDC has overall losses of ~1%, which is close to that of LCC.

The MMC has lower high-frequency noise due to reduced *dv/dt* and *di/dt* with the lower voltage steps in the switching ac waveform. It also has modular design and inherent redundancy. This modular design of MMC contributes to lower cost, shorter manufacturing as well as maintenance period, and high extensibility for higher voltage and power applications. Furthermore, the HVDC interface is reliable because failed SMs can be easily replaced by redundant ones [157].

INDUSTRY INSIGHT

Several companies such as GE, Hitachi, and Siemens use the MMC topology in their HVDC interfaces for VSC-HVDC as well as for other flexible ac transmission system (FACTS) products such as STATCOMs (static var compensator). A comparison has been done between (1) a LCC-HVDC, (2) a two-level VSC-HVDC, and (3) a half-bridge based MMC-HVDC for site footprint, building area, and building volumes as shown in Table II where the LCC-HVDC Grita project is the baseline (100% reference).

Table II – Comparison of site areas among LCC and two-level VSC- and MMC-based HVDC systems [158]

Application	Site footprint	Site area (%)	Max building height (%)	Converter building footprint	Converter building area (%)	Converter building volume (%)
LCC-HVDC (reference)	225 m × 120 m	27,000 m^2 (100%)	20 m (100%)	35 m × 20 m	700 m^2 (100%)	14,000 m^2 (100%)
Two-level VSC	180 m × 115 m	20,700 m^2 (77%)	24 m (120%)	38 m × 35 m	1330 m^2 (190%)	25,000 m^2 (179%)
Half-bridge MMC-HVDC	165 m × 95 m	15,675 m^2 (58%)	15 m (75%)	70 m × 45 m	2730 m^2 (390%)	29,500 m^2 (211%)

This comparison is made for comparable power and voltage ratings: for LCC-HVDC (Grita project, 500 MW and 400 kV), two-level VSC-HVDC (500 MW and 400 kV), and half-bridge MMC-HVDC (EWIC project, 500 MW and ± 200 kV) [158]. Different from LCC-HVDC, the converter reactors and dc yard equipment in VSC-HVDC are mounted in converter buildings, which provide more convenient maintenance, improved personnel safety, lower high-frequency emissions and acoustic noise, and protection of equipment from adverse weather. Without the requirement for reactive power compensation, the overall site area for two-level VSC-HVDC is 77% of that for LCC-HVDC, despite its higher converter building footprint, height, and volume. By adopting MMC, the site area is further reduced to only 58% of the reference value, and lower building height is achieved because of a decreased internal suspension height of converter valves. The overall site area reduction of MMC-HVDC supplies a significant benefit, especially for locations with restricted available area and/or high land price.

5.2 Disadvantages

One disadvantage of the MMC is to meet the requirement for capacitor voltage ripple, C_{sub}/N should be constant, which makes the power stage dimensioning quite difficult, especially for a MMC with numerous SMs per arm. Each SM requires a gate drive, protection, capacitor voltage monitoring, and associated communication resources, which greatly increase the cost of the system.

The control scheme for an MMC is much more complicated than that in a two-level converter. In addition to the generic higher-level control to meet the overall system behavior requirements (V_{dc}-Q, P-Q, etc.), capacitor voltage-balancing control and circulating current suppression control are indispensable in a MMC for desirable operation performance, and to lower the voltage and current stress applied on semiconductor devices and passive components. Because of the demand for accurate capacitor voltage and arm current detection and/or high-speed communication, these control schemes will introduce considerable expense and computing burden to the control unit.

6 Summary

In this course module, an overview of the Modular Multilevel Converter (MMC) is provided introducing its operating principles, main component design, control strategies, and pros and

cons in HVDC systems. MMCs feature for its modular structure using SM stacks instead of the series-connected IGBTs for enabling low-voltage power devices in high-voltage applications. The equivalent circuit is derived to reveal the relationship between the differential-mode arm voltage and output current, as well as the common-mode voltage and inner circulating current. Various multilevel modulation methods are demonstrated, including fundamental frequency switching methods and carrier-based PWM techniques. The design of MMC components such as SM number, SM capacitance, and arm inductance is then addressed. Characteristic controls in MMC including those inherent by its modular structure are covered, including the SM voltage balancing control, inner circulating current suppression, and startup schemes. Lastly, advantages and disadvantages of MMC in HVDC systems are discussed.

Problems

Problem 1: Describe the advantages and disadvantages of multilevel converters compared to two-level converters, especially as it relates to application in HVDC interface converters.

Solution:
Multilevel converters have the following advantages compared to two-level converters:

(1) Lower dV/dt change rate resulting in less EMI
(2) Output voltage waveform more closely is a sinewave (typically, THD < 1%) even with little filtering
(3) Redundant levels allow for continuous operation even with failure in a submodule

The disadvantages of a multilevel converter compared to a two-level converter include:

(1) Having many submodules in a multilevel converter increases probability of a failure in a module.
(2) There will be a need for many control, gate drive, and auxiliary power supplies for submodules in a multilevel converter.

Problem 2: Figure 2 depicts circuit schematics for an individual half-bridge MMC module and its associated switching states. For each figure subfigure, describe which switches are ON, which devices and are conducting current, and if the capacitor is being charged, discharged, or is bypassed.

Solution:
In Figure 2(a), the left figure depicts startup or protection state where both IGBTs (T1 and T2) are turned off. If current is flowing into the midpoint of the module (node between T1 and T2), then it flows through the antiparallel diode D1 of T1 and into the positive side of the capacitor, charging it. If instead current is flowing out from the module at the midpoint, then it enters at the negative dc bus of the module and flows through the antiparallel diode D2 of IGBT T2.

In Figure 2(b) for the module insert state, IGBT T1 is ON and IGBT T2 is OFF. If current is flowing into the midpoint of the module, then it flows through the antiparallel diode D1 of T1 and into the positive side of the capacitor, charging it. If instead current is flowing out from the module at the midpoint, then the current enters the negative dc bus of the module and flow through the capacitor and through IGBT T1, discharging the capacitor.

In Figure 2(c) for the module bypass state, IGBT T2 is ON and IGBT T1 is OFF. If current is flowing into the midpoint of the module, then it flows through IGBT T2 and out the negative dc bus, effectively bypassing the capacitor. If current is flowing the other direction, it enters the negative dc bus and then flows through the antiparallel diode D2 and exits the midpoint.

Problem 3: An MMC contains 100 submodules in the upper arm and another 100 modules in the lower arm. The rated voltage of the dc capacitor in each submodule is 2 kV after including a safety margin. For the IGBTs and diodes, 3.3 kV devices are used. (a) What is the maximum dc link voltage that this MMC could support? (b) If at an instant of time it is desired for one leg of the MMC inverter to produce an output voltage of +80 kV with respect to ground, how many submodules are inserted from the upper arm and the lower arm of that submodule? (c) If at an instant of time an inverter ac voltage of -40 kV is desired, how many submodules are inserted from each arm?

Solution:
(a) The 100 SMs with 2 kV capacitors can provide a voltage of 200 kV for the upper arm, and the lower arm with 100 SMs and 2 kV capacitors can also provide a voltage of 200 kV. Thus, the leg can support an HVDC dc-link voltage of 200 kV.
(b) The output voltage for any phase *j* as shown in Figure 3 is given by the two equations:

$$v_j = \frac{V_{dc}}{2} - u_{pj}$$

$$v_j = \frac{-V_{dc}}{2} + u_{nj}$$

To produce an output voltage of +80 kV, 10 of the upper submodules (2 kV each) are inserted. Conversely, for the lower submodules, 90 of the lower submodules are inserted.

$$v_j = \frac{V_{dc}}{2} - u_{pj} = 100\ \text{kV} - 10 \cdot 2\text{kV} = 80\ \text{kV}$$

$$v_j = \frac{-V_{dc}}{2} + u_{nj} = -100\ \text{kV} + 90 \cdot 2\text{kV} = 80\ \text{kV}$$

(c) To produce -40 kV output voltage, 30 submodules of the lower arm are inserted and 70 of the upper arm. Note that there are always 100 modules inserted and 100 not (the sum of the lower arm and upper arm inserted modules equals the number of modules in an arm).

$$v_j = \frac{V_{dc}}{2} - u_{pj} = 100\ \text{kV} - 70 \cdot 2\text{kV} = -40\ \text{kV}$$

$$v_j = \frac{-V_{dc}}{2} + u_{nj} = -100\ \text{kV} + 30 \cdot 2\text{kV} = -40\ \text{kV}$$

Problem 4:
Provide a short description of the different types of PWM methods typically used for MMC control.

Solution:
Nearest level modulation (NLM) chooses the number of levels that is closest to the reference (modulation) waveform is a fundamental frequency switching method where each SM is only switched ON and OFF once in a fundamental frequency (60 Hz) cycle. Selective harmonic elimination is used to cancel specific harmonic components and then filter out any residual components. SHE can be used in fundamental frequency switching and for PWM. For phase shift PWM, there are two main methods, one referred to as $2N$+1 PS-PWM (where carriers are shifted by 180°/N from each other and one as N+1 PS-PWM where carriers are shifted by 360°/N from each other.

Problem 5:
(a) Why is capacitor voltage balancing important in multilevel converters? (b) What is the most common method used to achieve balancing?

Solution:
(a) Most of the control methods depend on having voltages close to the nominal value. If balancing is not done, then some levels would completely discharge and others would overcharge and exceed the rating of the capacitors and/or switches.
(b) The most common open-loop balancing method inserts the highest voltage SM first when there is a discharging current and inserts the lowest voltage SM first when there is a charging current.

Problem 6:
What are the causes of circulating current in a MMC phase leg and why should it be minimized?

Solution:
Circulating current in a MMC is mostly caused by voltage variations between the capacitor voltages of the submodules within each phase unit. The capacitor voltages within these SMs are not perfectly balanced. Due to these voltage variations, there are differences in the instantaneous voltages between the upper and lower arms of each phase leg. These voltage imbalances force current to flow through the arm inductances, creating the circulating current. This current is often a second-order harmonic component. Excessive circulating current can distort the arm currents, increase losses, and potentially impact the lifespan of the converter's components.

Problem 7:
Why is a startup scheme important in an MMC?

Solution:
The individual capacitors in the submodules have to be charged up, which could result in excessive inrush current if there is nothing to limit or control the startup current. Also, the individual SMs need to have somewhat balanced voltage during startup to ensure that no SM has excessive voltage.

Glossary

Term	Definition
Arm	In a MMC converter, each phase leg consists of two arms, an upper arm connected to the positive HVDC link and a lower arm connected to the negative HVDC link
Leg	Each phase of a power electronic converter is typically referred to as a leg. Hence, a three-phase converter has three legs. In an MMC, each phase leg consists of an upper arm and a lower arm.
Submodule	Each arm in an MMC is made up of several identical power electronic submodules. Typically, this is either a half-bridge converter and capacitor or a full-bridge and converter.
PD-PWM	Phase displacement PWM is the most common form of carrier level shift PWM; it consists of multiple carriers that have an amplitude equal to the nominal voltage of an individual submodule and are displaced vertically. Each carrier can be mapped to an individual SM.
PS-PWM	Phase shift PWM has carriers that correspond to the amplitude of the full HVDC dc and are phase shifted from each other. Each carrier is mapped to an individual SM.

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