Module 5a: HVDC fault management and protection systems

HVDC LEARN
Modules for Maturing HVDC Electric Transmission Knowledge

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Prerequisite Competencies:	1. Power electronics 101: Fundamentals of switching pwr conv + EMT – Module 3b 2. Operation of thyristors & IGBTs in converters – Module 3c
Module Objectives:	1. Identify different types of fault types in HVDC systems 2. Categorize the faults based on severity 3. Develop protection schemes based on fault types

Abstract

As HVDC systems become more common place in the electrical grid topology, fault detection will play a critical role in the reliability and safety of the grid. Unlike the well-established AC fault management and protection systems employed by today's electrical grid, detection of DC faults will require a new approach. In addition to DC fault detection, methods to protect the grid from the various types of DC faults will need to be developed to ensure the least damage and downtime to the electrical grid.

The objective of this module is to discuss the various types of faults available in a two-point and multi-terminal HVDC network, assign severity levels to the faults, and manage the proper response to each fault to minimize the disruption and damage to the electrical grid. Fault management will entail the development of protection schemes relevant to each fault type.

Table of Contents

Table of Figures

List of Tables

Acronyms

AC	Alternating current
ACCB	AC Circuit Breakers
CSC	Current source converter
CWT	Continuous wavelet transform
DC	Direct current
DCCB	Direct Current Circuit Breaker
DG	Distributed generation
DLTG	Double line-to-ground
FT	Fourier transform
HB-MMC	Half-Bridge MMC
HVDC	High voltage direct current
IGBT	Insulated gate bipolar transistor
LCS	Load commutation switch
LTG	Line-to-ground
LTL	Line-to-line
LVDC	Low Volt DC
MT	Multi-terminal
OC	Over current
PTP	Point to point
ROCOC	Rate of change of current
ROCOV	Rate of change of voltage
ROTV	Ratio of transient voltage
STFT	Short time fourier transform
SVC	Static var compensator
THC	Transient harmonic current
TW	Traveling Wave
UFD	Ultra-fast disconnector
VSC	Voltage source converter
WT	Wavelet transform

5a-1 Introduction

High Voltage Direct Current (HVDC) transmission has emerged as a vital technology for modern power systems, particularly in the context of increasing renewable energy penetration and the need for long-distance power transfers. With its ability to transmit bulk power efficiently over large distances, HVDC is essential for several key applications: interconnecting asynchronous AC zones, integrating large-scale onshore and offshore renewable energy sources into the grid, and enhancing the stability and controllability of power systems. In this evolving energy landscape, HVDC grids are expected to progress beyond traditional point-to-point (PTP) configurations to form the backbone of modern transmission systems especially for the offshore wind power integration, enabling the efficient and reliable utilization of vast offshore and remote energy resources.

In addition to its capacity for large-scale power transfer, HVDC technology offers a range of operational and economic benefits. These include enhanced controllability and flexibility, greater redundancy, improved reliability and system security, and often lower investment costs compared to equivalent AC infrastructure [1]. These advantages make HVDC not merely a complementary technology, but a central element in future-proofing transmission networks.

Despite its many benefits, HVDC technology faces unique technical challenges that must be addressed to ensure safe and reliable integration into existing grids. A particularly critical challenge lies in ensuring robust DC fault ride-through capability. During a DC-side short-circuit fault in an HVDC system, significant current can be contributed by the distributed capacitors of modular multilevel converters (MMCs) particularly those based on Half-Bridge submodules—before converter blocking mechanisms are triggered. Furthermore, additional current stress can be imposed on converter semiconductor devices due to capacitive discharge from long DC cables and lines [2].

Pole-to-ground DC faults in symmetrical monopole configurations pose additional risks. These events can cause severe voltage stress on the insulation of the non-faulted DC pole and lead to sustained DC offset currents in converter transformers, which can negatively impact their thermal and magnetic performance. These issues underscore the importance of implementing advanced fault detection, classification, and management strategies that enable a fast and effective protection response.

This module focuses on the characterization and management of faults in point-to-point HVDC systems. The structure is as follows:

- **Section 5a-2** identifies and classifies the different types of faults that can occur in HVDC systems.
- **Section 5a-3** categorizes these faults according to severity and their impact on system performance.

- **Section 5a-4** presents the development of fault protection devices tailored to the HVDC fault scenarios.
- **Section 5a-5** summarizes the key learning objectives and conclusions from the module.

5a-2 HVDC fault types

When considering an HVDC system, various faults need to be considered. Among these are AC faults, internal converter faults, and DC faults. Many of these faults are caused by factors such as insulation failure caused by short circuits, switching, and lightning events. For AC faults, these can be divided into two types, symmetrical and asymmetrical. When faults occur in an AC transmission line connected to a CSC-based HVDC station, commutation failure can occur, leading to DC voltage collapse [3]. AC transmission lines are traditionally protected from such disturbances by distance relays. Internal converter faults are related to device misfire / fire-through, DC link capacitor failure and flashover, etc. [4].

On the DC side, there are three main types of faults which can occur. These include positive / negative LTG faults, LTL faults, and DLTG faults. Analysis of DC faults based on symmetric components is presented in [5]. DC faults in CSC-based HVDC line typically are not very severe. This is due to the fact that the fault current is limited by the large DC reactors at the DC terminals. However, a VSC-based HVDC system is vulnerable to DC failures due to the fast rise time and high peak and steady fault current [6]. With the increasing number of MT VSC-based HVDC systems being constructed, DC fault protection has received considerable attention. Analytical and simulation studies on DC faults in HVDC systems are presented in [7, 8, 9, 10, 11, 12, 13, 14, 15].

5a-2.1 DC line-to-ground fault

There are two types of HVDC lines we consider when talking about LTG faults, underground and overhead. In the case of underground lines, the fault is typically caused by insulation failure between the DC conductor and the ground. For overhead lines, the fault is mainly caused by lightning strikes and pollution. These faults also tend to be temporary. Figure *1* shows the equivalent circuit of an LTG fault [16]. R_1, R_2 and L_1, L_2 represent the equivalent resistance and inductances of the fault line from the VSC to the fault point.

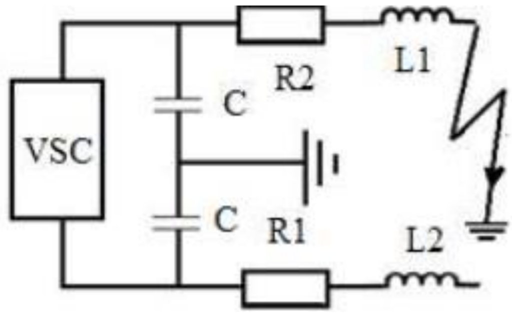


Figure 1. DC LTG fault equivalent circuit

LTG faults frequently occur and are mainly dependent on the grounding of the HVDC system. The fault resistance should not be neglected, as it plays a significant role in the system response. In a normal HVDC system, there are two ground points, the neutral-ground link of the transformer and the mid-point of the DC link capacitor. A LTG fault produces an additional ground point in the system. This additional grounding point forms a ground loop among the grounding points. The LTG faults can be analyzed using two stages, capacitor discharging and grid current feeding phases [16].

At the beginning of the LTG fault, the capacitor discharging stage begins with the capacitor discharging. This creates a discharge circuit between the fault pole capacitor and the fault impedance through the fault line. The dc-link capacitor, transmission line inductance, fault resistance, and ground point form a loop circuit. The equivalent circuit is shown in Figure *2* [17], where R and L are the equivalent resistance and inductance of the fault line from the VSC to the location of the ground fault, C is the capacitance of dc-link capacitor and Rf is the fault resistance. The equivalent equation of the circuit is,

$$\frac{LC}{2}\frac{d^2VC}{dt}+\frac{RC}{2}\frac{dVc}{dt}+Vc=0 \quad (1)$$

Where Vc is the capacitor voltage between faulty transmission line and ground point and R= R1+ R2, L= L1+L2 from Figure *1*.

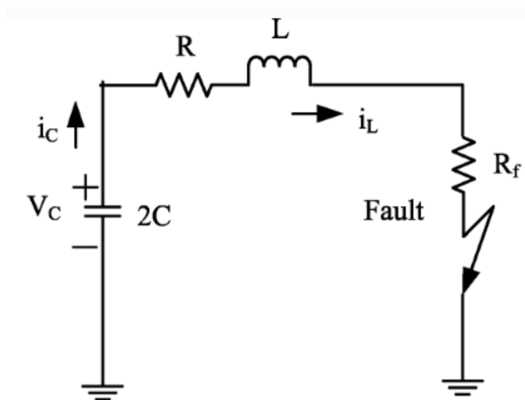


Figure 2. DC LTG fault capacitor discharge equivalent circuit

During the discharging stage of the DC side capacitor, the DC voltage will continuously drop. Once the DC voltage drops below any of the AC phase voltages, the system will experience the grid side current feeding. This stage will continue to the point where the DC voltage becomes higher than the AC phase voltage again. Figure 3 shows the equivalent circuit for the power supply stage on the side current feed stage. During this stage, the DC side capacitor is charged through the fault line by AC power. The duration of this stage is short with low current. If the response to the LTG fault can be made in a timely response, the DC voltage would avoid dropping to below the AC phase voltage and the grid side current feeding stage would be skipped.

The response to an LTG fault for various lengths of transmission lines can be seen in Figures 4 and Figure 5 [17]. Analytical and simulation studies of the fault current contribution under line-to-ground faults from various sources such as the DC capacitor and reactor, and AC network are presented in [18, 19, 20, 21].

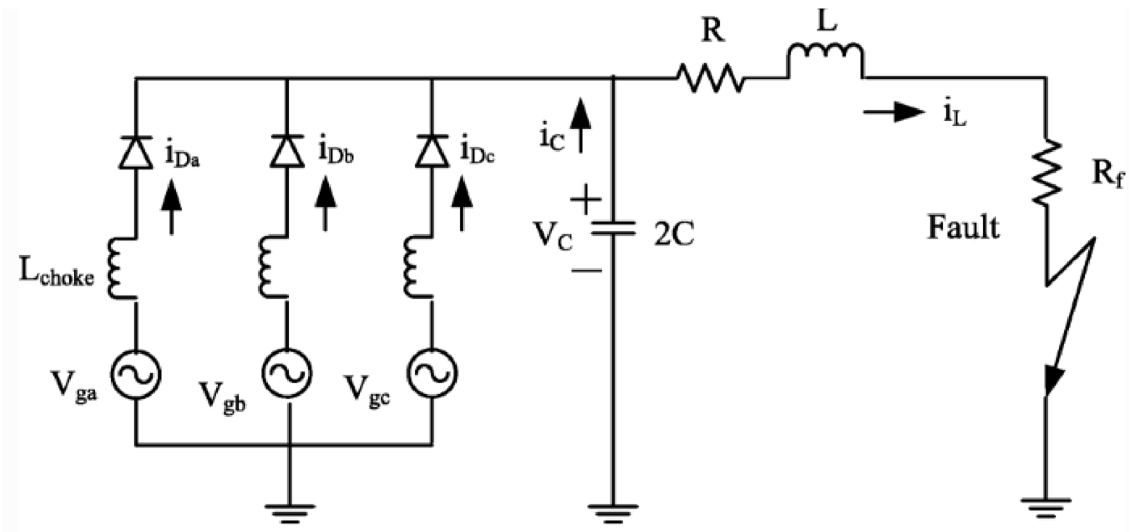


Figure 3. DC LTG fault grid current feeding equivalent circuit

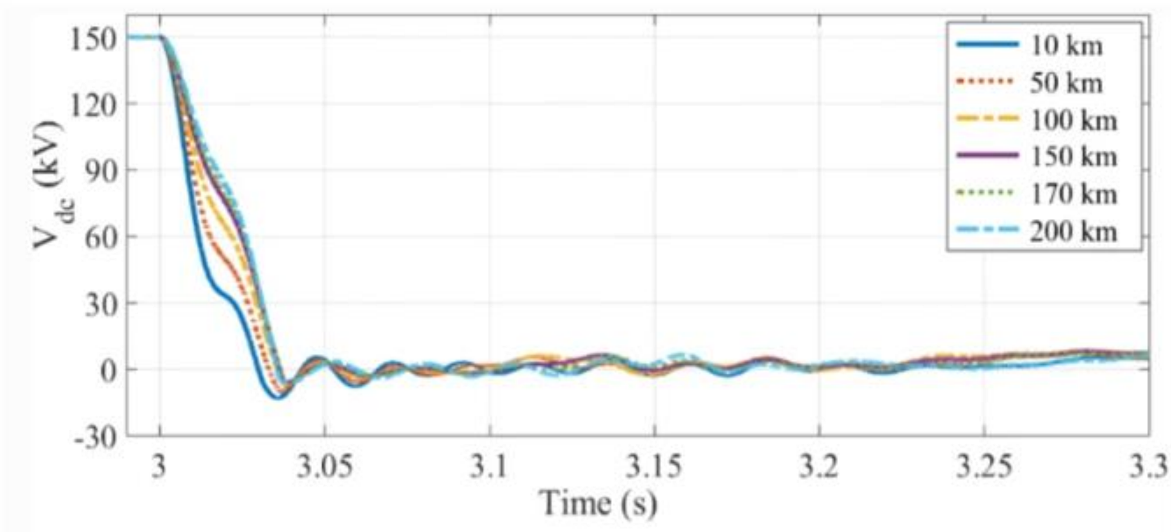


Figure 4. DC LTG fault positive voltage (V_{dc})

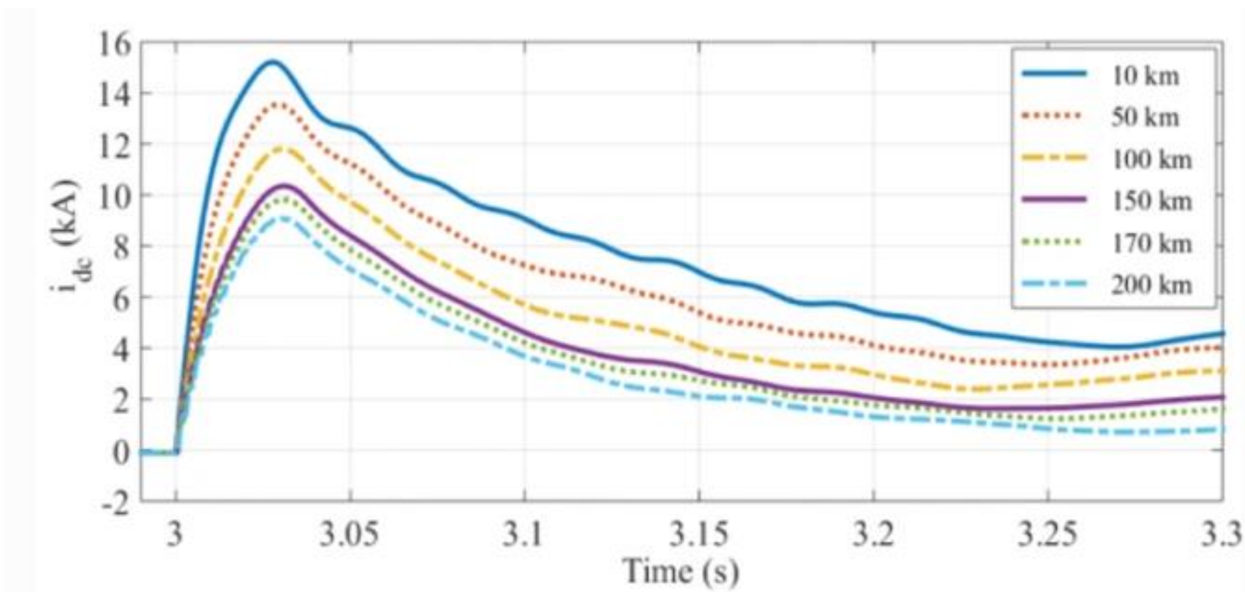


Figure 5. DC LTG fault current (i_{dc})

5a-2.2 DC line-to-line fault

An LTL fault is the worst case of DC faults in the operation of a VSC-HVDC system. Fortunately, these types of faults are usually rare. Figure *6* shows the equivalent circuit of an LTL fault where R1, R2, L1, L2 are the equivalent resistances and inductances of the positive and negative lines from the VSC to the location of the line-to-line fault respectively and C is the capacitance of the dc-link capacitor in parallel with the VSC [22].

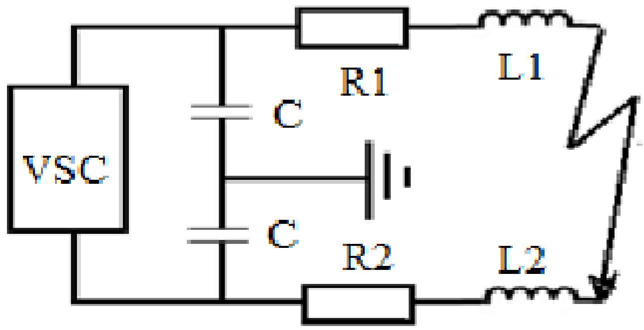


Figure 6. DC LTL fault equivalent circuit

When the LTL fault occurs, the IGBTs in the VSC are blocked and the fault current flows through the antiparallel diodes. There are then three stages that the fault goes through, capacitor discharging, diode freewheeling and grid current feeding.

Like what was discussed in 5a-2.1, when the fault occurs, a loop circuit without source is formed. Figure *7* shows the equivalent circuit of the capacitor discharge stage [22]. At this point, the DC link capacitor begins to rapidly discharge, leading to a collapse of the DC voltage. As the DC-link capacitor discharges through the DC transmission line, the DC voltage in both the positive and negative lines quickly decreases, while the DC current quickly increases. Figure *7* shows the positive LTL fault DC voltage for various lengths of transmission lines [17]. The DC fault current response for various lengths of transmission lines can be seen in Figure *8* [17]. The capacitor discharging stage ends when the capacitor voltage drops to zero.

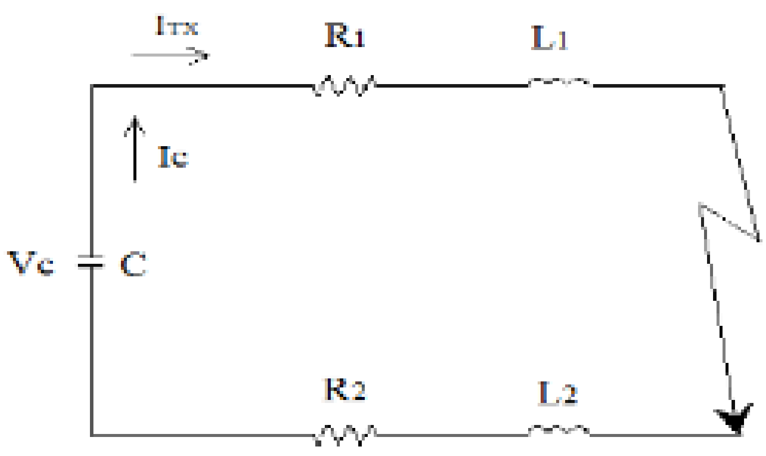


Figure 7. Equivalent circuit of capacitor discharge stage

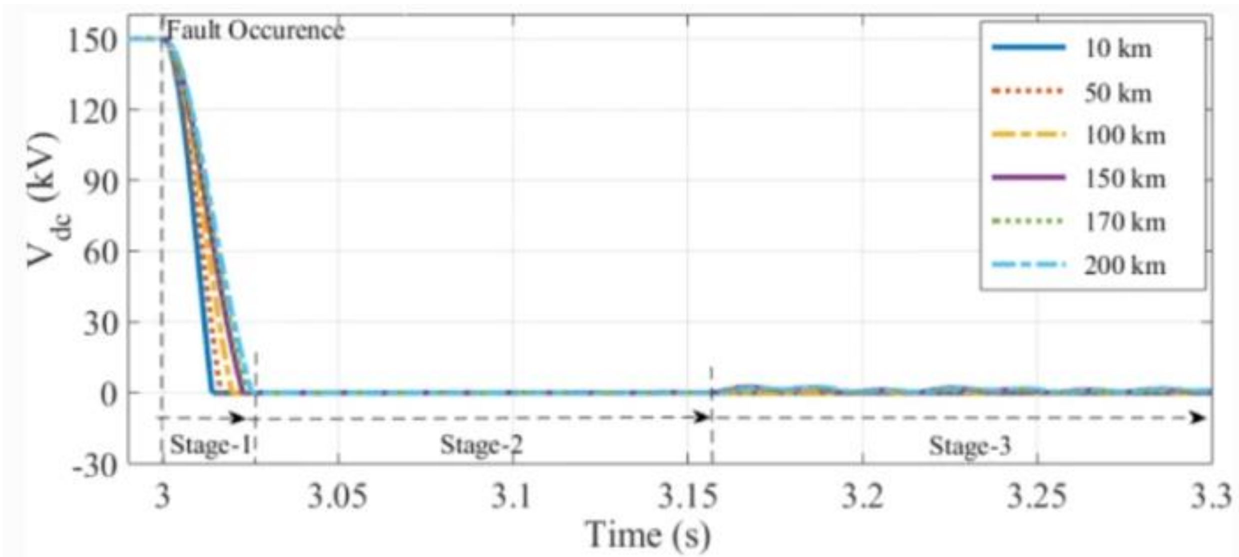


Figure 8. DC LTL fault positive voltage (V_{dc})

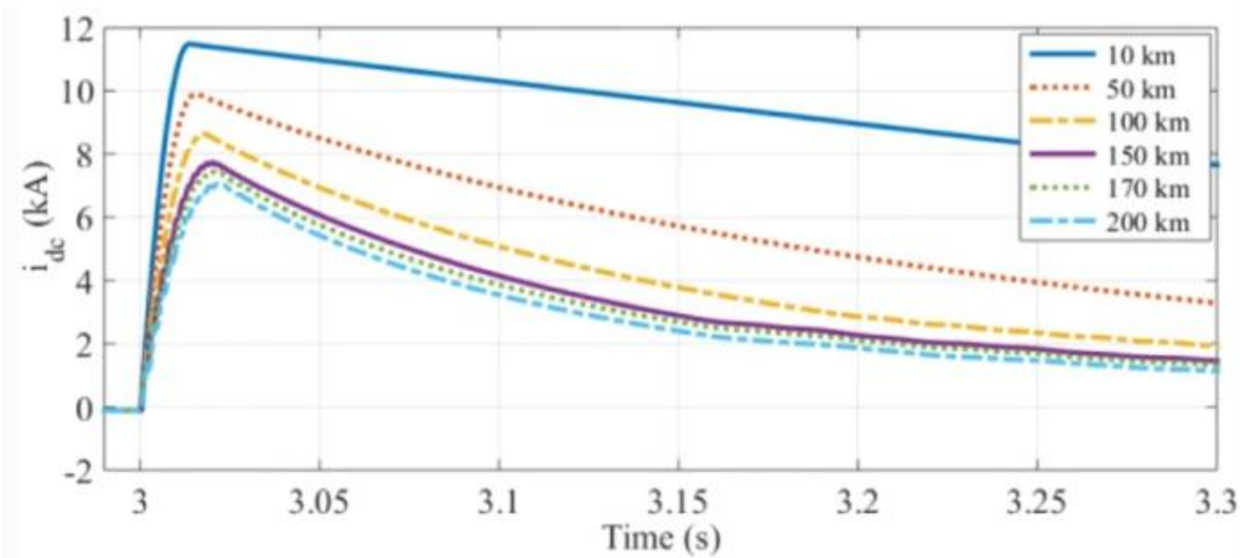


Figure 9. DC LTL fault current (i_{dc})

When the capacitor voltage drops to zero, the DC fault is pushed over to the converter freewheeling. This begins the diode freewheel stage. This is the most hazardous period, as the circulating fault current can destroy the anti-parallel diodes. Figure 10 shows the equivalent circuit for the diode free-wheel stage [22].

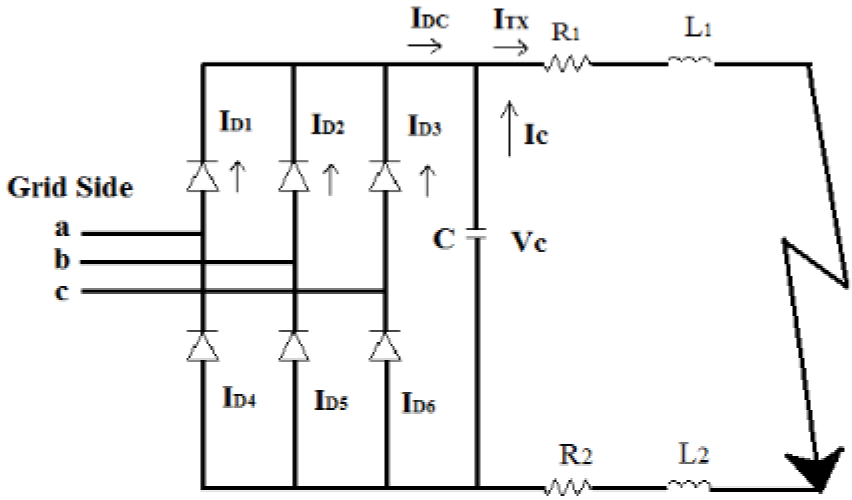


Figure 10. Equivalent circuit of diode freewheel stage

A loop circuit is formed as the DC-link voltage drops to zero. This leads to the grid current feeding stage. Figure *11* shows the equivalent circuit of the grid current feeding stage [22]. During this stage, the IGBTs are blocked, and the converter behaves as an uncontrolled rectifier, injecting current into the DC side fault.

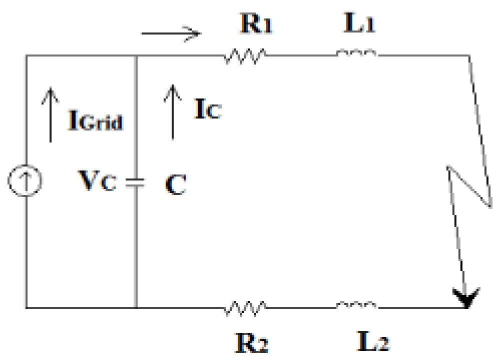


Figure 11. Equivalent circuit of grid current feeding stage stage

A VSC-based HVDC system (±150 kV test system) with CLR is considered for the DC fault studies, and its detailed modeling is given in [23].

5a-2.3 DC double line-to-ground fault

A DPTG fault in an HVDC line is a fault condition in which one or more of the HVDC conductors (poles) of a bipolar transmission line come into contact with each other or with the ground. In a DPTG fault, current flows from one pole to the other through the ground, causing a significant increase in ground potential and potentially damaging nearby equipment. The fault can also cause a rapid decrease in voltage at the fault location, which can lead to a loss of power transmission in the affected section of the HVDC line.

The probability of DPTG fault occurrence is much lower and almost unfeasible if both positive and negative conductors are placed on different cables. However, if a DPTG fault occurs, then the fault will go through the same three stages as described in 5a-2.2 for the LTL fault scenario. The responses of the DC voltage and current under double line-to-ground faults at various distances are shown in Figure *12* and Figure *13* respectively [17].

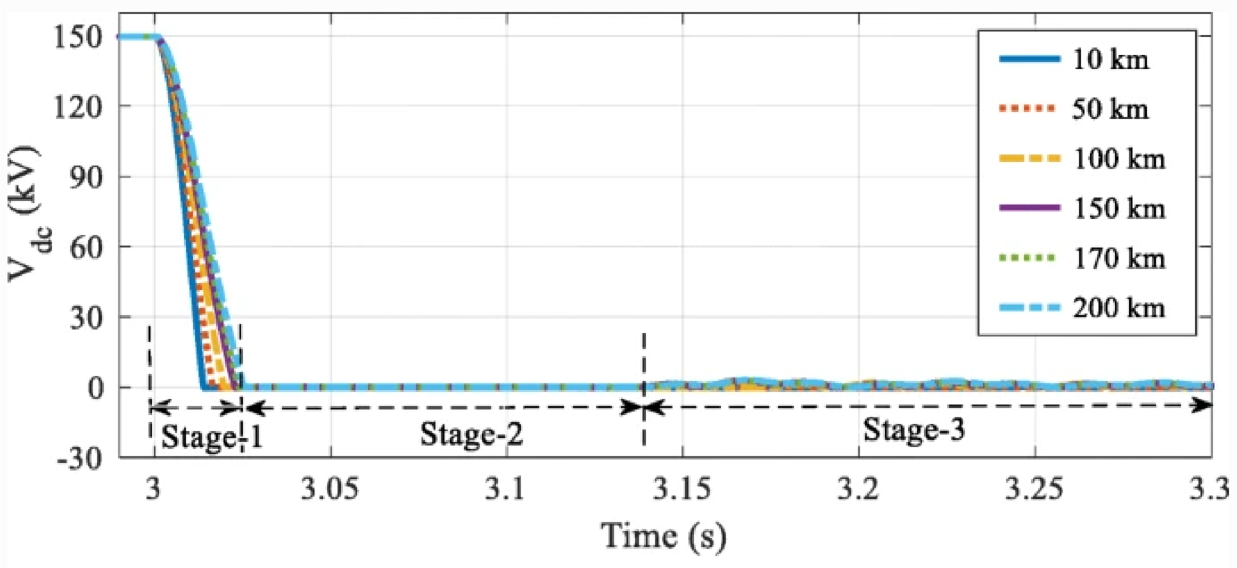


Figure 12. DC DLTG fault positive voltage (V_{dc})

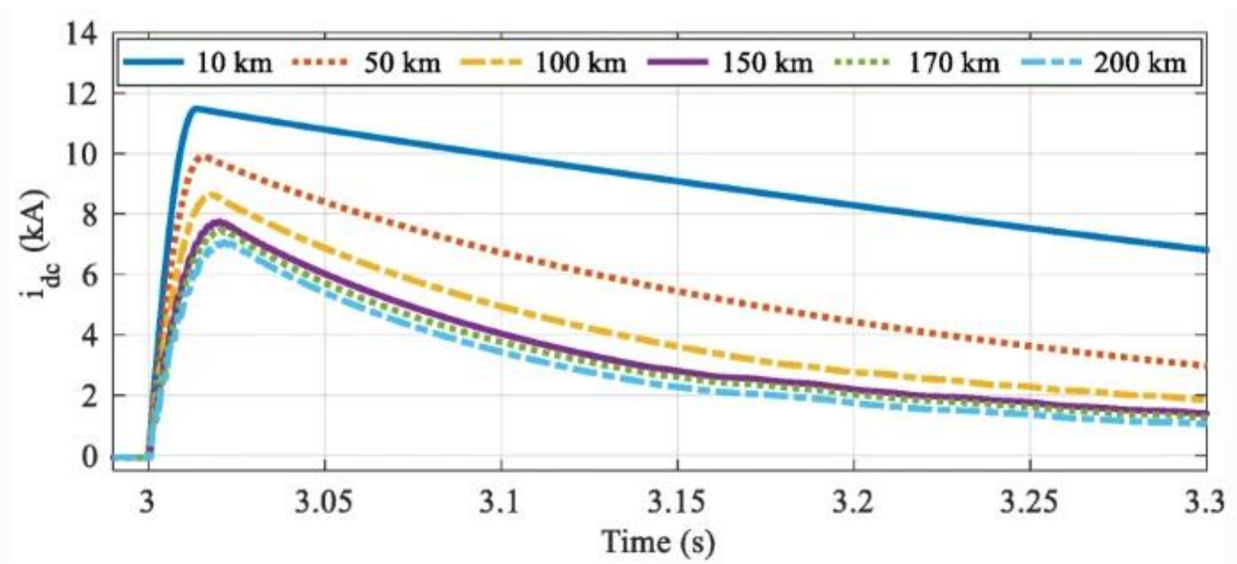


Figure 13. DC DPTG fault current (i_{dc})

5a-3 HVDC fault detection

In an AC transmission system, protection is one of the most critical aspects that should be used to ensure a reliable and resilient system. It is not different for a DC transmission system. Therefore, a critical part of a VSC-HVDC network is the fault detection algorithms embedded in protective relaying systems. In an HVAC system, the protection algorithms are categorized as either (i) single-end/multi-end measurement-based methods, or (ii) unit/non-unit-based methods, or (iii) communication/non-communication-based methods [24]. These terms describe the different characteristics or features of the protection schemes used in power systems. We can take this same approach and apply it to the HVDC system.

The protection algorithms operate on the basis of the data acquired from voltage and/or current signals from single or multiple ends of MT-HVDC systems. The single-end information-based methods are less costly and less selective as compared to multi-end information-based methods. The protection scheme based on multiple end measurements generally requires an advanced communication infrastructure and relay technology [24]. Communication-based approaches are inherently selective [25]. However, the time delay imposed by the communication channel makes it unsuitable for an application demanding fast relaying speed [26]. Another important aspect of the protection system is the range of protective relays used. Based on the ranges, the protection system can be broken down into unit and non-unit-based methods. The unit protection method is designed to create a fixed boundary in which a particular zone will be protected. The voltage or current signals are measured at each end of the protected zone. Similarly, the non-unit schemes are designed for the protection of a specific area but have no fixed boundaries. Although protective zones are created to protect their specified areas, the zones can overlap with other zones in the system. The non-unit schemes are inherently capable of providing backup protection whenever a neighboring protection system fails to operate.

This section will list and describe some of the main methods in use today to detect faults in the HVDC systems.

5a-3.1 Handshaking method

In MT-HVDC systems, the handshaking-based protection methods are used to differentiate and identify various LTL and LTG faults. Based on this method, if a fault (for instance, a positive LTG fault) occurs in a line of an MT-HVDC system, then the current direction of the faulted line will always be positive (from bus to fault point) and regarded as a positive fault current. On the other hand, in the case of a healthy line, the fault current is always negative and is considered a negative fault current. This principle can be utilized as a handshaking method to detect faulty and healthy line segments. One handshaking method described in

[27] describes detecting DC faults in MT-VDC grids DC switches and ACCB. When a fault occurs in the DC line, the ACCB operates followed by the DC switch. This isolates the faulted line from the healthy DC network and the AC side. This handshaking method can be applied to PTP HVDC networks and is typically less expensive than using DCCBs. In the case of a MT HVDC network, when the ACCB operates, all the MMCs should be shut down. This will in turn interrupt the power flow within the entire network. When this occurs, the capacitor discharge and diode freewheeling described in 5a-2.2 will occur within a few milliseconds. This can lead to damage to the power electronics within the network.

The handshaking methods offer an economical, highly reliable detection and isolation of faults in an MT-HVDC system based on local measurements which negates the need for communication systems. One downside to the handshaking method is that it can temporarily de-energize the whole grid following unwarranted outages. This makes it unsuitable for local distribution networks and LVDC microgrids, where a lot of energy resources and loads are coupled to the system [28-30].

5a-3.2 Traveling wave method

The fundamental principle of TW is described in [31-32]. In contrast to an AC system where there are no transient TWs at the fault point for the fault inception angle at the zero-crossing point, the transient TW is present for the fault at any point in a DC transmission line. This property makes the TW method suitable for an HVDC transmission line. At the moment of fault occurrence on the transmission line, the fault current and voltage give rise to impulses that travel from the point of fault occurrence to the line terminals. This phenomenon of fault current represented by TWs is highlighted by the Bewley lattice diagram shown in Figure *14* [24]. The fault location and detection tasks are performed by estimating the reflections of this wave at one or both ends of the transmission line.

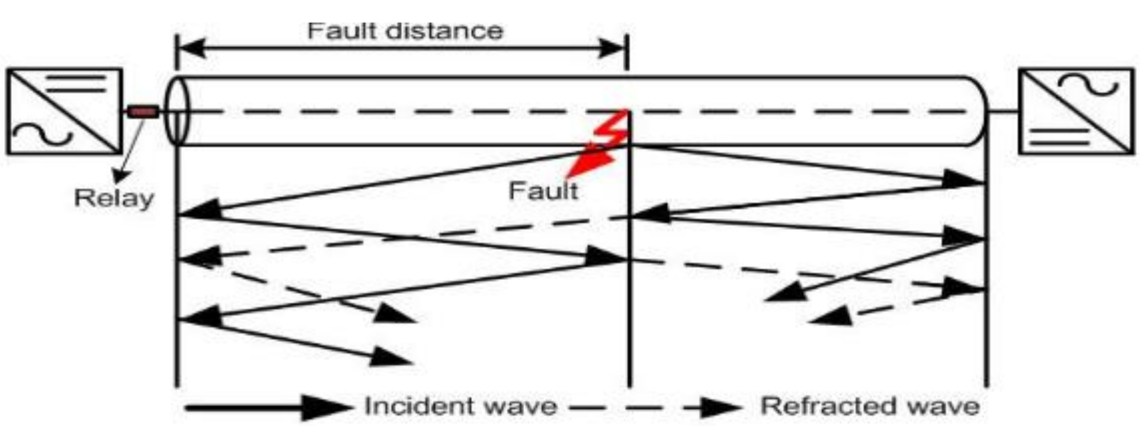


Figure 14. Bewley lattice diagram

The TW based method can be used based on measurements from a single end or both ends of the transmission line. Using measurements from a single end of the line presents the simplest method without the need for communications on the line. If using both ends of the line for measurement, then a communication infrastructure must be in place. There are several different TW approaches that are in use today. Some of the more common ones are highlighted below.

Reference [33] describes a two-terminal TW-based fault location method used to protect an MT-HVDC system. In this method, the surge arrival time used for the calculation of the fault distance has been tracked using CWT applied to the current signal extracted only from the converter stations. The fault distance can be calculated by

$$x_F = \frac{(L-(\Delta t)\times v)}{2} \tag{2}$$

Where L is the line length, v is the propagation velocity and Δt is the surge arrival time difference.

Reference [34] presents the protection method for an MT-HVDC grid with an inductive DC terminal. This uses a directional protection scheme to identify the fault by comparing the polarity of transient energies at both ends of the HVDC line. The method is stated to be more reliable in comparison to conventional directional approaches for the MT-HVDC grid with inductive termination.

References [35 and 36] propose a hybrid protection scheme based on both TW and boundary protection to differentiate between internal and external faults. In addition, this method can also be used to detect closed faults. The differentiation is accomplished by using a one-end high frequency transient signal. This method does require a high sampling frequency of up to 50 kHz to resolve a useful TW.

Reference [37] proposes a protection algorithm for LCC-HVDC grids, where the traveling wave propagation process is used to differentiate the internal fault from the external fault using the Teager energy operator (TEO). There are several advantages to this method including: easy calculations, faster detection speed, as it uses only a 2-millisecond sampling data window, not needing to extract any harmonic or high-frequency components, and detection of high impedance and long-distance faults.

Reference [38] describes an integrated TW-based DC-line fault detection and faulty pole identification method using symmetrical component analysis. The values of the voltage and current TWs are calculated and analyzed. After the analysis, a detection criterion is laid out based on the positive and zero sequence backwards TWs.

Note that in the traveling wave-based method, the detection of the wave head is the key challenge in identifying faults in an HVDC line. It is also difficult to detect the surge arrival time since the traveling wave is very weak in the case of high fault resistance and continuous variation in the transition resistance [39].

5a-3.3 Transient method

In the transient-based method, high-frequency components of the voltage/current signals are typically used to recognize the DC line faults. This makes the method more capable and robust against high transition resistance [24]. There are many different schemes available which use this method for fault detection. Several of these are described below.

Reference [40] proposes a fault location scheme for MT-HVDC systems using the non-characteristic frequency signal extracted with the help of a complex wavelet transform from the current signal. An internal fault occurs when the characteristic frequency current is more than the non-characteristic frequency current; otherwise, it is considered as an external fault.

Reference [41] presents the fault location method based on the sheath voltage for a two-terminal VSC-HVDC system. The sheath of the cable is grounded at each converter substation and the sheath voltage is measured at this point. During no-fault conditions, the transient voltage in the cable sheath is zero, and no current flows through it. However, in a fault situation, the transient voltage of the cable sheath has a certain magnitude, leading to a fault current flowing through it. Therefore, the transient voltage of the cable sheath is used to identify the fault, and the signs on both sides are applied to discriminate between the DC fault and capacitor unbalance.

Reference [42] shows a time-domain transient-based protection scheme that uses TW power for a four-terminal MCC-HVDC grid. Proper thresholding is provided to the TW power to differentiate internal and external faults. The direction selectivity analysis has been carried out by calculating the ratio of forward and backward TW power.

Reference [43] highlights a protection scheme for the VSC-MT-HVDC system that can provide primary and backup protection. The principles for both primary and backup relaying schemes are based on the supplementary inductor used at each terminal of the DC line. Fault recognition has been accomplished using the ROTV computed at both sides of the inductor. The primary scheme is non-communication based, whereas the backup relaying is a pilot scheme based on the ROTVs at both ends of the DC line segment.

Reference [44] presents a transient harmonic current (THC)-based scheme to detect and classify the internal and external faults in the MT-HVDC grid. The transient harmonic current is low in the case of an external fault since it is limited by the DC filter and smoothing reactor, but it has a high value for an internal fault. Therefore, the difference between the THC at both ends is applied to differentiate between the internal and external faults. There are a few drawbacks to this scheme, the sensitivity of this protection scheme is affected by the fault resistance and location, and it requires both side information to make the decision. This may impact the reliability of the scheme and the cost factor because of the requirement for communication infrastructure.

5a-3.4 Impedance based method

The time-domain fault location method based on a distributed parameter approach for the AC and DC transmission lines uses the voltage distribution calculation of the line to locate the fault. This is achieved by taking the synchronously measured voltage and current at both ends of the line [45-48]. This method can acquire any section of the data, from the fault transient to the steady state, and simply requires a low sampling frequency to obtain accurate results. One drawback of the method is that it is sensitive to parameter uncertainty such as characteristic impedance, velocity, and line resistance. Each of these parameters generates inaccuracies in the voltage distribution calculation. Unsynchronized two-end measurements also affect the protection scheme. The ability to consider uncertain line parameters and unsynchronized measurement time differences to locate the fault in an HVDC transmission line is demonstrated in [49].

Using a two-voltage divider arrangement, the fault distance can be calculated [50-51]. In this arrangement, the DC current measurement is not taken for the distance calculation. This is due to the possibility of measurement error caused by the immediate change in high fault current. In place of DC current measurements, two voltage sensor units are used to calculate the fault distance, as shown in Fig. 15 [17] where one sensor unit is used at the relay point (n) and the other is the reference voltage sensor unit (r) used to avoid long-distance communication.

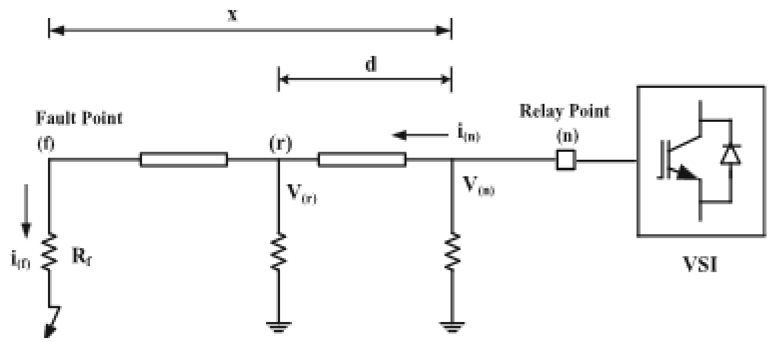


Figure 15. Fault distance calculation using two voltage dividers

From Fig. 15, the voltage at the relay point (n) is given by

$$V_n = x \times R \times i_n + x \times L \times \frac{di_{(n)}}{dt} + V_f \tag{3}$$

$$V_n = x\left(R \times i_n + L \times \frac{di_n}{dt}\right) + V_f \tag{4}$$

$$V_n = d \times R \times i_n + d \times L \times \frac{di_n}{dt} + V_r \tag{5}$$

$$\frac{V_n - V_r}{d} = R \times i_n + L \times \frac{di_n}{dt} \tag{6}$$

Substituting (6) into (4) yields

$$V_n = x\left(\frac{V_n - V_r}{d}\right) + V_f \tag{7}$$

The fault distance (x) is given by

$$x = d\left(\frac{V_n - V_f}{V_n - V_r}\right) \tag{8}$$

where V_r and V_f are the voltages at the reference sensor and fault point, respectively. R and L are the line parameters. In terms of a solid fault, $R_f = 0$ and $V_f = R_f \times i_f = 0$ and the fault can be accurately measured by the two-voltage divider arrangement. It should be noted that this method only looks at the fault location. In the case of a high-resistance fault, the distance estimation may not be accurate.

In the case of a remote end fault in the two-terminal bipolar HVDC transmission line shown in Fig. 16 [17], reference [52] provides a method of protection for the line.

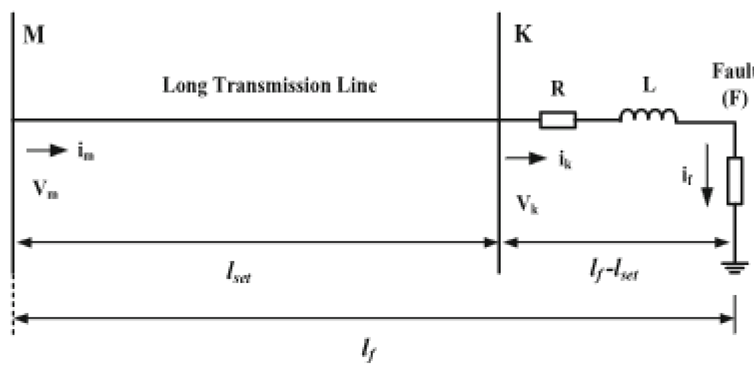


Figure 16. Transmission line model under fault (F) condition

The inductance (L) of the transmission line is mainly dependent on the frequency. Based on this, the distance protection considering frequency-dependent parameters is taken to evaluate the fault distance in the HVDC line. The distance relay is located at point M. Voltage and current V_m and i_m are measured at the relay location M, and V_k and i_k are the voltage and current at the setting point K. The accuracy is dependent on the conditions set forth in (9)

$$E_r < |l_f - l_{set}| \tag{9}$$

where Er is the measurement error, l_f and l_{set} are the fault and setting distances, respectively. The allowable error ($l_f - l_{set}$) is the difference between the fault distance and setting distance. The allowable error vs. fault distance is shown in Fig. 17 [17].

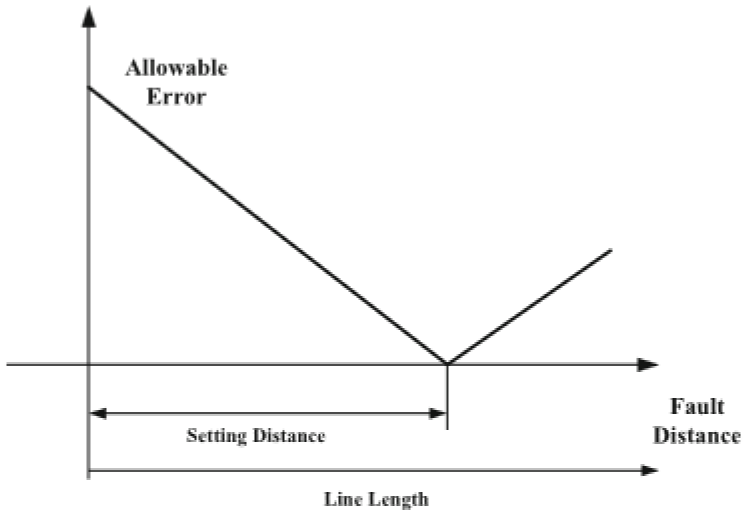


Figure 17. Allowable error vs fault distance

There is a very small allowable error when the fault occurs near the setting point K. Therefore, high accuracy is very important in this method. The measurements are taken at the setting point (K) with the help of the frequency-dependent parameter line model. The voltage at the setting point and the criteria for identifying the fault are given by

$$V_k = \left(Ri_k + l\frac{di_k}{dt}\right)\left(l_f - l_{set}\right) + R_f i_f \quad (10)$$

$$l_f \leq l_{set} \quad (11)$$

If the fault occurs near or at the setting distance or point, the allowable error E_r tends to become very small. This, in turn, will affect the accuracy of the protection scheme.

5a-3.5 Wavelet transform-based method

Non-stationary signals are an important component for the protection of a HVDC transmission line. Fourier transform (FT) has been used to extract the spectral components of a signal, but it only provides the frequency components in the signal with no time information. This makes it unsuitable for non-stationary signals. Short time Fourier transform (STFT) is now used to extract the spectral contents of the signal. This provides the existing frequency bands and corresponding time intervals, but it does not provide information on the existing frequency at the time instant. This is where WT comes into play. WT is used to extract the transient signals from faults and other disturbances. In terms of signal processing methods to track fault transients in nonstationary signals, WT is a powerful tool [53-57]. The continuous wavelet transform (CWT) of a signal f(t) is given by

$$CWT(a,b) = \int_{-\infty}^{\infty} f(t)\, \varphi_{a,b}^{*}(t)dt \quad (12)$$

$$\varphi^*_{a,b}(t) = \frac{1}{\sqrt{a}}\varphi(\frac{t-b}{a}) \quad (13)$$

Where $\varphi^*_{a,b}(t)$ is the complex conjugate of the mother wavelet, and a and b are the respective scaling and shifting parameters.

There are several different TW approaches that are in use today. Some of the more common ones are highlighted below.

Reference [58] demonstrates how WT is applied to identify the DC fault in the MT VSC-HVDC system using local measurements. Here, DC voltage, current, and their derivatives are used as wavelet coefficients, and triple modular redundancy (TMR) is used to achieve selectivity.

Reference [59] the fault current rising time is captured using WT to detect the fault in the HVDC system.

Reference [40] describes how the complex WT is used to extract the characteristic and non-characteristic frequency current for fault detection in an MT-HVDC line.

References [60-61] explain how discrete WT is used to track high-frequency transient signals to locate the fault in the MT HVDC system.

Reference [41] shows how WT is used to extract the high-frequency transient of the cable sheath voltage to detect faults in a VSC-HVDC line.

Reference [45] presents the boundary discrete WT based overcurrent protection for the IEEE 30 bus distribution system with DG. In this reference, the simulation results are compared to the conventional FT based overcurrent protection.

It should be noted that in the WT based protection methods, the wavelet coefficient is predefined for the fault detection. The fault inception angle and fault resistance can influence the effectiveness of the wavelet co-efficient-based protection scheme. In addition, it may not be suitable for a standalone protection method [17].

5a-3.6 Natural frequency-based method

In the natural frequency-based method, the natural frequency of a line is a combination of harmonic frequencies, which consist of the frequency components of the generated traveling wave due to the fault or any other transient events. In this method, the one-end transient signal is enough to detect the fault, and there is no need to track the wave head. There are various ways to apply this method for fault detection. One method is demonstrated in [62] where it explains the relation between the natural frequency and fault distance when the impedance of the system is zero or infinite and uses the distributed parameter model.

Reference [63-64] demonstrates a fault location method in a two-terminal VSC-based HVDC system by extracting the natural frequency of the fault current. During a fault occurrence, the

DC line has a high transient energy which will create more natural frequency components. The natural frequency is generated by the distributed parameters and reflection of a traveling wave. Also, the natural frequency signal is reflected by the shunt capacitors, which makes extraction easy. The natural frequency is related to the wave speed and the fault distance l is given by

$$l = \frac{kv_k}{2f_k} \quad (14)$$

where k is an integer, f_k is the natural frequency of the kth order and v_k is the velocity of the traveling wave. The accuracy of this protection scheme depends on the extraction of the natural frequency and the calculation of the velocity of the traveling wave. In the natural frequency-based method, any section of the data during the fault period can be applied to identify the fault in an HVDC line. This differs from the wave-head detection in the TW method.

Reference [65] demonstrated where the natural frequency is used to locate the fault in a bipolar CSC-based HVDC system. Here the dominate natural frequency is used to fine the faut distance by calculating the traveling wave velocity and reflection coefficient.

Note that the natural frequency-based method may not be suitable for time-varying transients. When a fault occurs in a DC line, a natural frequency may be generated due to resonance caused by the shunt capacitor and line inductor, and the accuracy of measurement decreases as the fault distance increases.

5a-3.7 Derivative method

Derivative-based methods are based on the rate of rise in voltage (dv/dt) or current (di/dt) measurement at a single end of the HVDC grid. These are classified as non-unit protection schemes and can be considered as one form of traveling wave-based protection [24]. In terms of speed and fault detection, the (dv/dt)-based protection method is more advantageous than the OC and current differential schemes [66]. The accuracy of this scheme is influenced by feeder length, and the selectivity is reduced with less line impedance. The (di/dt) scheme uses an initial rate of rise of current for fault decision-making. This closely relates to the voltage derivative. This principle is also like OC protection, but the amplitude of the current transient is used instead. This method is vulnerable to a noisy environment and could falsely operate based on the possibility of inappropriate data sample collection [67]. There are several different derivative-based approaches are currently in use today. Several of these are referenced below.

Reference [68] outlines a one-end (dv/dt) and (di/dt) based protection scheme for the MT-HVDC system. The fault can be identified if the rate of change of DC voltage and current exceeds the preset threshold.

Reference [69] presents the fault detection in an earthed HVDC grid based on the ROCOV. In the scenario, the peak fault current is controlled to be below the DCCBs current rating by connecting a DC inductor in series with the DCCB. This proposed fault detection method is shown in Figure *18*. The voltage across the inductor V_L is given by

$$V_{L(t)} = L\frac{di(t)}{dt} \tag{15}$$

From Fig. 18, the voltage at the bus terminal is given by

$$V_{bus(t)} = V_{L(t)} + V_{line(t)} \tag{16}$$

$$V_{L(t)} = V_{bus(t)} - V_{line(t)} \tag{17}$$

Substitution of (17) into (15) gives

$$L\frac{di(t)}{dt} = V_{bus(t)} - V_{line(t)} \tag{18}$$

$$\frac{di(t)}{dt} = \frac{V_{bus(t)} - V_{line(t)}}{L} \tag{19}$$

Where Vbus is the voltage at the bus terminal, Vline is the voltage on the transmission line or cable side, and L is the inductance value. When a fault occurs in a line, V_{bus} is constant for the first few milliseconds, and the ROCOC at the DCCB is mainly dependent on the V_{line}. Hence, the fault location can be achieved by measuring the ROCOV on the line side of the limiting inductor. By setting the preset threshold values, the different zone and bus faults can be distinguished through the variation range of the ROCOV. By increasing the value of the inductor connected in series with the DCCB, the rate of rise of the fault current can be limited. This assumes that the DC voltage of the converter output is constant after the fault.

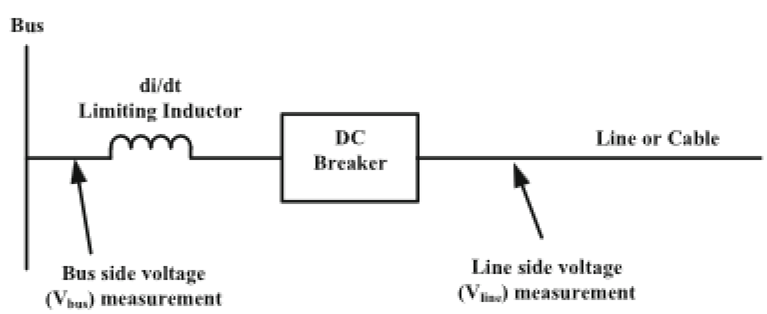


Figure 18. Illustration of fault detection method

Reference [70] describes a non-unit protection scheme for the MT-HVDC system, where the inductive termination decides the zone of protection. In this scheme, under-voltage detection is applied to detect the fault with a pre-set threshold value of 85% of the rated DC voltage. After fault identification, the (dv/dt) and (di/dt) are used to discriminate the first and second zone faults. Knowing that the (dv/dt) is susceptible to close faults and noise, a directional criterion of (di/dt) is used to discriminate the frontward and backward faults. However, the scheme may falsely operate during zone 2 solid faults as it shows very similar characteristics in the case of zone 1 high-resistance faults. However, the threshold setting for the fault discrimination criterion may not work properly when the fault resistance variation is high.

5a-4 HVDC fault protection

In today's HVAC system, ACCBs are mainly used to disrupt the excessive current created during a fault. This is different for HVDC systems. Compared to HVAC systems, there is no zero crossing of the current in the transmission lines. When a fault occurs in the HVAC line, a mechanical breaker can operate at the point of zero crossing of the AC current. The HVDC system does not have this ability. Therefore, to protect the HVDC system, a different style of DCCB is used

Today, there are three main types of DCCBs used to protect the HVDC system. These can be broken down into all-solid HVDC breakers, resonant HVDC breakers, and hybrid HVDC breakers [71].

This section will discuss the three types of DCCBs being used today.

5a-4.1 HVDC breakers

This section presents the three types of HVDC breakers used today.

5a-4.1.1 All-solid HVDC breaker

Reference [72] describes an all-solid DCCB. Figure *19*(a) [71] shows the circuit diagram for the breaker. The sending end of the HVDC system is indicated and the IGBTs are connected in series in the HVDC line. When the fault current is detected as shown in Figure *19*(b), all IGBTs are blocked. The paralleled capacitor of each IGBT is charged through the loop. When the current of the HVDC breaker decays to zero, the rest energy will be consumed in the designed loop.

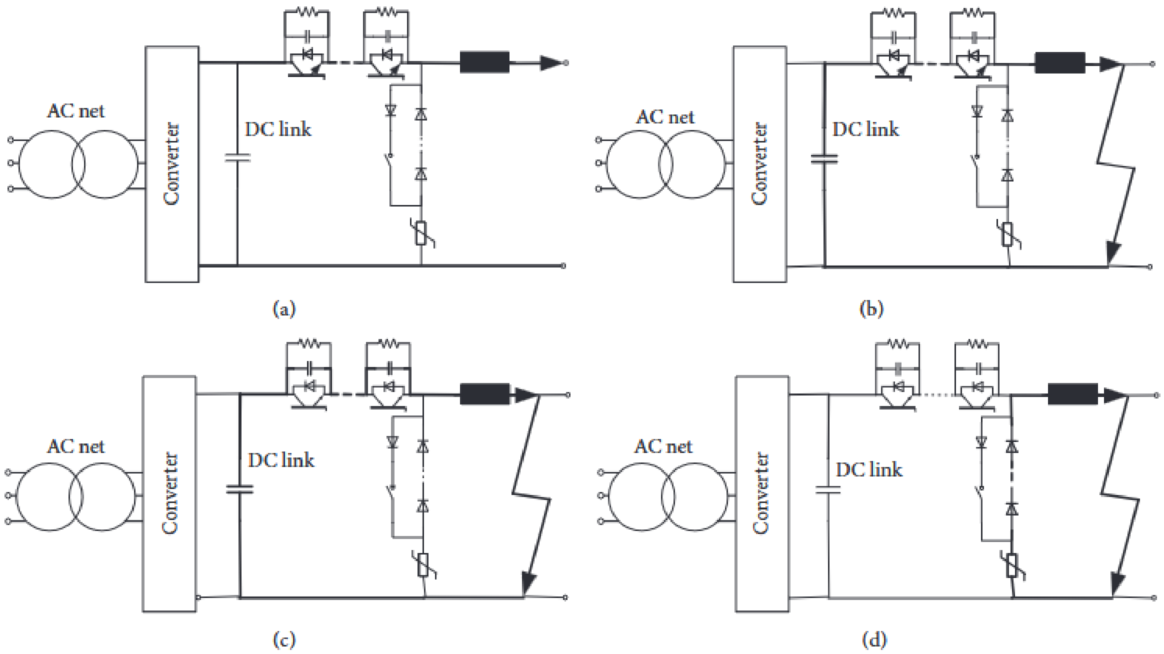


Figure *19*. Structure and working principle of all-solid DCCB (a) Normal operation of all-solid HVDC. (b) Short circuit fault occurs. (c) The paralleled capacitor of each IGBT is charged through the loop. (d) The rest energy is consumed in the designed loop.

In this system, the switching time of this DCCB is very fast, almost equal to the switching time of IGBTs. Because of this fast-switching time, the over current is low. All IGBTs in the HVDC line have conduction loss During normal operation. This leads to high total losses in this DCCB.

5a-4.1.2 Resonant HVDC breaker

Reference [73] presents a model of resonant DCCB. The structure of this breaker is shown in Figure *20* [71]. During normal operation, the DC current flows through the mechanical switches. At the inception of fault current, the vacuum switches begin to operate. The current in one of the switches will commutate to its parallel diode and will flow through a plasma in another vacuum switch when the contacts in the vacuum switches begin to separate,

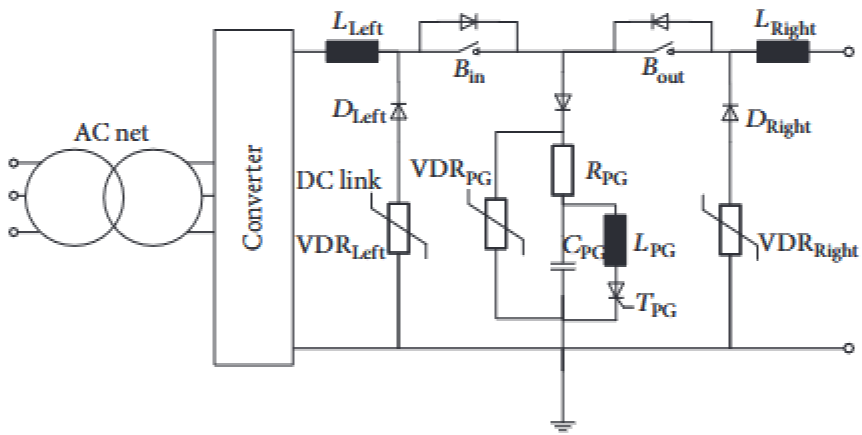


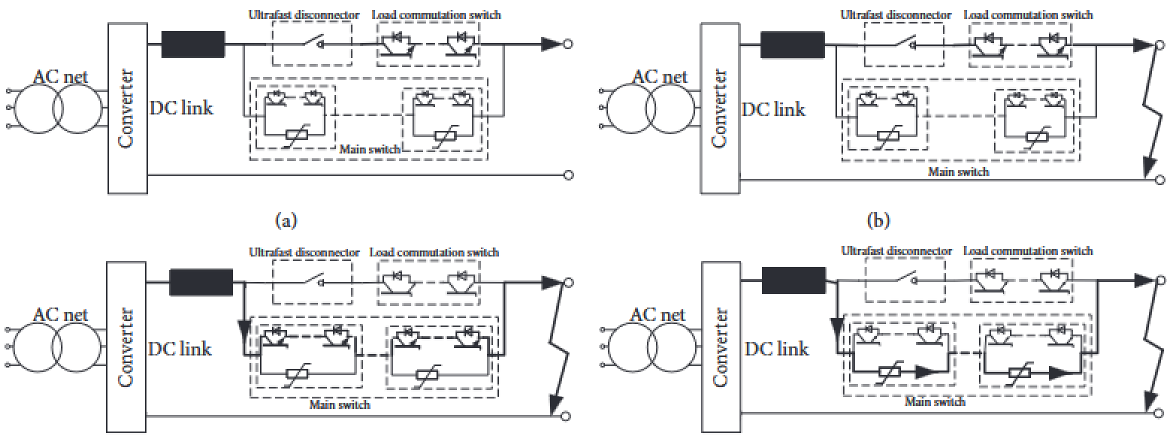
Figure 20. Structure of resonant DCCB

After a short delay (0.5 ms), the thyristor of the current pulse generator is triggered and a current pulse flows through the pulse generator branch and the two external MOVs. At this point, the current in the vacuum switch still flows through the plasma and then reverses and the current commutates to its parallel diode at the created zero crossing. Both vacuum switches are then switched off. After separation, the remaining energy of the line inductances must be absorbed. The input current will continue to flow to recharge the capacitor C_{PG} until the arrester VDR_{PG} becomes conductive.

5a-4.1.3 Hybrid HVDC breaker

To solve the high loss problem of the all-solid DCCB, reference [71] presents the hybrid DCCB. Figure *21* [71] shows the structure of hybrid DCCB. In this breaker, the DC current flows through the UFD and LCS during normal operation. The switching time of UFD is set to be 2 ms [74] and several IGBTs are used to construct the LCS. The total loss of this configuration is much lower than the all-solid DCCB.

At the inception of the fault, the LCS is blocked (Fig 21(b)) and the fault current commutates to the IGBTs in the main switch (Fig 21(c)). If there is no current flowing through the UFD, it can be turned off. When UFD is separated, the LCS can be turned on. The IGBTs in the main switch can be turned off after the turning-off of UFD. The fault current will commute to the arresters of the main switch and the energy will be consumed by these arresters (Fig 21(d)). At this point, the fault current can be cut off.



(a) (b) (c) (d)

Figure *21*. Structure and working principle of hybrid HVDC breaker. (a) Normal operation of hybrid HVDC breaker. (b) Short circuit faults occur and LCS is blocked. (c) Fault current commutates to main switch and UFD is turned off. (d) IGBTs in main breaker are blocked and fault current commutates to arrestors' branch

5a-4.1.4 Comparison of DCCBs

Each type of DCCB has certain advantages and disadvantages when compared to each other. Reference [71] describes the comparison between the three types of DCCBs when used in identical systems. For the comparisons, it is assumed the DCCBs are connected to a HVDC system where the DC voltage is 300 kV, the DC current is 1200 A and the DC reactor is 100 mH. Table 1 presents the comparisons between the three types of DCCBs.

Table 1. Advantage/disadvantage comparison of DCCB types

DCCB Type	**Advantage**	**Disadvantage**
All-solid	Fast activation speed (1.7 *μs)*. Low incremental current after detection	High hardware cost (300 IGBTs, 300 Diodes) and large power loss (990 kW)
Resonant	Virtually zero power loss. Relatively fast activation speed (0.5 *ms)*	High hardware cost (300 Diodes, 1200 thyristors). High overcurrent after activation
Hybrid	Lower power loss (12 kW). Lower hardware cost (300 IGBTs)	Slow activation speed (2 *ms*). High overcurrent after detection.

As shown in Table 1, each type of DCCB has its pros and cons. Determining which type to use will be left up to the specific needs of each HVDC system.

5a-5 Summary of main learning points

We summarize the main learning points of HVDC fault management and protection system addressed in this module.

1. There are three main types of HVCD fault types: Line-to-ground (LTG), Line-to-line (LTL) and Double line-to-ground (DLTG).
2. LTL faults are the most severe while LTG are the least. The DLTG fault is as severe as the LTL, but the chances of them occurring are miniscule.
3. Fault detection algorithms play a critical role in providing the required protection of an HVDC system to ensure reliability. Seven of the more commonly used detection methods are described. These methods include handshaking, traveling wave, transient, impedance based, wavelet transform based, natural frequency based and derivative.
4. HVDC requires a different type of circuit breaker, compared to HVAC, to interrupt fault current. Three designs are described. These designs include all-solid DCCB, resonant DCCB and hybrid DCCB.

Quiz Questions

1. **True or False:** A line-to-ground (LTG) fault is the most common type for fault as well as the most severe.

   (Answer: False, line-to-line (LTL) is the most severe)

2. **List the three stages that a Line-to-Line fault goes through.**

3. **1.**

   2.

   3.

   (Answer1. Capacitor discharge 2. Diode freewheeling 3. Grid current feeding)

4. **True or False:** A hybrid DCCB has a fast response time typically in the μs range.

   (Answer: False, hybrid DCCB response time is in the ms range)

5. **Which fault detection method provides an economical, highly reliable detection and isolation of faults in an MT-HVDC system based on local measurements which negates the need for communication systems?**
   A) Traveling wave
   B) Impedance based
   C) Handshaking
   D) Derivative

   (Answer: C - Handshaking)

6. **List the three categories of protection algorithms.**
   1.

   2.

   3.

   (Answer: 1. Single end / multi end 2. Unit / non-unit based 3. Communication / non-communication based)

7. **True or False:** The traveling wave transient is present at any point on a DC transmission line.

   (Answer: True)

8. **What is the most hazardous stage of a Line-to-Line fault?**

   (Answer: Diode freewheeling)

9. **What type of failure leads to DC collapse when a fault occurs in an AC transmission line connected to a CSC-based HVDC station?**

   (Answer: Commutation failure)

10. **True or False:** In a Line-to Ground fault, the fault tends to be long lasting

    (Answer: False, The LTG fault is typically a temporary fault)

11. **True or False:** DC faults in CSC-based HVDC line typically are not very severe.

    (Answer: True)

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