Symmetrical Fault Analysis

1.0 Definition

A *symmetrical* fault is a fault where all phases are affected so that the system remains balanced. A three-phase fault is a symmetrical fault. The other three fault types (line to ground, line to line, and two-line to ground) are called *unsymmetrical* or *asymmetrical* faults.

Because symmetrical faults result in balanced conditions, they may be analyzed using per-phase analysis.

2.0 Approaches

In these notes, we will describe a method for performing symmetrical fault analysis called the Thevenin approach. This approach provides insight into fault analysis, enhancing the engineer's intuition in regards to what causes high fault currents. We will later investigate a computer-based approach.

Before beginning, however, you should be aware that there are other equivalent ways of performing "intuitive" fault analysis. One way is called the "internal voltage" approach and is articulated in [1, pp. 383-390]. Another way makes use of the superposition principle is articulated in [2, pp. 284-286]. We begin with the simplest of examples.

3.0 Example

Consider a single generator supplying an R+jX load as shown in the one-line diagram of Fig. 1.

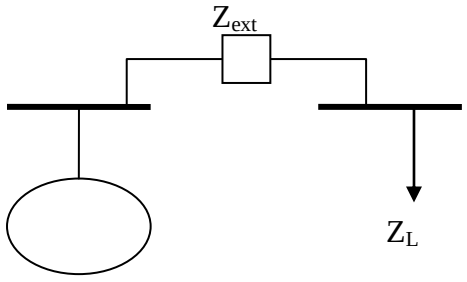

Fig. 1

Under steady-state, balanced conditions, the per-phase equivalent circuit appears as in the circuit diagram of Fig. 2.

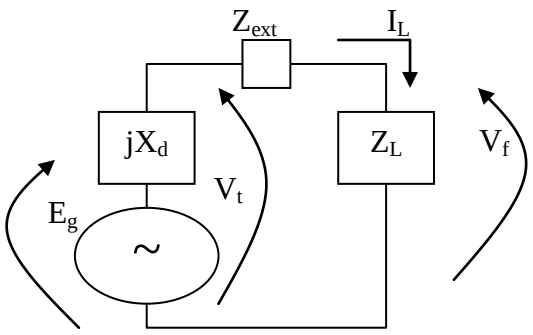

Fig. 2

The nomenclature in Fig. 2 is defined as:

- Z_{ext}: "external" impedance (transmission line impedance)
- Z_L: load impedance
- V_f: impedance at load bus (f denotes "fault" because this is the bus that will be faulted).
- E_g: steady-state internal gen voltage
- X_d: synchronous (steady-state) reactance
- I_L: load current
- V_t: generator terminal voltage

We refer to this as the steady-state model. Using KVL to express E_g, we have:

$$E_g = I_L \left[Z_{ext} + Z_L + jX_d \right] \qquad (1)$$

Let's consider a symmetrical fault on the load bus side of the transmission line, as shown in the one-line diagram in Fig. 3.

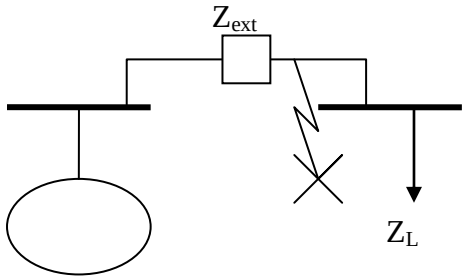

Fig. 3

We desire to compute the subtransient current I''. As a result, we need to utilize the subtransient impedances. Some assumptions that we will make are:

- All three phases fault to ground through identical impedances Z_f (this is the more general case and includes the "perfect" short circuit, sometimes called a "bolted" fault, where $Z_f=0$).
- Transmission lines are represented by their positive-sequence series reactance. Series resistance & shunt capacitance is neglected.

- Transformers are represented by their leakage reactances. Winding resistances, shunt admittances, and Δ-Y phase shifts are neglected.
- Synchronous machines (generators and motors) are represented by constant voltage sources behind subtransient reactances. Armature resistance, saliency and saturation are neglected.
- We assess only the steady-state current (we called it i_1 in previous notes) in terms of its RMS amplitude. The implication is that we may use standard phasor analysis, neglecting the DC offset. We can account for the influence of the DC offset by multiplying by an appropriate factor (~1.7).

Let's draw the per-phase circuit diagram corresponding to Fig. 3, given in Fig. 4.

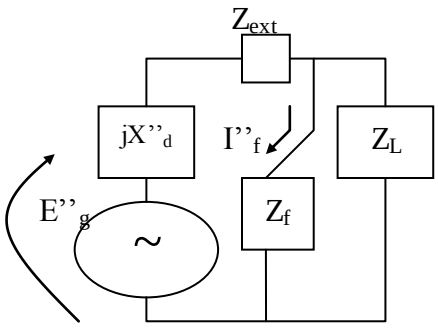

Fig. 4

This is an easy circuit to solve – if we know the subtransient internal voltage E''_g. Although we know (or can obtain from eq. (1)) E_g, the steady-state internal voltage, we do not know the subtransient internal voltage E''_g.

So how do we analyze the circuit of Fig. 4 if we do not know E''_g? As mentioned in the introduction, there are three different ways. But we will use only the Thevenin approach.

As its name implies, the Thevenin approach depends on application of Thevenin's theorem. To see this, consider redrawing Fig. 4 as in Fig. 5. Note that the two circuits are exactly the same.

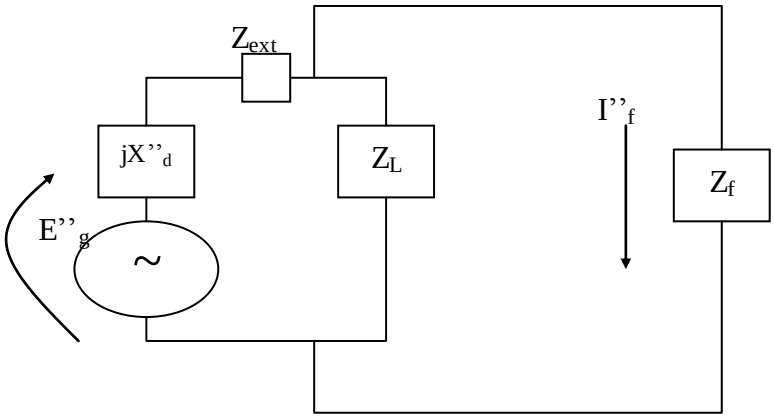

Fig. 5

The reason we have drawn Fig. 5 in this way is that I suspect it will be easier for you to see the Thevenin equivalent circuit looking into the original network from the faulted point. Figure 6 illustrates.

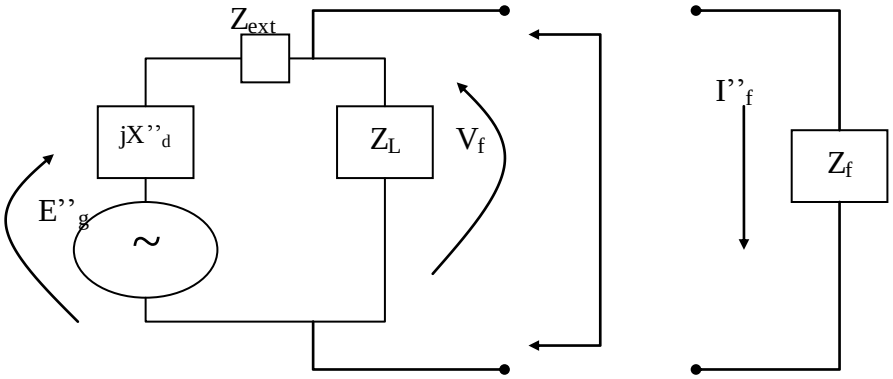

Fig. 6

The bracket with arrows shows the direction we "look" in obtaining the Thevenin.

Recall that in obtaining the Thevenin, we need to do two things:

1. Obtain the Thevenin impedance by "idling" all sources (short voltage sources, open current sources).
2. Obtain the Thevenin voltage by computing the voltage across the terminals into which we "look."

So the Thevenin impedance is the impedance of the network into which we look with all generators shorted.

In this case, we have just the one generator, so this impedance will appear as in Fig. 7.

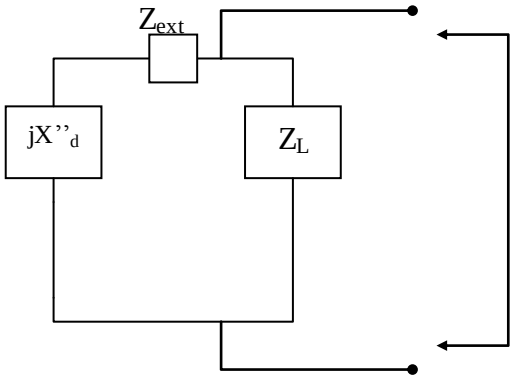

Fig. 7

From Fig. 6, the Thevenin voltage is the voltage at the fault point of the unfaulted

network. Interesting. This is just V_f, the voltage of the faulted bus but before the fault occurs. The upshot of this discussion is that determination of the Thevenin voltage is simple – it is just the pre-fault voltage at the fault point V_f !!! We can compute V_f from basic circuit analysis. In a large-scale network, we would obtain V_f from the output of a solved power flow case (of the unfaulted network).

Aside: Inspection of Fig. 6 suggests that we need to compute the fault point voltage using E''_g and X''_d instead of E_g and X_d. This might bother some of you, because Fig. 6 is the pre-fault circuit, and application of E''_g and X''_d must result in a pre-fault voltage of V_f, as we obtain when applying E_g and X_d. But how do we know this will be the case? We really do not know that, unless we require it to be so.

Therefore we will *define* E''_g to be that voltage which, when applied to the pre-fault,

subtransient (using subtransient generator reactances) network, results in the network voltages computed when we use E_g and X_d in the pre-fault network. In other words, we will require

$$V_f = E_g - I_L\left[Z_{ext} + jX_d\right]$$
$$= E_g'' - I_L\left[Z_{ext} + jX_d''\right] \quad (2)$$

It is easy to show using algebraic manipulation that (2) is true if

$$E_g - E_g'' = jI_L\left[X_d - X_d''\right] \quad (3)$$

That is, the difference between E_g and E''_g must be the same as the difference between X_d and X''_d scaled by I_L. Notice that

- When I_L=0, then E_g=E''_g, which is the condition used in the homework where we considered faulting an unloaded generator
- If X''_d<<X_d, then E''_g<E_g.

Back to discussion of Thevenin network:
The resulting Thevenin equivalent network, reconnected to the faulted part of the circuit, is shown in Fig. 8.

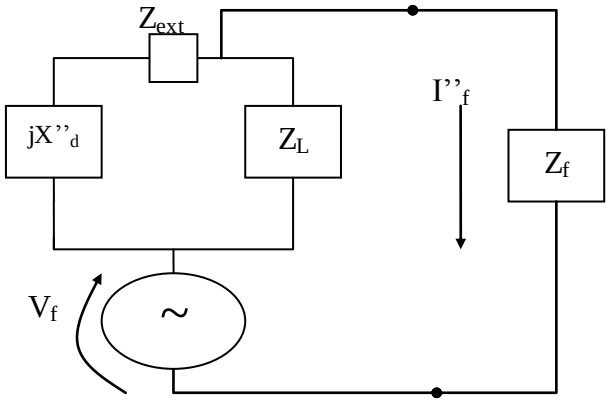

Fig. 8

Observe, in Fig. 8, that the Thevenin voltage V_f is in series with the fault impedance Z_f. Let's redraw the circuit to bring out this fact more clearly, as shown in Fig. 9.

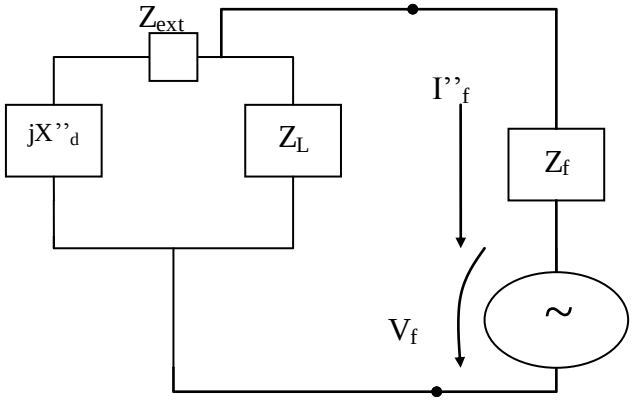

Fig. 9

Now let's step back and identify what we have in Fig. 9.

We have

- a voltage source (with voltage equal to the fault point voltage before the fault) in series with the fault impedance,
- connected from the fault point to ground
- with the rest of the network represented exactly as it is in the unfaulted condition
- except that all network sources are idled (all generators are shorted).

Figure 10 is exactly the same as Fig. 9, except drawn differently.

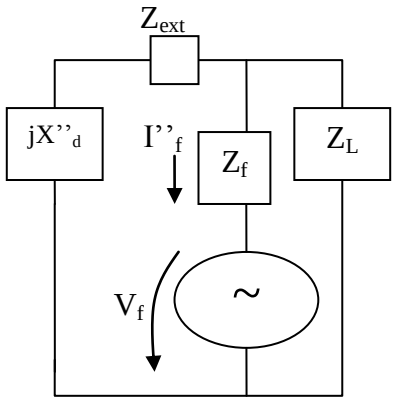

Fig. 10

As a result, we can see that I''_f is computed from:

$$I''_f = \frac{V_f}{Z_f + Z_{Thev}} \qquad (4)$$

where

- Z_f is the fault impedance
- Z_{Thev} is the Thevenin impedance seen looking into the unfaulted network from the fault point
- V_f is the voltage at the fault point of the unfaulted network.

In the case of this particular circuit, Z_{Thev} is given by:

$$Z_{Thev} = (Z_{ext} + jX''_d) // Z_L = \frac{(Z_{ext} + jX''_d)Z_L}{Z_{ext} + jX''_d + Z_L} \qquad (5)$$

In almost all cases, however, Z_L is very large relative to all transmission line and generator impedances. Paralleling a large impedance with a small one is almost like just having the small one by itself.

For example, in eq. (5), we see that if $Z_L >> Z_{ext} + jX''_d$, then

$$Z_{Thev} = \frac{(Z_{ext} + jX''_d)Z_L}{Z_{ext} + jX''_d + Z_L} \approx \frac{(Z_{ext} + jX''_d)Z_L}{Z_L} = Z_{ext} + jX''_d \quad (6)$$

It is in fact a quite reasonable approximation in fault analysis to assume all loads (except large motors) have infinite impedance, so that the only current flow is into the fault.

4.0 Motor Loads

There are three basic types of motors: synchronous motors, induction motors, and DC motors. DC motors of course may only be connected to an AC network through some kind of AC/DC rectifier circuit; this circuit effectively isolates the motor from affecting the AC network during faulted conditions.

On the other hand, synchronous motors and induction motors are directly connected to the AC network. Although during normal (unfaulted) conditions, the current flows into the motor (and therefore would not, of themselves, result in higher fault currents), during fault conditions, both types of motors look like a voltage source to the rest of the network and therefore contribute fault current just as a synchronous generator does. In fact, for purposes of fault analysis, a synchronous motor should be treated exactly as we treat a synchronous generator.

Induction motors, on the other hand, differ from synchronous machines in that they do not have an independent field source. As a result, induction motors do not sustain their internal voltage. Typically, induction motor contribution to fault current decays within a few cycles, before circuit breaker operation, and therefore are not generally of concern in fault studies. Reference [3] discusses further

the issue of representation of induction motors in fault studies.

5.0 Homework

The following two problems are due Monday, January 23.

1. Consider the two-bus system shown in Fig. 11. The two generators and transformers are assumed of equal rating – 300 MVA – which is the 3-phase base power for all pu unit data given in what follows.
   - Line has series reactance of 0.20 pu
   - Pre-fault bus voltage magnitudes are both 1.0 pu.
   - The generators are sharing the total real power load equally.
   - Assume that the prefault bus voltage at bus 1 is the reference.
   - The transformers both have leakage reactance of 0.12 pu.

- Both generators have subtransient reactance of 0.1 pu.
  a. For the pre-fault conditions, compute the pu real power consumed by each load, the pu real power delivered by each generator, the power angle δ, and the pu reactive power delivered by each generator.
  b. Compute the prefault currents into each load.
  c. Compute the fault current for a symmetric three-phase fault occurs on bus 1, with fault impedance $Z_f=0$.
  d. Compare the fault current computed in (c) with the pre-fault load currents computed in (b).

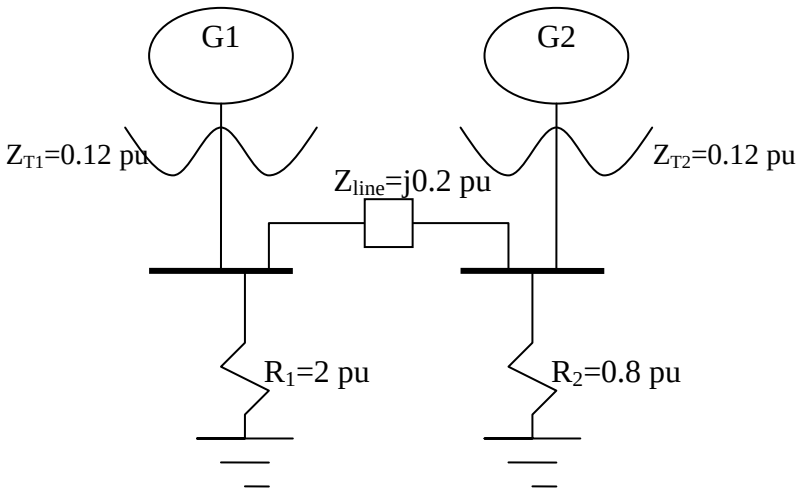

Fig. 11

2. The one-line diagram of a three-bus power system is shown in Fig. 12. Each generator is represented by an emf behind the transient reactance. All impedances are expressed in pu on a common 100 MVA base. Determine the fault current, the bus voltages, and the line currents *during the fault* when a balanced three-phase fault with fault impedance Z_f=j0.16 pu occurs on bus 1. Assume that all pre-fault bus voltages are 1.0 pu.

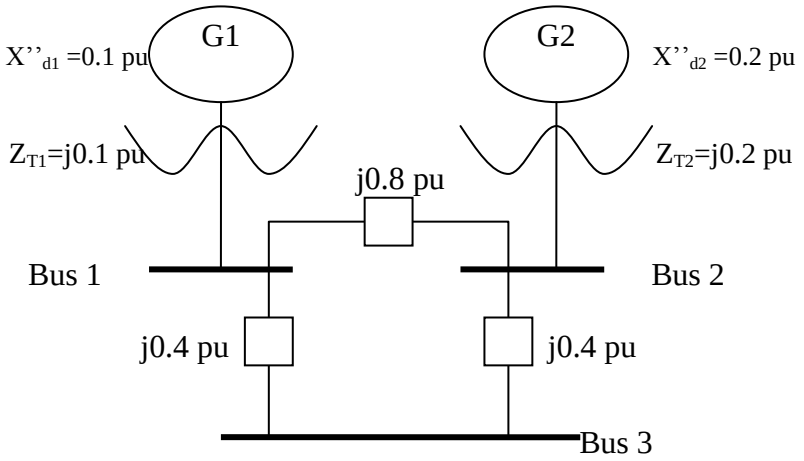

Fig. 12

[1] J. Grainger and W. Stevenson, “Power System Analysis,” 1994, McGraw-Hill.
[2] J. Glover and M. Sarma, “Power system analysis and design,” PWS Publishers, Boston, 1987.
[3] J. Blackburn, Protective Relaying, Principles and Applications,” Marcel Dekker, 1987.