EE 501 Lab 5 Common mode feedback (CMFB) circuit

Report due: Oct. 23th, 2014

Objectives:

1. Understand why CMFB circuits are needed and how they work to ensure robust operation.
2. Understand the advantages and disadvantages of different common-mode detector circuits.
3. Learn how to design CMFB amplifier.
4. Learn how to simulate the Common-mode loop gain and output swing range and how to setup fully differential amplifier close-loop testbench.

Conditions:

1. Load cap = 2pF at each output node
2. Output common mode voltage close to zero or middle point of output swing range.
3. Power supply +2.5, -2.5V

Task & Steps:

Task A:

1. A former graduate student was trying to design a folded cascode two stage op amp. As shown in Fig 1, at first the circuit was biased by current mirror. After the amplifier was designed, he claimed that with finite resolution of current mirror transistor sizes, it is impossible to make every transistor in saturation region. Instead, he added an independent voltage supply at "VB" and swept it. A voltage, which corresponds to 12 significant-digits, was found.
   a. Connect the biasing voltage to the "CMFB" node of the amplifier and build a test-bench as Fig 2. Verify the student's design and find DC gain, GBW and phase margin of that circuits. For "stb" simulation, refer to Appendix A.
   b. If the biasing voltage is changed by 10mV by the process variation. What happens to the circuit? What will the circuit be when the widths of the current mirror transistors change 0.15um by other design requirement or the supply voltage changes from ±2.5V to ±2.4V.
   c. Is it a good strategy to use this voltage to biasing the circuit? Explain the above phenomenon and conclusions.
2. The solution to this problem is to use feedback to the correct biasing voltage. The circuit is shown in Fig 3. You can also change the given amplifier to introduce the feedback node (for example, split the load NMOS transistors into four identical transistors with middle two ones biased by the current mirror and the other two ones connected to the feedback node as shown in Fig 4).

   a. Voutn and Voutp are the amplifier's differential outputs. Two identical resistors sense the common-mode voltage at the middle point. The swept voltage "Lab5_VB" is added at the bottom and "vcvs", whose gain is usually smaller than 0dB, is used to generate variation of the biasing voltage. 0V is the desired output common-mode voltage. Determine the sign of the gain in "vcvs" and explain why.
   b. In this case, when the input common-mode voltage changes, what happens to the output common-mode voltage? Record the output voltage of the "vcvs", V_{CMFB}.
3. Run "stb" simulation to find the DC gain, GBW, UGF, and phase margin of differential path.
4. Run "stb" simulation for the common-mode signal and change the gain of "vcvs" (usually by decreasing the gain) to make sure the CMFB loop is stable. Record the CMFB DC loop gain, GBW, UGF and phase margin.

Task B:

1. In previous task, we use two identical resistors to sense the commom-mode voltage. Sweep the resistance from 2K to 100K and record the DC gain, GBW, UGF and phase margin, explain why.
2. From last step you should notice the loading effect of resistive common-mode detector. To eliminate this loading effect, we could use the active common-mode detector, the circuit is shown in Fig 5. Design the amplifier and replace the previous detector and "vcvs" (testbench shown in Fig 6), then repeat task A.3. The output DC voltage should be close to the biasing voltage of "Lab5_VB". (Note: the design strategy is shown in the CMFB lecture slides, page 30 and keep in mind that the output operating point should be in the middle of output swing range, not 0)
3. Use the designed active common-mode detector in test-bench as shown in Fig 6 and find the CMFB loop gain, UGF, and phase margin. Tune the CMFB amplifier until the PM is larger than 50 degree. (The UGF of the CMFB loop is typically around 5~10 times lower than the differential mode UGF.)
4. Report the DC gain, GBW, UGF and phase margin of both common-mode and differential signal paths.
5. Use the test-bench shown in Fig 6 to simulate the output swing range of the amplifier. (The method is shown in video, please watch it if you don't know the detail). Compare the output swing range between two different common-mode detectors (Resistive and active). Explain why.

Task C:

1. From previous work, we could conclude that the resistive common-mode detector will reduce the DC gain, and the active common-mode detector will have range reduction. To eliminate these two drawbacks, we could use the leaky capacitance common-mode detector as shown in Fig.7. However, the resistance also needs to be large enough to reduce loading effect. Instead of using resistors, we could use the off-state transistors to replace the resistors, as shown in Fig.8. Explain how it works and why it could replace resistors.
2. Design a CMFB "amplifier" or attenuator (an example is shown in Fig 9 and you can use other structures). The output DC voltage should be close to the biasing voltage of "Lab5_VB".

3. Use the designed CMFB amplifier in test-bench as shown in Fig 10 and find the CMFB loop gain, UGF, and phase margin. Tune the CMFB amplifier until the PM is larger than 50 degree. (The UGF of the CMFB loop is typically around 5~10 times lower than the differential mode UGF.)
4. Report the DC gain, GBW, UGF and phase margin and output swing range of both common-mode and differential signal paths.

In conclusion, the designed amplifier should have the following characteristics,

1. The output common-mode voltage can be determined by the reference voltage (the other input node of the CMFB amplifier, in this case which connects to ground or middle point of swing range).
2. In addition to the DC gain, GBW and power consumption as required in your particular design job, the amplifier should have a good stability in differential signal path (phase margin>50°).
3. CMFB circuit is in nature an amplifier in close loop which means it must also be stable to ensure the design valid and this is also interpreted as good phase margin (>50°).

Bonus:

Try to find some other path to introduce the common-mode feedback, explain the method and give the simulation results.

Figures:

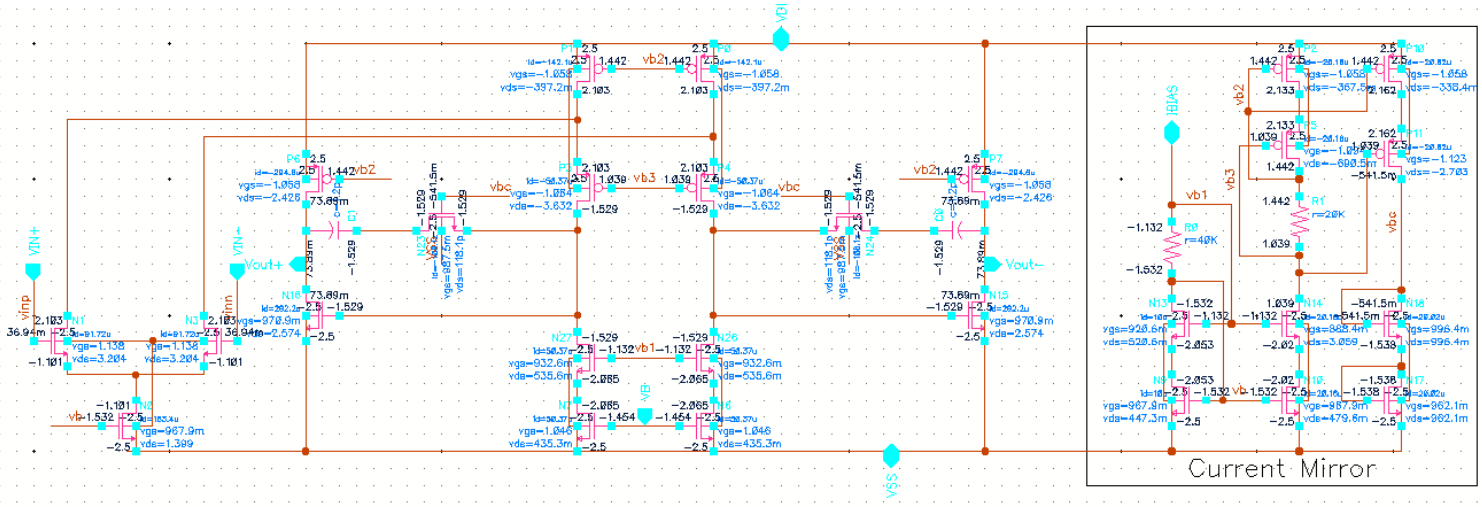


Fig 1

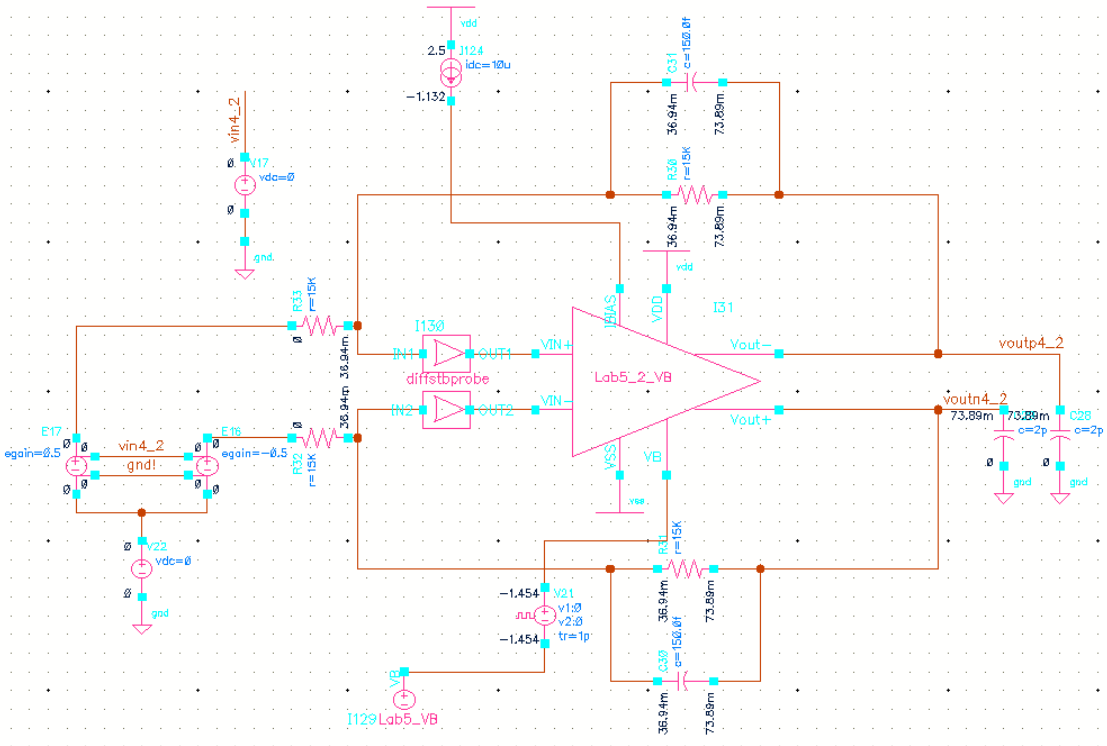


Fig 2

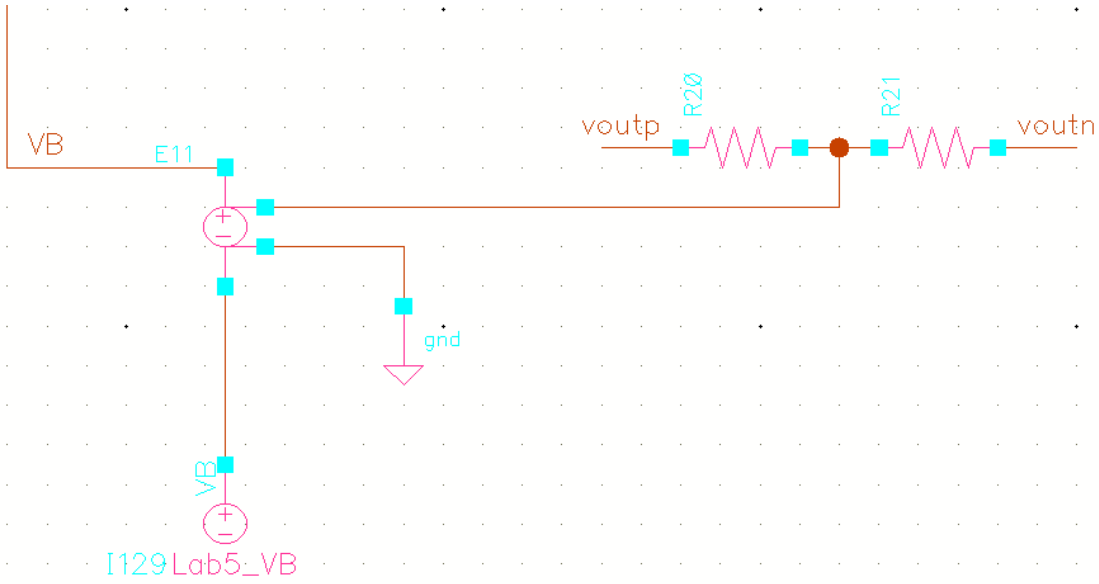

VB
E11
voutp
R20
R21
voutn
gnd
VB
I129 Lab5_VB

Fig 3

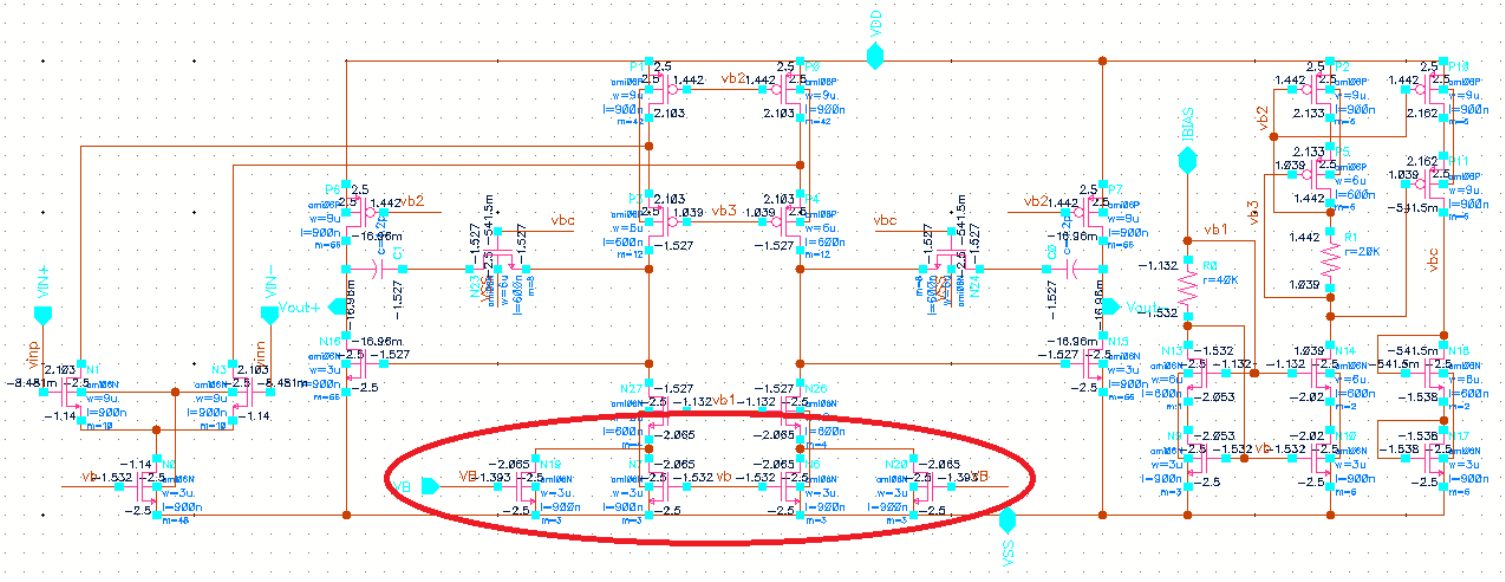
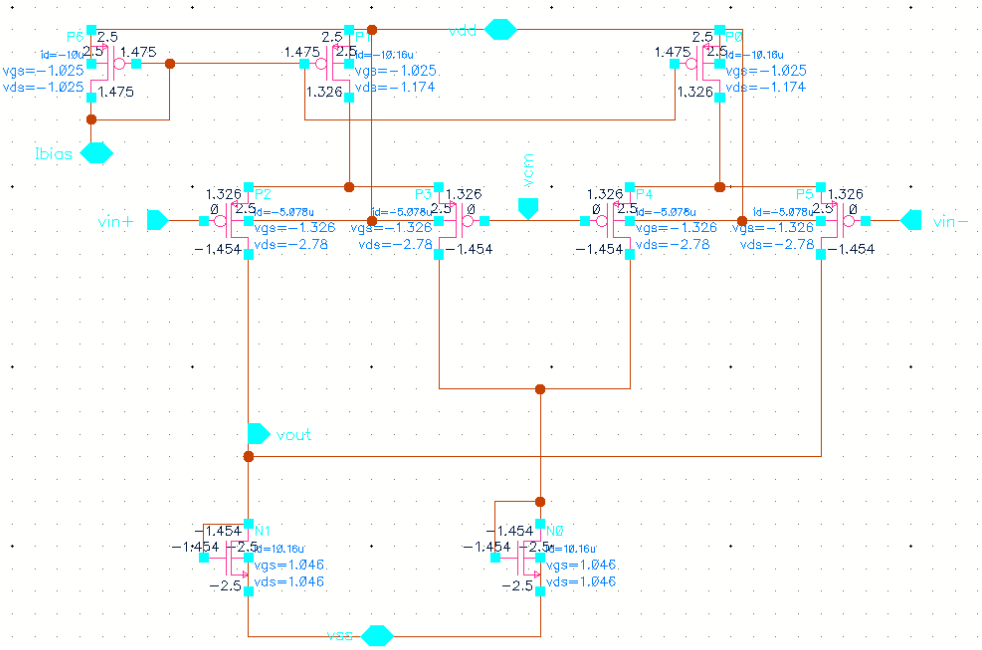

VDD
VSS
VIN+
VIN-
Vout+
Vout-
vinp
vinn
vb1
vb2
vb3
vbc
IBIAS
VB
R0
r=42K
R1
r=20K
C0
C1

Fig 4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Ibias
vcm
vin+
vin−
vout
vss
P6
P7
P8
P2
P3
P4
P5
N1
N0

Fig 5

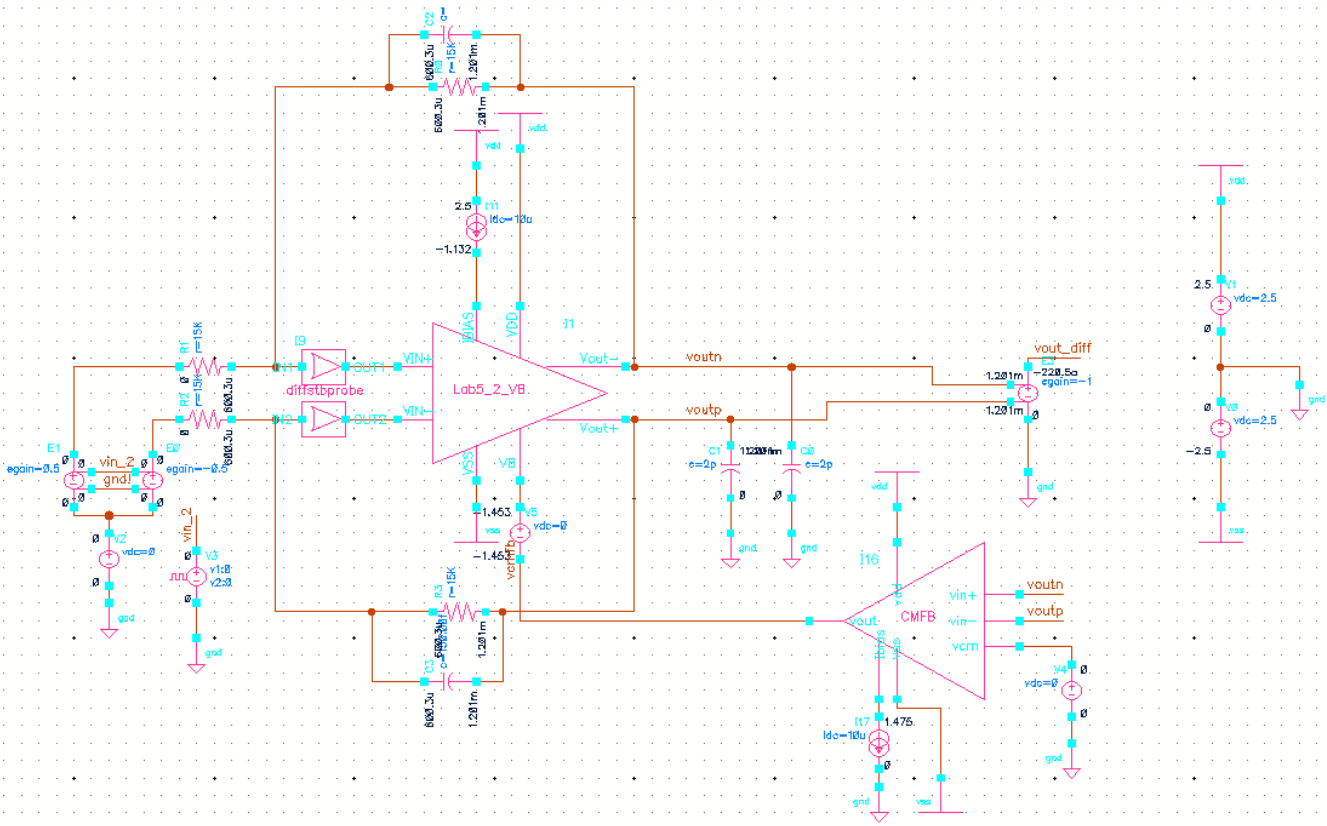
vdd
vout_diff
voutn
voutp
vin+
vin−
vcm
CMFB
Lab5_2_VB
diffstbprobe
vin_2
gnd!
gnd

Fig 6

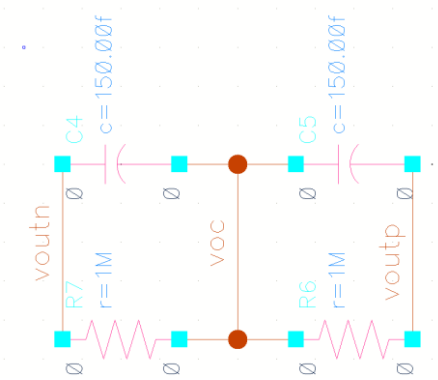

Fig 7

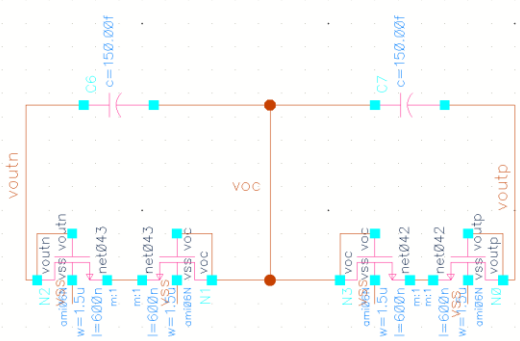

Fig 8

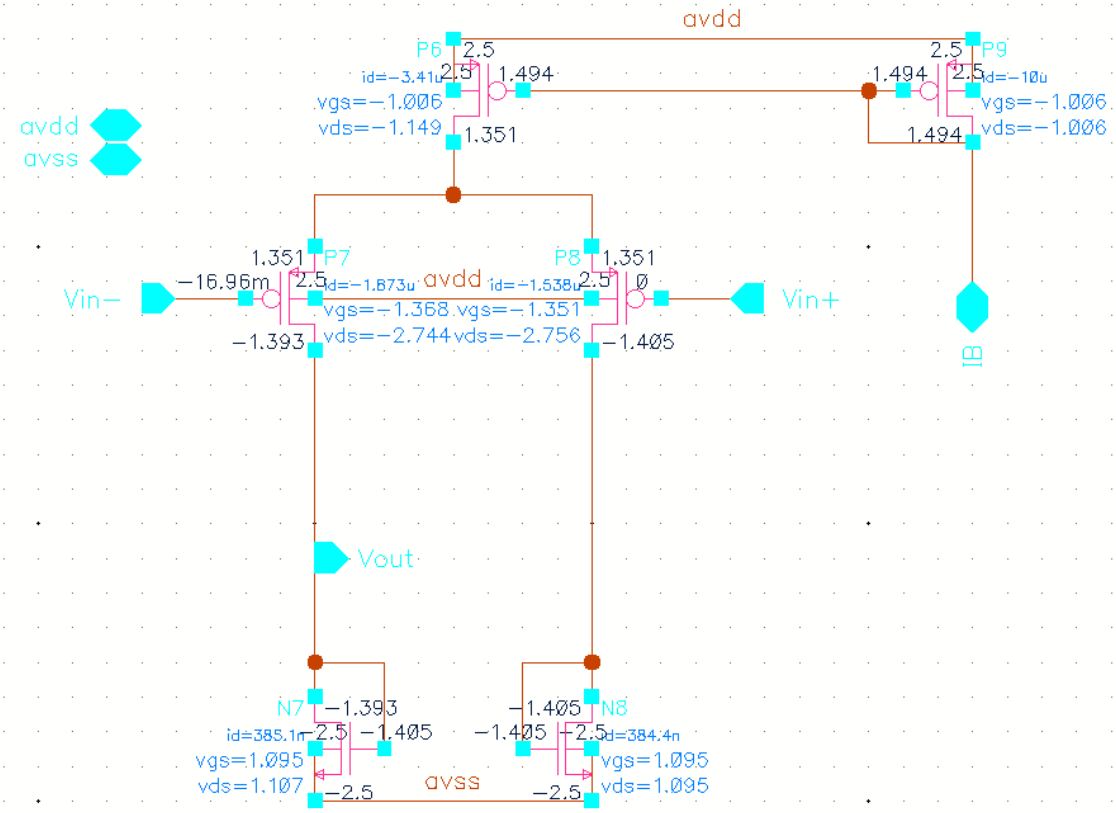

Fig 9

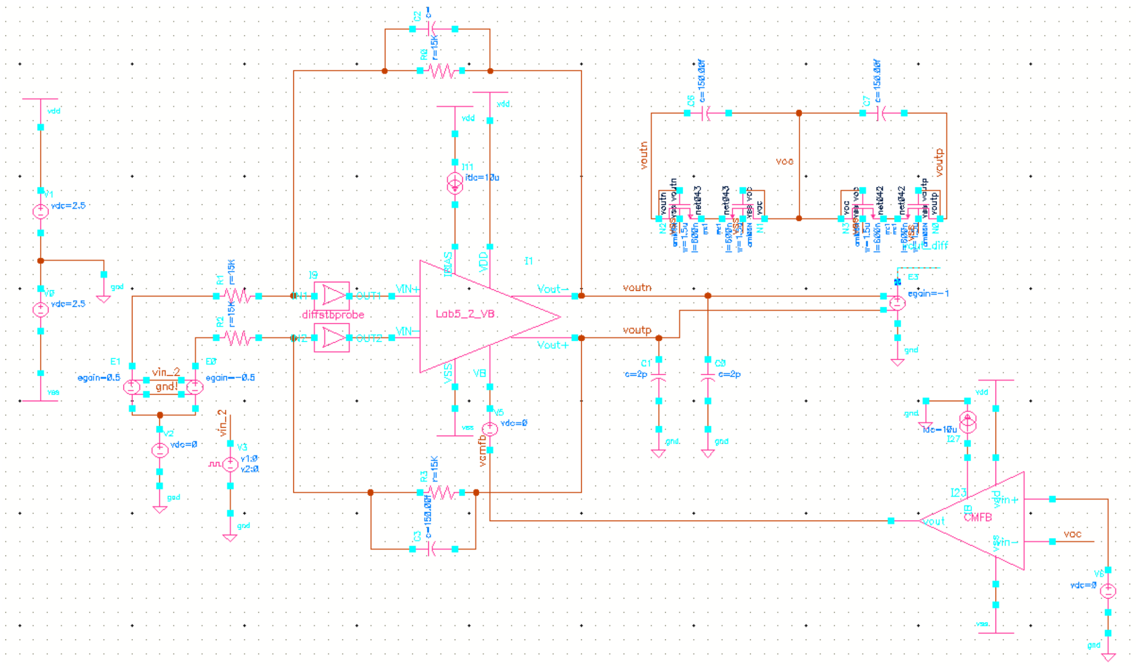

Fig 10

Appendix A:

"stb" simulation setup for fully differential amplifier

1. For Fully differential amplifier, there are two input/output nodes. "diffstbprobe" can help find the differential signal.

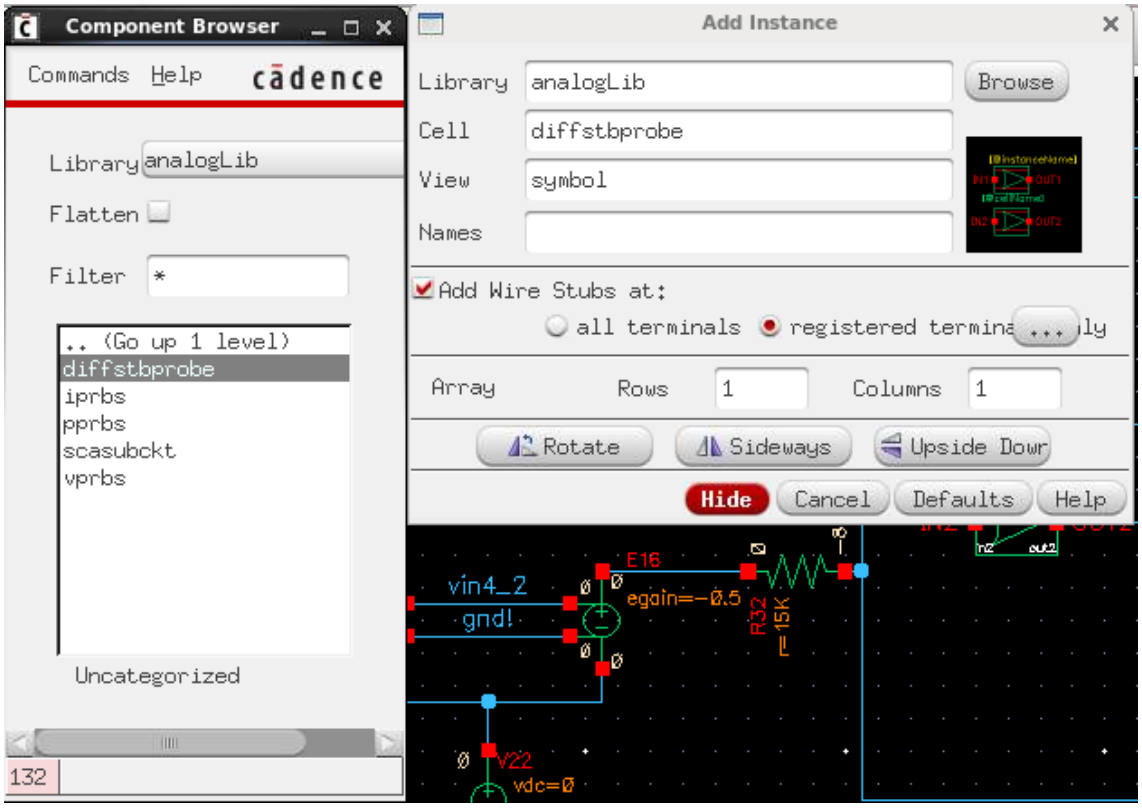

Fig A.1

2. Setup "stb" simulation by choosing "probe instance" as your "diffstbprobe" component.

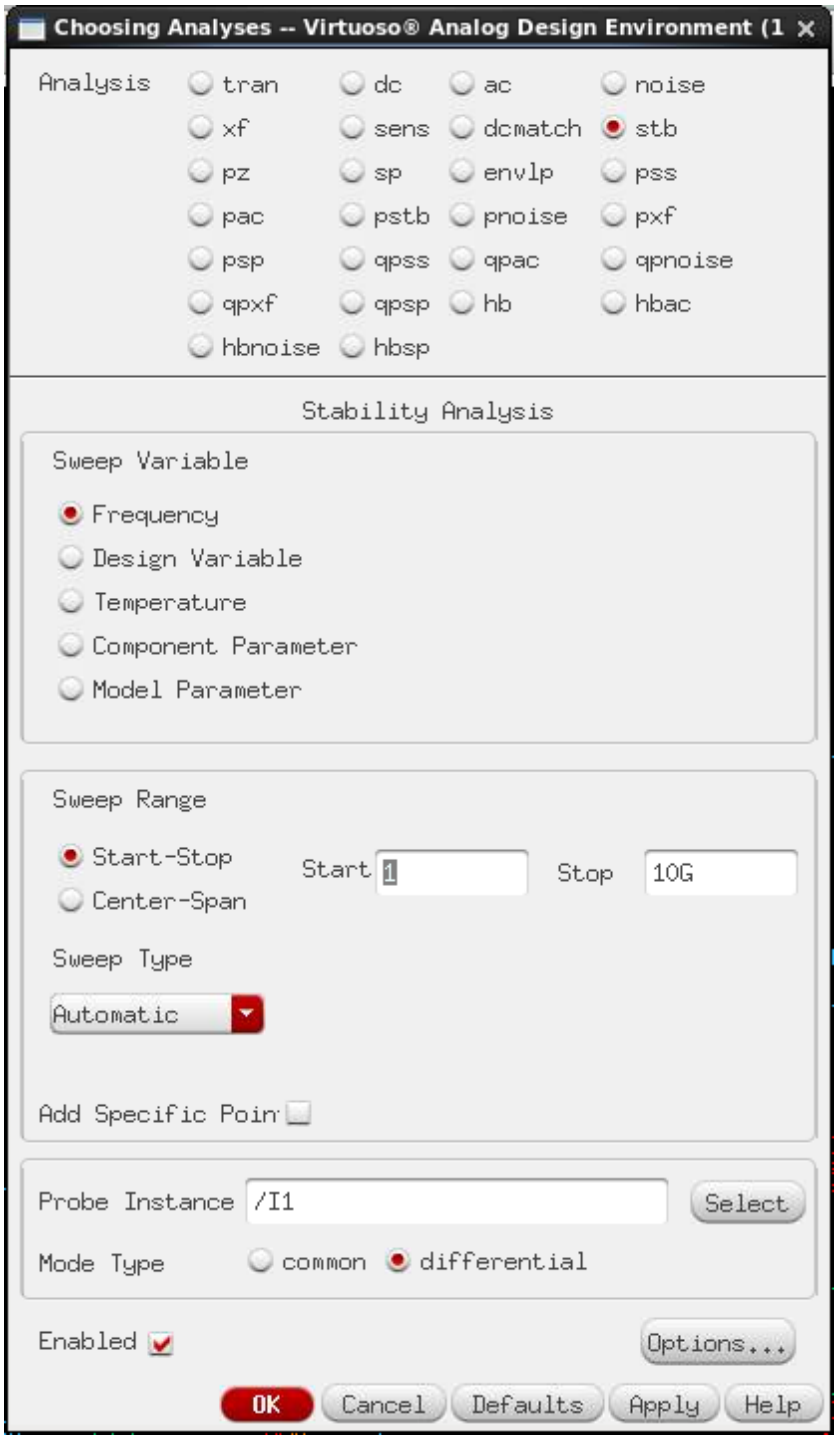

Fig A.2

3. To test the CMFB loop, add a “vdc” between the CMFB node of the op amplifier and the output of the CMFB amplifier as shown in Fig 3.
4. Change the setup of “stb” to choose the “Probe Instance” as the “vdc” component and rerun the simulation.