Rethinking the Wirelength Benefit of 3D Integration

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***Abstract*—To sustain the pace of integration density improvement, 3D IC technology is hailed as a "Beyond Moore" driver. It has been demonstrated to have great potential to diminish footprint, reduce interconnect delay, promote system performance, decrease power consumption and facilitate integration of heterogeneous processes. Besides, it is commonly cited as a means of reducing lateral wirelength. Some early theoretical and experimental studies have also shown that 3D IC can significantly reduce lateral wirelength. However, the effect of through-silicon via (TSV) area overhead on the wirelength has been largely overlooked. In this paper, we derive a mathematical upper bound on the wirelength benefit of placing a circuit in 3D that takes the TSV area overhead into account. For a set of IBM placement benchmarks scaled to the 32nm process, we show that 3D integration cannot help to reduce the wirelength under current TSV technologies.**

***Index Terms*—3-D IC, through-silicon via, wirelength, mathematical upper bound, 3-D placement**

I. Introduction

Lately there has been intense interest in 3D ICs in the semiconductor industry. 3D integration is being hailed as a "Beyond Moore" driver which promises to provide further increase in integration density. A 3D IC is made up of an IC stack with very short vertical interconnections between adjacent dies by means of through-silicon vias (TSVs). There are a lot of potential advantages to go 3D including smaller footprint, reduced interconnect delay, higher system performance, and lower power consumption. Moreover, heterogeneous technologies can be comfortably integrated in a die stack. One can choose the most suitable process to manufacture each die to optimize the cost and performance. The simplest example is stacking memory and CPU.

There were a number of theoretical studies on the wirelength benefit of 3D ICs [1]–[3]. They all predicted that the interconnect length would be greatly reduced when a standard cell circuit was spread across multiple layers. The wirelength reduction originates from the usage of TSVs as vertical connections which are very short. But these analysis typically had an implicit assumption that the TSVs could be made extremely small, and hence the effect of TSV size was ignored in the analyses. Similarly, the substantial wirelength reduction reported by some experimental studies for standard cell circuits [4]–[6] also ignored the area overhead of TSVs. However, it has become evident that the TSV area overhead is actually non-negligible.

TSV diameter may range from tens of microns down to nearly a micron [7]. Though the smallest TSV diameter claimed is about 1μm, there are still many manufacturing and reliability challenges in making TSVs with small diameter and low height-to-diameter ratio, which requires extremely thin dies. These challenges make it hard to get good yield. Filling TSVs without voids is difficult even for diameter of 5 to 6μm [8]. Besides, the thermo-mechanical stress caused by TSVs is known to severely impact the carrier mobility of nearby devices [9], [10]. So, there needs to be a keep-out zone around a TSV. As a result, a TSV cell (including keep-out zone) is much larger than an average standard cell. [11] estimated that the TSV cell dimension is about 5 to 10 times the height of a standard cell in 32nm technology.

The non-negligible TSV area overhead will increase the separation of cells and negatively impact the lateral wirelength. Thus, we have to ask again if 3D integration is really beneficial to the total wirelength, say, for the 32nm process. Of course, one possibility is to perform an empirical study by placing a set of circuits both in 3D and in 2D and see if 3D integration can reduce the wirelength. However, the conclusion is easily affected by the qualities of the 3D and 2D placers used. 3D EDA tools are not mature yet, a negative conclusion may be due to a poor 3D placement approach. So, in this paper, we mathematically derived an upper bound on the wirelength benefit of placing a circuit in 3D. Even if 3D placement tools continue to improve, the wirelength benefit of placing a given circuit in 3D will never exceed the theoretical upper bound derived.

Our work is distinct from the existing works on 3D-wirelength prediction [1]–[3], [12] that use stochastic approaches based on Rent's rule. These works target to predict the point-to-point wirelength distribution of a homogeneous random gate network placed in a regular 3D gate array-like structure given the number of gates and the values of the Rent's parameters of the network. Though the 3D wirelength of a circuit can be estimated by substituting the estimated values of the Rent's parameters, there is no guarantee if it will underestimate or over-estimate, and by how much. So we cannot be sure if a circuit's 3D wirelength is really better(worse) than its 2D wirelength even when the 3D wirelength estimate is smaller(larger) than the 2D wirelength estimate by Rent's rule. Another limitation is that the number of TSVs used by a 3D placement cannot be changed (unless we change the Rent's parameters which implies changing the circuit).

In this work, we derive a TSV-aware mathematical upper bound on the wirelength benefit of placing a circuit in 3D. It is not based on Rent's rule and does not need to assume placing a homogeneous random gate network to a regular 3D gate array-like structure or use estimated Rent's parameters. In addition, the number of TSVs used and the TSV size in the 3D placement of a given circuit are adjustable parameters. We performed a study on a set of IBM benchmarks [13]

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Symbol	Meaning
m	# of layers in 3D IC
W	width of 3D layout
H	height of 3D layout
L_{3D}	total wirelength of the given 3D layout
L_i^x	wirelength along x-direction in layer i of 3D layout ($1 \le i \le m$)
L_i^y	wirelength along y-direction in layer i of 3D layout ($1 \le i \le m$)
L_i^z	wirelength along z-direction in layer i of 3D layout ($1 \le i \le m$)
L_{2D}	total wirelength of the constructed 2D layout
L_{2D}^*	total wirelength of a good 2D layout
α_i	width reduction factor of layer i after removing TSVs ($1 \le i \le m$)
n_i^v	# of TSVs in layer i ($1 \le i \le m$)
μ	area utilization in 2D and 3D layouts
ρ_i	% of area occupied by TSV cells in layer i ($1 \le i \le m$)
ρ	avg. % of area occupied by TSV cells in upper $m-1$ layers
a^v	area of one TSV cell
β	a lower bound of $L_i^x / \left(\sum_{i=1}^m (L_i^x + L_i^y)/2m\right)$ for $2 \le i \le m$
n^c	total # of standard cells
a^c	average area of one standard cell

TABLE I
NOTATIONS FOR WIRELENGTH BENEFIT ANALYSIS.

scaled to a 32nm process. We found that under current TSV technologies the total wirelength is expected to get worse rather than better with 3D integration. If TSV cell size can be diminished and made comparable with that of standard cell, 3D integration may help reduce the total wirelength but the potential reduction is less than what most people expected in the past.

II. UPPER BOUND ON WIRELENGTH BENEFIT

In this section, we derive a theoretical upper bound on the wirelength benefit of placing a given circuit in 3D compared to a good 2D placement. The notations that we use in our analysis are listed in Table I. In our discussion below, we assume that the TSV cell area includes the keep out zone required by a TSV. We assume that front-to-back bonding (see Figure 1) is used. In other words, TSVs will occupy some area in the upper layers but not the first layer.

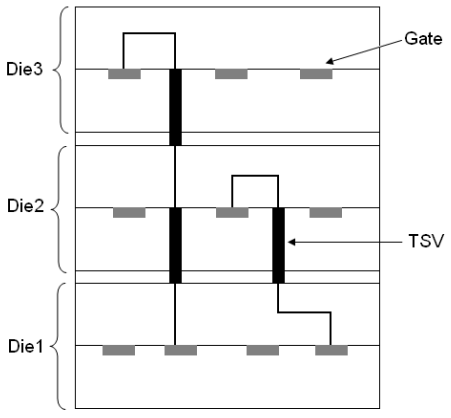

Fig. 1. Front-to-back bonding.

Suppose we have a 3D layout of a circuit with m layers that satisfies whatever required constraints like cells of the same block must be kept together in the same layer. Let W and H be the width and the height of the 3D layout, respectively. Assume without loss of generality that $W \le H$. Let L_{3D} be its wirelength. Based on the 3D layout, we can construct a 2D layout of the circuit with wirelength L_{2D} by simply arranging the layers side-by-side as shown in Figure 2. In the constructed 2D layout, TSVs in the upper layers are removed and the layers are compacted along the x-direction. Note that L_{2D} based on our simple construction is considered to be a loose upper bound on the wirelength of a good 2D placement L_{2D}^*. The placement is not optimized after the layout is transformed into 2D. The shape of the 2D layout is also far from a square. Typically, if we generate a 2D layout with a square shape from scratch, the wirelength would be much better. Comparing with L_{3D}, on one hand, L_{2D} may be more because each TSV will become a very long wire in the 2D layout. On the other hand, L_{2D} may be less because wirelength along the x-direction can be reduced due to compaction. In the analysis below, we show theoretically that L_{3D} cannot be much better than L_{2D}, let alone that of a good (or even optimal) placement L_{2D}^*.

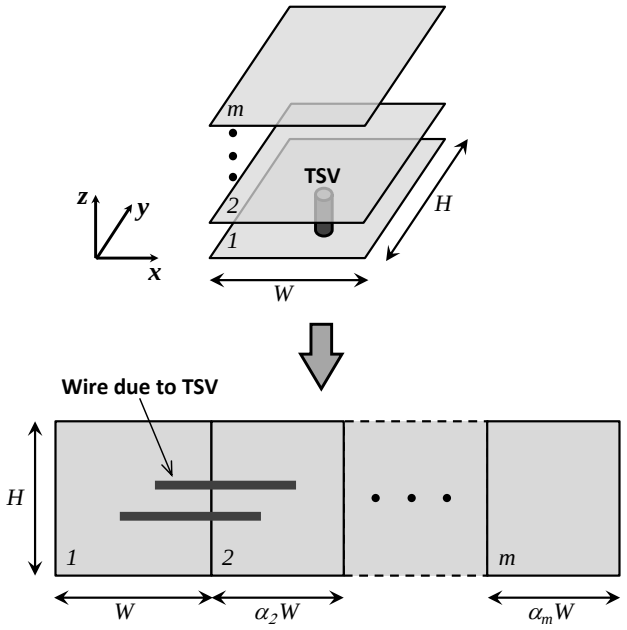

Fig. 2. Construction of 2D layout based on a given 3D layout.

Consider layer i of the 3D layout ($1 \le i \le m$). Let L_i^x, L_i^y and L_i^z be the wirelength along x-, y- and z-direction, respectively. In other words

$$L_{3D} = \sum_{i=1}^{m} (L_i^x + L_i^y + L_i^z). \quad (1)$$

When the 3D layout is flattened, assume the width of layer i is reduced by a factor of α_i after the TSVs are removed. (Note that $\alpha_1 = 1$ as there is no TSV in layer 1.) As a result, the wirelength along x-direction is scaled by the factor α_i while the wirelength along y-direction is unchanged. Let n_i^v be the number of TSVs in layer i. These TSVs are connecting to layer $i-1$ and each is stretched into a wire of length $(\alpha_{i-1}/2 + \alpha_i/2) \times W$ on average during flattening. Then the

total wirelength of the 2D layout is

$$L_{2D} = \sum_{i=1}^{m} (\alpha_i L_i^x + L_i^y) + \sum_{i=2}^{m} n_i^v \left(\frac{\alpha_{i-1} + \alpha_i}{2} \right) W. \quad (2)$$

Let μ be the area utilization (including standard cells and TSV cells) in 2D and 3D layouts. Let ρ_i be the percentage of area occupied by TSV cells in layer i. (Note that $\rho_1 = 0$ and $0 \le \rho_i \le \mu$ for $2 \le i \le m$.) The total area of standard cells in layer i should equal $\mu \times WH - \rho_i \times WH$. Taking white space into account, the area of layer i after removing TSVs should then be $(\mu - \rho_i) \times WH/\mu$. Hence, the width reduction factor of layer i after removing TSVs should be

$$\alpha_i = 1 - \rho_i/\mu. \quad (3)$$

Let a^v be the area of one TSV cell. The total TSV cell area of layer i can be expressed as both $n_i^v a^v$ and $\rho_i \times WH$. Hence

$$n_i^v = \rho_i WH/a^v. \quad (4)$$

By substituting (3) and (4) into (2)

$$\begin{aligned} L_{2D} &= \sum_{i=1}^{m} \left(L_i^x + L_i^y - \frac{\rho_i}{\mu} L_i^x \right) \\ &+ \sum_{i=2}^{m} \frac{\rho_i WH}{a^v} \left(1 - \frac{\rho_{i-1}}{2\mu} - \frac{\rho_i}{2\mu} \right) W. \end{aligned} \quad (5)$$

Let ρ be the average percentage of area occupied by TSV for the upper $m-1$ layers, i.e.,

$$\rho = \frac{\sum_{i=2}^{m} \rho_i}{m-1}. \quad (6)$$

By substituting (6) into (5) and rearranging, we get

$$\begin{aligned} L_{2D} &= \sum_{i=1}^{m} (L_i^x + L_i^y) - \frac{1}{\mu} \sum_{i=1}^{m} \rho_i L_i^x \\ &+ \frac{WH}{a^v} W \left((m-1)\rho - \sum_{i=2}^{m} \frac{\rho_{i-1}\rho_i}{2\mu} - \sum_{i=2}^{m} \frac{\rho_i^2}{2\mu} \right). \end{aligned} \quad (7)$$

Let β be a lower bound of the ratio of the wirelength along x-direction in any upper layer to the average over both directions and all layers, i.e.,

$$\beta \le \frac{L_i^x}{\sum_{i=1}^{m} (L_i^x + L_i^y)/2m} \text{ for } 2 \le i \le m. \quad (8)$$

Typically, the wires are evenly distributed among the layers and in both directions. Thus, β is close to 1 in practice. Based on $\rho_1 = 0$, (8) and (6), we get

$$\begin{aligned} \sum_{i=1}^{m} \rho_i L_i^x &\ge \left(\sum_{i=2}^{m} \rho_i \right) \times \left(\frac{\beta}{2m} \sum_{i=1}^{m} (L_i^x + L_i^y) \right) \\ &= \frac{(m-1)\rho\beta}{2m} \sum_{i=1}^{m} (L_i^x + L_i^y). \end{aligned} \quad (9)$$

Let n^c be the total number of standard cells and a^c be the average area of one standard cell in the circuit. The total die area of 3D layout can be expressed as both $m \times WH$ and $(n^c a^c + \sum_{i=2}^{m} \rho_i WH)/\mu$. Hence

$$m \times WH = \left(n^c a^c + \sum_{i=2}^{m} \rho_i WH \right) / \mu.$$

By substituting (6) and rearranging,

$$WH = \frac{n^c a^c}{m\mu - (m-1)\rho}. \quad (10)$$

As $W \le H$, (10) implies

$$W \le \sqrt{\frac{n^c a^c}{m\mu - (m-1)\rho}}. \quad (11)$$

Based on Jensen's inequality [14]

$$\frac{\sum_{i=2}^{m} \rho_i^2}{m-1} \ge \left(\frac{\sum_{i=2}^{m} \rho_i}{m-1} \right)^2.$$

By substituting (6) into the inequality, we have

$$\sum_{i=2}^{m} \frac{\rho_i^2}{2\mu} \ge \frac{(m-1)\rho^2}{2\mu}. \quad (12)$$

Based on $\rho_{i-1}\rho_i \ge 0$ for all i, (9), (10), (11) and (12), we can upper bound L_{2D} in (7) as below

$$\begin{aligned} L_{2D} &\le \sum_{i=1}^{m} (L_i^x + L_i^y) - \frac{(m-1)\rho\beta}{2m\mu} \sum_{i=1}^{m} (L_i^x + L_i^y) \\ &+ \frac{1}{a^v} \left(\frac{n^c a^c}{m\mu - (m-1)\rho} \right)^{\frac{3}{2}} \left((m-1)\rho - \frac{(m-1)\rho^2}{2\mu} \right). \end{aligned}$$

As $\sum_{i=1}^{m} (L_i^x + L_i^y) \le L_{3D}$, we get

$$\begin{aligned} L_{2D} &\le L_{3D} \times \left(1 - \frac{(m-1)\rho\beta}{2m\mu} \right) \\ &+ \frac{(m-1)\rho}{a^v} \left(\frac{n^c a^c}{m\mu - (m-1)\rho} \right)^{\frac{3}{2}} \left(1 - \frac{\rho}{2\mu} \right). \end{aligned}$$

Therefore

$$1 - \frac{L_{3D}}{L_{2D}} \le 1 - \frac{1 - \frac{(m-1)\rho}{a^v \times L_{2D}} \left(\frac{n^c a^c}{m\mu - (m-1)\rho} \right)^{\frac{3}{2}} \left(1 - \frac{\rho}{2\mu} \right)}{1 - \frac{(m-1)\rho\beta}{2m\mu}}.$$

As $L_{2D} \ge L_{2D}^*$, so

$$1 - \frac{L_{3D}}{L_{2D}^*} \le 1 - \frac{L_{3D}}{L_{2D}}$$

and

$$\begin{aligned} &1 - \frac{1 - \frac{(m-1)\rho}{a^v \times L_{2D}} \left(\frac{n^c a^c}{m\mu - (m-1)\rho} \right)^{\frac{3}{2}} \left(1 - \frac{\rho}{2\mu} \right)}{1 - \frac{(m-1)\rho\beta}{2m\mu}} \\ &\le 1 - \frac{1 - \frac{(m-1)\rho}{a^v \times L_{2D}^*} \left(\frac{n^c a^c}{m\mu - (m-1)\rho} \right)^{\frac{3}{2}} \left(1 - \frac{\rho}{2\mu} \right)}{1 - \frac{(m-1)\rho\beta}{2m\mu}}. \end{aligned}$$

Hence, the wirelength benefit of 3D over a good 2D layout is

$$1 - \frac{L_{3D}}{L_{2D}^*} \le 1 - \frac{1 - \frac{(m-1)\rho}{a^v \times L_{2D}^*} \left(\frac{n^c a^c}{m\mu - (m-1)\rho} \right)^{\frac{3}{2}} \left(1 - \frac{\rho}{2\mu} \right)}{1 - \frac{(m-1)\rho\beta}{2m\mu}}.$$

Circuit	n_c	$a_c(\mu m^2)$	$L^*_{2D}(\mu m)$	2D die area(μm^2)
ibm01	12506	1.580	169415	28188
ibm02	19342	1.310	345036	36303
ibm03	22853	1.360	462608	44433
ibm04	27220	1.460	555368	56651
ibm05	28146	1.460	962797	58816
ibm06	32332	1.050	488335	48629
ibm07	45639	1.300	816002	84506
ibm08	51023	1.200	898645	87704
ibm09	53110	1.340	945069	102032
ibm10	68685	1.700	1768071	166678
ibm11	70152	1.310	1360500	131669
ibm12	70439	1.780	2230254	179096
ibm13	83709	1.280	1640461	152529
ibm14	147088	1.350	3183703	283506
ibm15	161187	1.210	3789764	278765
ibm16	182980	1.400	4195917	366177
ibm17	184752	1.650	5956272	436663
ibm18	210341	1.320	4114316	397448

TABLE II
CIRCUIT PARAMETERS. THE WIRELENGTHS AND DIE AREAS ARE GENERATED WITH μ SET TO 70%.

Circuit	$\frac{\text{3D die area}}{\text{2D die area}}$	# TSVs	$1 - \frac{L_{3D}}{L^*_{2D}} \leq$
ibm01	1.12	40	-2.44%
ibm02	1.12	52	-3.01%
ibm03	1.12	63	-3.00%
ibm04	1.12	81	-2.70%
ibm05	1.12	84	-3.39%
ibm06	1.12	69	-2.87%
ibm07	1.12	120	-2.28%
ibm08	1.12	125	-2.36%
ibm09	1.12	145	-1.96%
ibm10	1.12	237	-1.66%
ibm11	1.12	188	-1.91%
ibm12	1.12	255	-1.99%
ibm13	1.12	217	-1.82%
ibm14	1.12	404	-1.01%
ibm15	1.12	397	-1.64%
ibm16	1.12	521	-0.62%
ibm17	1.12	622	-0.94%
ibm18	1.12	566	-0.03%
Average:	1.12		-1.98%

TABLE III
RESULTS FOR $m = 4$, $\mu = 0.7$, $a_v = 5 \times 5$, AND $\rho = 0.1$.

III. SIMULATION RESULTS AND DISCUSSION

We used the ISPD-98 placement benchmarks [13] from IBM for our case study. The benchmarks are scaled to a 32 nm process. The standard cell height is $1.536\mu m$. A very important parameter in our study is the TSV cell dimension. [11] indicated that the TSV cell dimension is about 5 to 10 times the height of a standard cell in 32nm technology. So, we first assume the TSV cells can fit into the height of five standard cell rows (= $9.216\mu m$) which reflects the optimistic end of current TSV technologies and report the corresponding results. After that, we also report the results assuming that in the future the TSV cells can be significantly diminished such that they can fit into the height of just a single standard cell row (= $1.536\mu m$).

Table II shows the cell count, the average cell size, and the 2D wirelength L^*_{2D} at 70% area utilization for each circuit. We got the 2D wirelength L^*_{2D} using FastPlace 3.0 [15] followed by FastDP [16]. For fair comparison, we assume the area utilization of the 3D layouts is also 70% as in the 2D layouts. We assume all 3D layouts take the square shape (i.e., $W = H$) for the results reported below, but our model is very flexible and can analyze layouts with any rectangular shape. β, the lower bound of wirelength along the x-direction in an upper layer to the average lateral wirelength of all layers, is conservatively taken to be 0.8. The TSV cell size is expressed as its width times its height where both width and height are in terms of standard-cell height.

First, we consider laying out the benchmark circuits in four layers with TSV cell size equals to 5×5. The TSV count in a design depends on ρ, the proportion of die area occupied by TSV cells in the upper layers. In Table III, we report the increase in die area, total number of TSVs, and wirelength benefit upper bound for each circuit when $\rho = 10\%$ (i.e., the ratio of the TSV cell occupied area to the standard cell occupied area in the upper layers is $1 : 6$ as $\mu = 70\%$). It can be seen that all circuits yielded a negative wirelength benefit when placed in 3D. In other words, the total wirelength of 3D integration is actually worse than 2D integration. This is because the TSV cells will take up silicon real estate and increase the separation of cells on the same layer. We also note that although the ratio of the TSV cell occupied area to the standard cell occupied area is already 1 to 6, the number of TSVs used in each case is still much less than the minimum cut size[1] of a 4-way partitioning of the circuit. So, we tried setting the value of ρ for each circuit according to the 4-way partitioning cut size by hMetis [17] and report the new results in columns 3 to 5 of Table IV. It can be seen that the ratio of the TSV cell occupied area to the standard cell occupied area in the upper layers ($\rho : (\rho - \mu)$) rises to $4 : 3$ on average which represents a huge overhead. As a result, the 3D total die area is increased to 1.78 times the 2D die area on average. But the upper bound on wirelength benefit of 3D integration remains negative for most cases.

Second, we predict what would happen if the TSV cell size can be diminished to 1×1. Again we assume the value of ρ for each circuit is set according to the 4-way partitioning cut size. The results are shown in the last three columns of Table IV. The ratio of the TSV cell occupied area to the standard cell occupied area in the upper layer ($\rho : (\rho - \mu)$) is only $2 : 33$ on average. So, there is only a modest increase in total die area compared to 2D layout. The upper bound on wirelength benefit of 3D integration becomes positive for all cases. In other words, the wirelength can potentially be reduced if the TSV cell size can be successfully reduced to the extent that it is comparable to a standard cell.

Third, we check if the conclusion still holds when the number of layers of 3D integration is changed. We report the results in Figure 3 for the three largest benchmarks. For each circuit, we use its two-way and three-way partitioning cut sizes by hMetis to set the values of ρ for 2-layer and 3-layer placement. It can be seen that if the TSV cell size can be reduced to 1×1, some wirelength reduction may be obtained. However, for TSV cell size of 5×5, the potential wirelength benefit is negligible no matter 2 or 3 or 4 layers are used.

[1]The minimum cut size is a lower bound of TSV usage.

Circuit	Cut size	$a_v = 5 \times 5$			$a_v = 1 \times 1$		
		ρ	3D die area / 2D die area	$1 - \frac{L_{3D}}{L^*_{2D}} \leq$	ρ	3D die area / 2D die area	$1 - \frac{L_{3D}}{L^*_{2D}} \leq$
ibm01	344	0.35	1.61	-6.56%	0.03	1.03	11.54%
ibm02	510	0.38	1.69	-10.21%	0.03	1.04	9.15%
ibm03	1358	0.50	2.17	-10.57%	0.07	1.08	20.13%
ibm04	1311	0.46	1.98	-8.08%	0.05	1.06	18.72%
ibm05	2994	0.57	2.55	-15.02%	0.10	1.12	23.27%
ibm06	1150	0.47	2.00	-9.65%	0.05	1.06	17.08%
ibm07	1570	0.43	1.84	-5.00%	0.04	1.05	19.07%
ibm08	2132	0.47	2.02	-4.67%	0.05	1.06	23.85%
ibm09	1406	0.38	1.67	-3.63%	0.03	1.03	16.41%
ibm10	1829	0.34	1.56	-2.56%	0.02	1.03	14.71%
ibm11	1947	0.39	1.71	-3.12%	0.03	1.04	17.95%
ibm12	3585	0.44	1.89	-2.35%	0.04	1.05	23.44%
ibm13	1678	0.34	1.56	-3.36%	0.03	1.03	13.85%
ibm14	3069	0.33	1.56	0.68%	0.02	1.03	18.13%
ibm15	4435	0.40	1.75	-0.95%	0.04	1.04	21.52%
ibm16	3707	0.32	1.53	2.22%	0.02	1.03	19.00%
ibm17	4562	0.33	1.54	0.87%	0.02	1.03	17.90%
ibm18	3106	0.28	1.42	3.12%	0.02	1.02	17.04%
Average:		0.40	1.78	-4.38%	0.04	1.04	17.93%

TABLE IV
RESULTS WHEN #TSVS (I.E., ρ) ARE SET BASED ON 4-WAY PARTITIONING CUT SIZE, $m = 4$, $\mu = 0.7$, $a_v = 5 \times 5$ OR 1×1.

Finally, another parameter we can vary is the placement area utilization (μ) and we found that it does affect our conclusion.

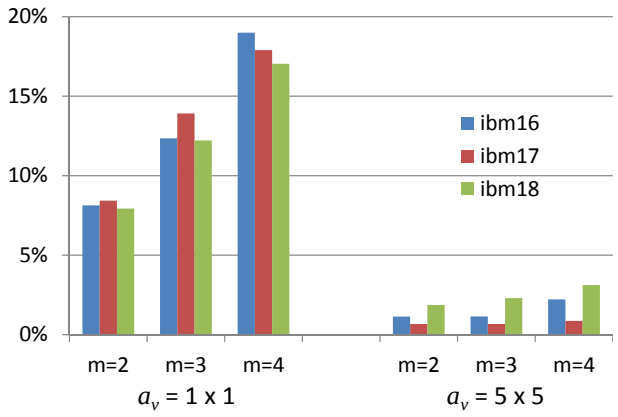

Fig. 3. Upper bound on wirelength benefit for ibm 16-18 with $m = 2, 3, 4$, $\mu = 0.7$, $a_v = 1 \times 1$ and 5×5.

We emphasize that the potential wirelength benefit values reported in this section are all upper bound values. In other words, the real wirelength benefit should be smaller. For example, we simply assumed the wirelength in the z-direction is zero when deriving the analytical expression for the upper bound. In addition, a practical 3D IC requires power/ground TSVs and clock network TSVs for distributing the power/ground signals and clock signals to all layers. It is not difficult to see that the values of the 3D wirelength benefit in the analysis above will get smaller after inserting power/ground TSVs and clock network TSVs since their inclusion will increase the die size and the separation between cells on the same layer. Hence, we can safely conclude that 3D integration is not expected to help reduce the total wirelength for the 32nm process. On the other hand, it is not to say that 3D integration will never help in reducing the wirelength. We have shown that 3D placement can potentially reduce the total wirelength if TSV cell size can be successfully diminished and made comparable with that of a standard cell, though the reduction will be less than what many people expected in the past. Our work only focuses on the total wirelength of 3D integration, but the delay benefit of 3D integration needs further investigation. We note that the delay benefit will depend on the interconnect length distribution and the TSV's resistance and capacitance.

REFERENCES

[1] J. W. Joyner, R. Venkatesan, P. Zarkesh-Ha, J. A. Davis, and J. D. Meindl, "Impact of three-dimensional architectures on interconnects in gigascale integration," *IEEE Trans. on VLSI Systems*, vol. 9, no. 6, pp. 922–928, Dec. 2001.

[2] A. Rahman and R. Reif, "System-level performance evaluation of three-dimensional integrated circuits," *IEEE Trans. on VLSI Systems*, vol. 8, no. 6, pp. 671–678, Dec. 2000.

[3] R. Zhang, K. Roy, C.-K. Koh, and D. B. Janes, "Stochastic wire-length and delay distributions of 3-dimensional circuits," in *Proc. of IEEE/ACM ICCAD*, 2000, pp. 208–213.

[4] J. Cong, G. Luo, J. Wei, and Y. Zhang, "Thermal-aware 3D IC placement via transformation," in *Proc. of ACM/IEEE ASPDAC*, 2007, pp. 780–785.

[5] J. Cong and G. Luo, "A multilevel analytical placement for 3D ICs," in *Proc. of ACM/IEEE ASPDAC*, 2009, pp. 361–366.

[6] B. Goplen and S. Spatnekar, "Placement of 3D ICs with thermal and interlayer via considerations," in *Proc. of IEEE/ACM DAC*, 2007, pp. 626–631.

[7] G. V. der Plas et al, "Design issues and considerations for low-cost 3-D TSV IC technology," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 1, pp. 293–307, Jan. 2011.

[8] D. Lammers, "Preparing for 3D IC stacking," System-Level Design Newsletter, Jul. 2010. [Online]. Available: http://chipdesignmag.com/sld

[9] A.-M. Corley, "Design challenges loom for 3-D chips," IEEE Spectrum, Feb. 2010. [Online]. Available: http://spectrum.ieee.org

[10] A. Karmarkar, "Performanace and reliability analysis of 3D-integration structures employing through silicon via (TSV)," in *Proc. of IEEE International Reliability Physics Symposium*, 2009, pp. 682–687.

[11] D. Noice and V. Gerousis, "Physical design implementation for 3D IC – methodology and tools," invited talk at Intl. Symposium on Physical Design, 2010. [Online]. Available: http://www.ispd.cc/slides/slides10/4_02.pdf

[12] D. H. Kim, S. Mukhopadhyay, and S. K. Lim, "TSV-aware interconnect length and power prediction for 3D stacked ICs," in *Proc. of IEEE Intl. Interconnect Technology Conference*, 2009, pp. 26–28.

[13] C. J. Alpert, "The ISPD98 Circuit Benchmark Suite," in *Proc. of ACM ISPD*, 1998, pp. 80–85.

[14] J. Jensen, "Sur les fonctions convexes et les inégalités entre les valeurs moyennes," *Acta Mathematica*, vol. 30, pp. 175–193, 1906.
[15] N. Viswanathan, M. Pan, and C. Chu, "FastPlace: An efficient multilevel force-directed placement algorithm," in *Modern Circuit Placement – Best Practices and Results*, G.-J. Nam and J. Cong, Eds. Springer, 2007, pp. 193–228.
[16] M. Pan, N. Viswanathan, and C. Chu, "An efficient and effective detailed placement algorithm," in *Proc. of IEEE/ACM ICCAD*, 2005, pp. 48–55.
[17] G. Karypis, R. Aggarwal, V. Kumar, and S. Shekhar, "Multilevel hypergraph partitioning: applications in VLSI domain," *IEEE Trans. on VLSI Systems*, vol. 7, no. 1, pp. 69–79, Mar. 1999.