Throughput Optimization for SADP and E-beam based Manufacturing of 1D Layout

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ABSTRACT

Due to the resolution limitations of optical lithography equipment, 1D gridded layout design is gaining steam. Self-aligned double patterning (SADP) is a mature technology for printing 1D layouts. However, for 20nm and beyond, SADP using a single trim mask becomes insufficient for printing all 1D layouts. A viable solution is to complement SADP with e-beam lithography. In this paper, in order to increase the throughput of printing a 1D layout, we consider the problem of e-beam shot count minimization subject to bounded line end extension constraints. Two different approaches of utilizing the trim mask and e-beam to print a layout are considered. The first approach is under the assumption that the trim mask and e-beam are used for end cutting. The second is under the assumption that the trim mask and e-beam are used to rid of all unnecessary portions. We propose elegant ILP formulations for both approaches. Experimental results show that both ILP formulations can be solved efficiently. The pros and cons of the two approaches for manufacturing 1D layout are discussed.

Keywords

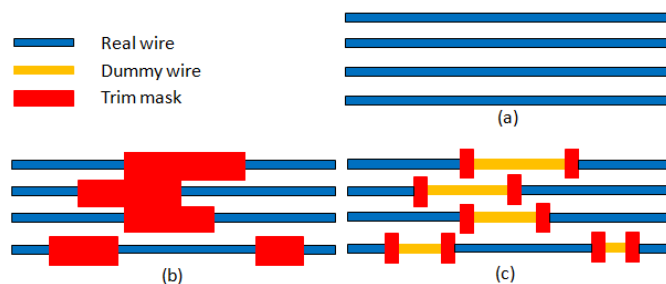SADP, gap removal, end cutting, e-beam

1. INTRODUCTION

The IC industry has been moving towards highly regular 1D gridded designs for advanced nodes[1, 2, 3, 4]. The use of 1D patterns and a simplified set of gridded design rules simplify both design and fabrication compared to conventional 2D layout style. It has been shown to result in better yield, smaller area, and better uniformity [3].

Self-aligned double patterning (SADP) is an excellent option for 1D gridded design manufacturing [5]. While litho-etch-litho-etch type double patterning requires high overlay accuracy in the exposure equipment, SADP can fabricate fine unidirectional line patterns without any overlay error easily. In the first step of SADP, uniform dense lines of the intended

Figure 1: The SADP process has two steps: dense line generation and trim mask design. (a)Dense line generation. (b)Trimming by gap removal. (c)Trimming by end cutting.

pitch are formed as illustrated in Fig. 1(a). Then, the portions not on the design can be removed by a trim mask in the second step as shown in Fig. 1(b). We will refer to this approach as *trimming by gap removal*.

On the other hand, Du et al. [6] proposed another possibility of trimming the layout for 1D gridded design at sub-20nm process node. Instead of totally removing the unwanted portions after fabricating the unidirectional line patterns, one may use small fixed size rectangular cuts (48nm by 32nm for 16nm process node) to chop up the parallel tracks into real and dummy wires as shown in Fig 1(c). We will refer to this approach as *trimming by end cutting*.

However, at sub-20nm process node, the trim mask may not be printable using 193nm immersion (193i) lithography alone. For the gap removal approach, some unwanted portions may become too small or too close to each other and violate the design rules of the trim mask. For the end cutting approach, the cuts may be too close to each other that forbidden patterns may be formed and cannot be printed by 193i.

As a solution, it is possible to apply the trim mask to rid of most of the unwanted portions / print most of the cuts and then apply e-beam lithography to remove the remaining unwanted portions / print the remaining cuts. This is an example of complementary or hybrid lithography [7, 8, 9]. In this paper, we assume variable-shaped beam (VSB) method [10] is used in e-beam lithography.

Du et al. [6] considered the end cutting approach for trimming and formulated a cut redistribution problem to maximize the number of cuts printed by 193i lithography while not violating any rule of forbidden patterns. Hence, the number of e-beam cuts can be minimized and the manufacturing

throughput will be increased. However, there are two short-comings in their work. First, their problem formulation assumes that line end extension is allowed as long as the logic connections are not changed when performing cut redistribution. Thus, the length of the wire segments may be greatly increased. This is not desirable in practice since significant line end extension will affect the circuit performance. Second, the proposed ILP-based cut redistribution algorithm in [6] was very time consuming. The CPU time of their optimal ILP for small layouts was up to 9 hours. For larger layouts, they proposed a faster iterative non-optimal version but still required hours of CPU time.

In this work, we investigate the printing of 1D layout with complementary SADP / e-beam lithography. We solve two problems of e-beam shot minimization, one for trimming by end cutting and another for trimming by gap removal, under line end extension constraint on individual wires to limit performance impact. For trimming by end cutting, we propose a fast optimal ILP based solution which is on average more than 1000 times faster than that in [6]. For trimming by gap removal, we give an optimal ILP based solution which is also very efficient in practice and can reduce the e-beam shot count by about 41.38% on average compared to trimming by end cutting based on layout benchmarks for M1 layer.

The rest of the paper is organized as follows. Section 2 firstly provides an overview of SADP and e-beam process. Then, it gives formal problem definitions for both trimming by end cutting and trimming by gap removal. In Section 3, we give elegant ILP formulations for both of the problems. Section 4 presents our experimental results. Finally, Section 5 concludes this paper.

2. PROBLEM DESCRIPTION

2.1 Overview of SADP and E-beam process

The traditional SADP has two major steps. The first step is dense line generation. Suppose the intended 1D layout pitch is p. 1D tracks with pitch $2p$ will firstly be fabricated. Printing at two times of the intended pitch is relatively easy to handle with 193i technology. By etching all the film material on the horizontal surface of 1D tracks and the original 1D tracks, a spacer which is a film layer deposited on the sidewall of 1D tracks is formed. Since there are two spacers for each track, the line density is doubled and pitch is halved.

The second step is trim mask application. In order to achieve the intended circuit pattern and functionality, some portions of the metal lines need to be trimmed away with the help of a trim mask. In practice, the trim mask can be designed by two different approaches. One is to use fixed size rectangular cuts to chop up the parallel lines at required positions such that the unwanted portions are separated from real wires. As a result, the trim mask contains those small rectangular cuts. We call this approach *trimming by end cutting*. The other one is to directly remove unwanted portions of wires. As a result, the trim mask contains patterns covering those unwanted portions. We refer to those unwanted portions as gaps and call this approach *trimming by gap removal*.

In SADP, the trim mask is printed by 193i lithography. The patterns on the trim mask must satisfy minimum spacing and minimum width constraints. However at sub-20nm process node, for both trimming approaches, it is very likely that some trimming patterns would violate the trim mask

constraints. In that case, the violations must be eliminated by some combinations of line end extension and e-beam lithography.

For both trimming approaches, three options to eliminate the violations are illustrated by the printing of the simple 1D layout in Fig. 2(a). For trimming by end cutting, let's focus on cuts 1 and 2 in Fig. 2(b). Suppose they are too close to each other such that the minimum spacing constraint is violated. To resolve the violation, one option is to merge the two cuts into a single one as shown in Fig. 2(c). Note that the line ends need to be extended to align the cuts vertically. Another option, as shown in Fig. 2(d), is to separate the two cuts from each other by extending the line ends. The third option is to use 193i to print cut 1 and e-beam to print cut 2 as shown in Fig. 2(e). Now consider trimming by gap removal. As shown in Fig. 2(f), the two patterns covering the gaps are too close to each other. Similar to above, we have three options to resolve it. The first option is to merge the two patterns as in Fig. 2(g), as long as the abutting part satisfies the minimum width constraint. The second option, as shown in Fig. 2(h), is to separate the two patterns from each other by extending the line ends. The third option is to print one of the patterns by e-beam as shown in Fig. 2(i).
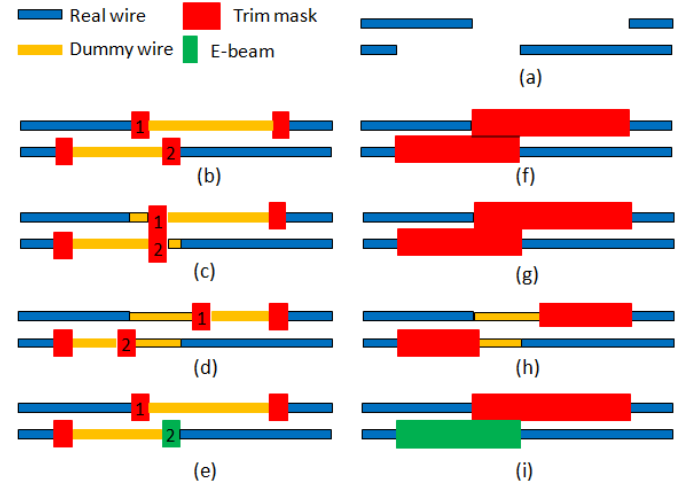
Figure 2: Three options to eliminate the violations of trim mask constraints. (a)A simple 1D layout. (b)Trimming by end cutting approach. (c)Merging two cuts. (d)Separating two cuts by line end extension. (e)Printing one cut by e-beam. (f)Trimming by gap removal approach. (g)Merging two patterns. (h)Separating two patterns by line end extension. (i)Printing one pattern by e-beam.

However, due to the throughput impact of e-beam shot count, we want to minimize the number of e-beam shots used. Meanwhile, significant amount of wire extension may affect circuit timing. In particular, some wires may be on the critical paths of the design for which wire extension is not even allowed. Consequently, we introduce a line end extension constraint for each wire which limits the allowed length of wire extension. We also want to minimize the total length of wire extension while satisfying line end constraints of all the wires.

2.2 Problem formulation

Given a 1D layout, we would like to use complementary lithography with SADP and e-beam to print it. For each wire,

a maximum allowed extension length is given. The problem is to minimize a weighted sum of the number of e-beam shots and the total line end extension length subject to layout constraints on trim mask and line end extension constraints on individual wires. Based on the two different approaches of trim mask design, we can formulate two different problems for complementary SADP / e-beam lithography of 1D layout.

2.2.1 Trimming by end cutting

To trim a 1D layout by end cutting, each wire is delineated by two small rectangular cuts on its two ends. The problem is basically to redistribute the cuts in order to eliminate all forbidden patterns while minimizing the required number of e-beam shots and total line end extension length. Du et al. [6] has considered a similar problem. Different from their work, we are adding line end extension constraints to the problem as a way to control the impact on performance.

2.2.2 Trimming by gap removal

Given a 1D layout, a gap is defined by the ends of the two wires on its left and right sides. For gap removal trimming approach, the problem is to determine the cut required for each gap to remove all or part of it so that the cut patterns are printable while the required number of e-beam shots and total line end extension length are minimized.

Compared with trimming by end cutting, trimming by gap removal intuitively has its advantages. In order to get rid of an unwanted portion, end cutting uses two small cuts to separate it from real wires. However, gap removal directly removes the unwanted portions with one cut. The number of cuts required to define the wires is relatively smaller. Thus the number of e-beam shots required is potentially smaller. We confirm this intuition in the experimental results section.

3. PROPOSED SOLUTIONS

We propose an elegant ILP formulation for each of the problems. Experimental results demonstrate that ILP solver can solve the ILPs in a very efficient manner.

3.1 ILP formulation for trimming by end cutting approach

[6] performed lithography simulation on rectangular cuts for 16nm 1D layout design. Based on the simulation results, they obtained the horizontal safe distance for two rectangular cuts in the same track or nearby tracks. We adopt this criterion and use it as the minimum spacing constraint in our ILP formulation. Meanwhile, we set the minimum width as the width of a rectangular cut. [6] proposed an ILP formulation for trimming by end cutting approach. However, our ILP formulation has three major advantages. Firstly, we can handle line end extension constraint for each wire. Secondly, fewer binary variables are introduced. Finally, instead of representing the x-coordinates of line ends as integer variables, we treat them as continuous variables. We show later in this section that integral optimal solutions will still be found. This modification helps speed up the ILP solution process dramatically.

Given a 1D layout with n wires, we number all the wires from 1 to n row by row from left to right. x_{2i-1} and x_{2i} are two continuous variables representing the x-coordinates of the left and right ends of $wire_i$. By definition, two small rectangular cuts c_{2i-1} and c_{2i} are located on the left and right ends

of each wire. e_{2i-1} and e_{2i} are two binary variables indicating whether c_{2i-1} and c_{2i} are printed by e-beam lithography. $e_{2i-1} = 1$ if c_{2i-1} is printed by e-beam lithography; $e_{2i-1} = 0$ if c_{2i-1} is printed by optical lithography(193i).

Objective:
Minimize $\sum_{i=1}^{2n} e_i + \alpha(\sum_{i=1}^{n}(x_{2i} - x_{2i-1}) - \sum_{i=1}^{n}(r_i - l_i))$ where α is a parameter that indicates the relative cost of e-beam shot to wire extension, l_i and r_i are the x-coordinates of the left and right ends of $wire_i$ in the given layout.

Constraints:
C1. Constraints for line end extension

$$\begin{cases} x_{2i} \geq r_i & 1 \leq i \leq n \\ x_{2i} - x_{2i-1} \leq r_i - l_i + \delta_i & 1 \leq i \leq n \\ x_{2i-1} \leq l_i & 1 \leq i \leq n \\ x_{2i-1} \geq LL & 1 \leq i \leq n \\ x_{2i} \leq RR & 1 \leq i \leq n \end{cases}$$

where δ_i is the allowed wire extension for each $wire_i$, LL and RR are the x-coordinates of the left and right boundaries in the given layout.

C2. Constraints for gap between wires
For any gap_k between $wire_i$ and $wire_{i+1}$ in the given layout, r_i and l_{i+1} are the x-coordinates of its left and right ends. We denote it as $gap_k[r_i, l_{i+1}]$. Two small rectangular cuts c_{2i} and c_{2i+1} locate on the left and right ends of gap_k, respectively. m_{2i}^{2i+1} is a binary variable indicating whether c_{2i} and c_{2i+1} overlap or abut. $m_{2i}^{2i+1} = 0$ if c_{2i} and c_{2i+1} do not overlap or abut. In this case, c_{2i} and c_{2i+1} should be separated horizontally by at least the minimum spacing. Otherwise, one of two cuts should be printed by e-beam. $m_{2i}^{2i+1} = 1$ if c_{2i} and c_{2i+1} overlap or abut, which means the two cuts merge into a single cut. Hence, we have the following constraints.

$$\begin{cases} x_{2i+1} - x_{2i} + B \times e_{2i+1} + B \times e_{2i} + B \times m_{2i}^{2i+1} \geq min_s \\ x_{2i+1} - x_{2i} - B \times (1 - m_{2i}^{2i+1}) \leq 2 \times min_w \\ x_{2i+1} - x_{2i} \geq min_w \end{cases}$$

where B is a very big constant, min_s is the minimum cut spacing, and min_w is the minimum cut width.

C3. Constraint for non-overlapping gaps
Given $gap_p[r_i, l_{i+1}]$ and $gap_q[r_j, l_{j+1}]$, $dist_{pq} = max(r_i, r_j) - min(l_{i+1}, l_{j+1})$ is defined as the horizontal distance for them. We say $gap_p[r_i, l_{i+1}]$ and $gap_q[r_j, l_{j+1}]$ are non-overlapping in the horizontal direction if $dist_{pq} \geq 0$. If $0 \leq dist_{pq} < min_s$, a forbidden pattern occurs. There are three available options to resolve a forbidden pattern: (1) merging a pair of rectangular cuts by aligning them vertically; (2) separating a pair of two rectangular cuts with at least the minimum spacing min_s by line end extension if necessary; (3) printing one of the rectangular cuts in a pair by e-beam. In this case, option (1) is not possible since two gaps are non-overlapping. However, the other two options are available. Without loss of generality, we assume $l_{j+1} \leq r_i$. We have

$$x_{2i} - x_{2j+1} + B \times e_{2i} + B \times e_{2j+1} \geq min_s$$

C4. Constraints for overlapping gaps
We say $gap_p[r_i, l_{i+1}]$ and $gap_q[r_j, l_{j+1}]$ are overlapping in the horizontal direction if $dist_{pq} < 0$. There are three cases when considering two overlapping gaps. For each case, the available options to resolve the forbidden pattern are different. As a result, the constraints in our ILP formulation are different. We discuss each case below. Note that we need to avoid forming a forbidden pattern between a cut at either end of gap_p and a cut at either end of gap_q. So, we need to impose a few constraints between a cut at either end of gap_p

and a cut at either end of gap_q. We only show the constraints between x_{2i+1} and x_{2j} below. The constraints for the other three pairs of end points are similar.

C4.1 Suppose $gap_p[r_i, l_{i+1}]$ and $gap_q[r_j, l_{j+1}]$ are on adjacent tracks. All three options to resolve a forbidden pattern are available.

$$\begin{cases} x_{2i+1} - x_{2j} + B \times (e_{2i+1} + e_{2j} + d_{2j}^{2i+1} + m_{2j}^{2i+1}) \geq min_s \\ x_{2i+1} - x_{2j} + B \times (1 - m_{2j}^{2i+1}) \geq min_w \\ x_{2i+1} - x_{2j} - B \times (1 - m_{2j}^{2i+1}) \leq min_w \\ x_{2j} - x_{2i+1} + B \times (e_{2i+1} + e_{2j} + 1 - d_{2j}^{2i+1} + m_{2j}^{2i+1}) \geq min_s \end{cases}$$

where m_{2j}^{2i+1} is a binary variable indicating whether c_{2j} and c_{2i+1} are aligned vertically. $m_{2j}^{2i+1} = 0$ if c_{2i} and c_{2i+1} are not aligned vertically, which means only options (2) and (3) are available to resolve the forbidden pattern. $m_{2j}^{2i+1} = 1$ if c_{2i} and c_{2i+1} are aligned vertically, so the two cuts merge into one bigger cut. Meanwhile, d_{2j}^{2i+1} is a binary variable corresponding to two location possibilities of c_{2j} and c_{2i+1} if option(2) is applied. $d_{2j}^{2i+1} = 1$ if finally c_{2i+1} is on the left side of c_{2j} in horizontal direction. $d_{2j}^{2i+1} = 0$ if finally c_{2i+1} is on the right side of c_{2j} in horizontal direction.

C4.2 Suppose $gap_p[r_i, l_{i+1}]$ and $gap_q[r_j, l_{j+1}]$ are on non-adjacent tracks and for each track in between there does not always exist a gap such that all these gaps together with gap_p and gap_q are mutually overlapped. In this case, the option (1) is not possible. This is because the merging of two rectangular cuts will intersect with wire segment on some track in between.

$$\begin{cases} x_{2i+1} - x_{2j} + B \times (e_{2i+1} + e_{2j}) + B \times d_{2j}^{2i+1} \geq min_s \\ x_{2j} - x_{2i+1} + B \times (e_{2i+1} + e_{2j}) + B \times (1 - d_{2j}^{2i+1}) \geq min_s \end{cases}$$

C4.3 Suppose $gap_p[r_i, l_{i+1}]$ and $gap_q[r_j, l_{j+1}]$ are on non-adjacent tracks and for each track in between there always exists a gap such that all these gaps together with gap_p and gap_q are mutually overlapped. In this case, the option (1) is possible only when there is a rectangular cut from each track in between also aligns with them vertically. Without loss of generality, we assume gap_p and gap_q are on non-adjacent tracks with only one track in between and there exists $gap_s[r_k, l_{k+1}]$ from this track such that gap_p, gap_q and gap_s are mutually overlapped.

$$\begin{cases} x_{2i+1} - x_{2j} + B \times (e_{2i+1} + e_{2j} + d_{2j}^{2i+1} + m_{2j}^{2i+1}) \geq min_s \\ x_{2i+1} - x_{2j} + B \times (1 - m_{2j}^{2i+1}) \geq min_w \\ x_{2i+1} - x_{2j} - B \times (1 - m_{2j}^{2i+1}) \leq min_w \\ x_{2k+1} - x_{2j} + B \times (1 - m_{2j}^{2i+1}) \geq min_w \\ x_{2k+1} - x_{2j} - B \times (1 - m_{2j}^{2i+1}) \leq min_w \\ x_{2j} - x_{2i+1} + B \times (e_{2i+1} + e_{2j} + 1 - d_{2j}^{2i+1} + m_{2j}^{2i+1}) \geq min_s \end{cases}$$

3.2 ILP formulation for trimming by gap removal approach

Objective:

Minimize $\sum_{i=1}^{m} e_i + \alpha(\sum_{i=1}^{m}(x_{2i-1} - x_{2i}) - \sum_{k=1}^{n}(r_k - l_k))$ where m and n are the total number of gaps and wires in the given layout respectively, e_i is a binary variable indicates whether the gap_i is printed by e-beam lithography, α is a parameter indicates relative cost of e-beam shot to wire extension, x_{2i-1} and x_{2i} are x-coordinates for left and right ends of gap_i, l_k and r_k are x-coordinates of left and right ends of $wire_k$ in the given layout.

Constraints:

C1. Constraints for line end extension

Based on the x-coordinates of all the gaps, we can find x-coordinates of left and right ends of each wire. Then line end

extension constraint is exactly same with C1 in Section 3.1. Due to the page limit, we are not repeating it here.

C2. Constraint for gap ends

Given a gap_i, we have

$$x_{2i} - x_{2i-1} + B \times e_i \geq min_w$$

where min_w is minimum width.

C3. Constraint for non-overlapping gaps or overlapping gaps with overlapping length less than minimum width

Given two gaps, suppose gap_i is between $wire_p$ and $wire_{p+1}$, gap_j is between $wire_q$ and $wire_{q+1}$. Then we have a similar definition of $dist_{ij}$ for $gap_i[r_p, l_{p+1}]$ and $gap_j[r_q, l_{q+1}]$ as in 3.1.C3. If $0 < dist_{ij} < min_s$ or $-min_w < dist_{ij} \leq 0$, $gap_i[r_p, l_{p+1}]$ and $gap_j[r_q, l_{q+1}]$ form a forbidden pattern. There are three available options to resolve a forbidden pattern: (1) merging two patterns with at least minimum width of abutting part; (2) separating two patterns with at least minimum spacing by line end extension if necessary; (3) printing one of two patterns by e-beam. In this case, the option (1) is not possible since either two gaps are non-overlapping or merging two gaps violates minimum width constraint. However, the other two options are available. Without loss of generality, we assume $l_{q+1} < r_p$. We have

$$x_{2i-1} - x_{2j} + B \times e_i + B \times e_j \geq min_s$$

where min_s is minimum spacing.

C4. Constraints for overlapping gaps with overlapping length equal or larger than minimum width

Given $gap_i[r_p, l_{p+1}]$ and $gap_j[r_q, l_{q+1}]$, two different cases should be considered if $min_w \leq \Theta_{ij}$.

C4.1 Suppose $gap_i[r_p, l_{p+1}]$ and $gap_j[r_q, l_{q+1}]$ are on adjacent tracks. In this case, all three options are available to resolve a forbidden pattern. Hence, we have following constraints.

$$\begin{cases} x_{2j} - x_{2i-1} + B \times e_i + B \times e_j + B \times (1 - m_i^j) \geq min_w \\ x_{2i-1} - x_{2j} + B \times (e_i + e_j + m_i^j) + B \times d_i^j \geq min_s \end{cases}$$

$$\begin{cases} x_{2i} - x_{2j-1} + B \times e_i + B \times e_j + B \times (1 - m_i^j) \geq min_w \\ x_{2j-1} - x_{2i} + B \times (e_i + e_j + m_i^j) + B \times (1 - d_i^j) \geq min_s \end{cases}$$

where m_i^j is a binary variable indicating whether gap_i and gap_j merge into one pattern. $m_i^j = 0$ if gap_i and gap_j do not merge, which means only options (2) and (3) are available to resolve the forbidden pattern. $m_i^j = 1$ if gap_i and gap_j merge into one pattern and the abutting part should satisfy minimum width constraint. Meanwhile, d_i^j is a binary variable corresponding to two location possibilities of gap_i and gap_j if option (2) is applied. $d_i^j = 0$ if finally gap_i is on the right side of gap_j in the horizontal direction. $d_i^j = 1$ if finally gap_i is on the left side of gap_j in horizontal direction.

C4.2 Suppose $gap_i[r_p, l_{p+1}]$ and $gap_j[r_q, l_{q+1}]$ are on non-adjacent tracks and for each track in between there always exist a gap such that all these gaps together with gap_i and gap_j are mutually overlapped. In this case, option (1) is not possible. This is because there is a wire segment on some track in between which separates $gap_i[r_p, l_{p+1}]$ and $gap_j[r_q, l_{q+1}]$ apart. Hence, we have following constraints.

$$\begin{cases} x_{2i-1} - x_{2j} + B \times e_i + B \times e_j + B \times d_i^j \geq min_s \\ x_{2j-1} - x_{2i} + B \times e_i + B \times e_j + B \times (1 - d_i^j) \geq min_s \end{cases}$$

Note that the wires of a 1D gridded design are supposed to end at discrete locations. Although we are using continuous variables to represent the x-coordinates of the line ends, both of our ILP formulations are optimal. We will prove it below.

LEMMA 3.1. *There always exists integral optimal solutions for our ILP formulations.*

PROOF. For our ILP formulations, all the parameters in the constraints are integers. If we fix the binary variables in our ILPs, all the constraints are of the form:

$$\begin{cases} A \leq x \leq B \\ C \leq x - x' \leq D \end{cases}$$

where A, B, C, and D are some integer constants. So the vertices of the polytopes formed by these constraints must be integral. This implies that there exist integral optimal solutions for our ILP formulations. □

A Simplex method based solver will always return the integral optimal solution as Simplex method moves from one vertex of the feasible set to an adjacent vertex during the search for the optimal solution. If some other methods are used to solve the ILPs, the optimal solution returned may not be integral. In that case, the optimal integral solution can be found by running one step of Simplex method to move to a vertex.

4. EXPERIMENTAL RESULTS

We run all experiments on a machine with an Intel Core i5 2.66GHz CPU (which has two cores) and 4GB of memory. We use Gurobi 5.6.0 linux64 to solve our ILP formulations. Note that Gurobi uses primal and dual simplex algorithms to solve LPs. It always returns integral solutions for all benchmarks.

We generated a set of benchmarks based on the benchmarks provided by [6]. As we consider line end extension constraints in our problem formuations, we randomly generate allowed wire extension value for each wire in the benchmarks. The benchmarks are based on 16 nm 1D standard cell design. In 1D standard cell design, standard cells of the same height are placed along the cell tracks in the layout. The cell tracks are isolated from one another by the power/ground rails. As a result, each benchmark corresponds to one cell track. In the 1D cell library used, wire tracks on Poly and Metal 1 are perpendicular to the cell tracks. The height of each standard cell is 14 grids, which means there are 14 locations along the Poly / Metal 1 wire direction to place the cuts. The wire tracks on Metal 2 are parallel to the cell tracks.

In Section 4.1, we first use 6 small benchmarks for Metal 1 (with 50 to 300 wire tracks) to compare the ILP formulation of [6] with ours. In Section 4.2, our ILP formulations for the two trimming approaches are compared. In addition to the small benchmarks, 8 larger benchmarks (4 for Metal 1 with 1000 to 8000 wire tracks and 4 for Metal 2 with width of 1000 to 8000 tracks) are used. Section 4.3 discusses the pros and cons of the two trimming approaches for manufacturing of 1D layout.

4.1 Comparison with [6]'s ILP formulation

In this subsection, we try to compare the performance of [6]'s ILP formulation with our ILP formulation for end cutting trimming approach. Because the ILP formulation in [6] does not consider line end extension constraints, we modify their ILP formulation and add line end extension constraints to it. Moreover, the ILP formulation in [6] does not consider the overlapping of e-beam shots. If two e-beam shots completely overlap, their ILP will still count them as two shots even though a single shot is enough to print them. In other words, their ILP may overestimate the required shot count. For the sake of comparison, we disable the consideration of

overlapping e-beam shots in our ILP formulation here. (We enable this feature of our ILP in all other experiments.) In Table 1, we can see that our ILP formulation dramatically reduces the runtime by more than 1000× while obtaining optimal solutions. We believe using continuous instead of discrete variables for the line end coordinates is one of the major reasons that our ILP is much faster than [6]'s. We cannot report the comparison based on bigger benchmarks here as the ILP in [6] is too slow to handle them.

Table 1: Comparison with [6]'s ILP formulation

M1 layer	[6]'s ILP		Our ILP (End cutting)	
#track	#e-beam	Runtime(s)	#e-beam	Runtime(s)
50	14	64.76	14	0.53
100	24	185.34	24	2.18
150	36	301.29	36	4.00
200	48	589.13	48	4.47
250	59	20141.16	59	4.03
300	69	22097.32	69	17.41
Normalized	1.00	1113.56	1.00	1.00

4.2 Comparison of ILPs for two trimming approaches

In this subsection, we compare the ILP formulations for the two trimming approaches of manufacturing 1D layout. We first test them on the same small benchmarks used in Section 4.1. From Table 2, we can see that the ILPs for both approaches can be solved efficiently. The gap removal approach is even faster[1]. In addition, the required number of e-beam shots and total length of wire extension are both less for gap removal approach.

Then we test the two ILPs on the larger benchmarks for both M1 and M2 layers. The results are reported in Table 3. For M1 layer, the gap removal approach still get a much faster runtime, fewer e-beam shots and less wire extension compared with end cutting approach. For the benchmarks for M2 layer, it is very interesting to see that end cutting approach generates much better solution than gap removal approach. It can print the M2 layouts without using any e-beam shot and the wire extension is also less than that of gap removal approach.

Table 2: Comparison for two trimming approaches on small benchmarks

M1 layer	End cutting approach			Gap removal approach		
#track	#e-beam	Wire ext.	Runtime(s)	#e-beam	Wire ext.	Runtime(s)
50	14	53	0.09	8	40	0.02
100	24	106	2.37	14	64	0.04
150	36	236	4.08	22	91	0.06
200	48	244	0.04	30	133	0.34
250	59	324	4.02	38	166	0.22
300	69	403	4.88	46	211	0.93
Normalized	1.63	1.88	26.34	1.00	1.00	1.00

4.3 Discussion of two trimming approaches

As pointed out by [6], wires on the M2 layer are used to connect different standard cells. Thus both wires and gaps in M2 layer are much longer than those in M1 layer. So when the end cutting approach is applied to M2 layer, the rectangular cuts are relatively few and are sparsely distributed. In other

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[1]Comparing with Table I, we notice that our ILP is even faster while getting the same e-beam counts when the overlapping of e-beam shots is not ignored.

Table 3: Comparison for two trimming approaches on large benchmarks

M1 layer	End cutting approach			Gap removal approach		
#track	#e-beam	Wire ext.	Runtime(s)	#e-beam	Wire ext.	Runtime(s)
1000	266	1560	1144.65	148	624	1.35
2000	515	3123	623.99	286	1248	5.09
4000	1026	6447	1866.07	564	2701	16.73
8000	2157	12924	12975.00	1166	5373	90.65
Normalized	1.82	2.45	306.29	1.00	1.00	1.00
M2 layer	End cutting approach			Gap removal approach		
Width	#e-beam	Wire ext.	Runtime(s)	#e-beam	Wire ext.	Runtime(s)
1000	0	63	0.33	8	172	0.30
2000	0	115	0.62	12	216	0.06
4000	0	218	1.19	564	426	0.10
8000	0	473	4.18	56	918	0.56
Normalized	0.00	0.49	7.70	1.00	1.00	1.00

words, forbidden patterns in a given layout may be few and can usually be resolved easily by line end extension as shown in Fig. 3(a).

However, for gap removal approach, longer gaps mean longer trim patterns. It is much easier for forbidden patterns to occur and it may take excessive line end extension to separate the conflicting patterns as shown in Fig. 3(b). If the wire extension required is beyond the allowed value, one e-beam shots is needed to resolve the forbidden patterns as shown in Fig. 3(c).
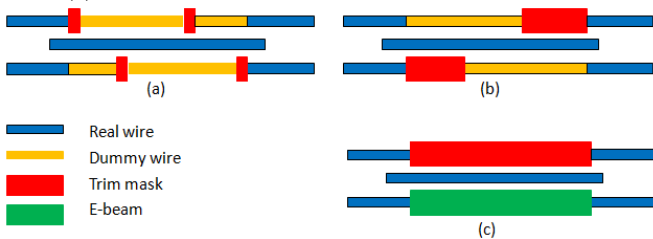
Figure 3: Explanation on why end cutting approach performs better than gap removal approach for Metal 2. (a)End cutting requires less wire extension to separate conflicting patterns. (b)Gap removal requires more wire extension to separate conflicting patterns. (c)If wire extension exceeds the limit, one more e-beam shot is required.

Based on the characteristics of M1 and M2 layer, the two approaches shows their pros and cons for manufacturing of 1D layout. For M1 layer, the line end distribution is dense and gap range is small compared with M2 layer, gap removal approach potentially can fabricate the layout with fewer e-beam shots and less wire extension. The ILP for gap removal approach can also be solved very efficiently. However, because the trim mask of gap removal approach is general shape instead of small fixed rectangles for end cutting approach, the cost of making the trim mask is probably higher [5]. Overall, the gap removal should still be the better approach for M1 layer. For M2 layer, the line end distribution is sparse and gap range is big, end cutting approach potentially can fabricate the layout with zero e-beam shot. Thus, the e-beam lithography process is totally eliminated for M2 fabrication, which tremendously saves the fabrication cost. The ILP for end cutting approach can also be solved very efficiently. Hence end cutting is the better approach for M2 layer.

5. CONCLUSION

In this paper, in order to increase the throughput of printing a 1D layout, we consider the problem of e-beam shot count and line end extension minimization subject to bounded line end extension constraints. Two different approaches of utilizing the trim mask and e-beam to print a layout are considered. The first approach which is called trimming by end cutting is under the assumption that the trim mask and e-beam are used to cut unnecessary portions from real wires. The second approach which trimming by gap removal is under the assumption that the trim mask and e-beam are used to rid of all unnecessary portions. We proposed elegant ILP formulations for both approaches. Experimental results show that both ILP formulations can be solved very efficiently. Meanwhile, the optimal solutions obtained by our ILP formulations demonstrate that gap removal approach is suitable for manufacturing of M1 layer and end cutting approach is suitable for manufacturing of M2 layer. For future work, we want to combine these two approaches and consider them simultaneously for manufacturing of 1D layout. Due to the larger solution space, we expect that we can obtain better solution than either one of the two approaches.

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