Transition Time Bounded Low-power Clock Tree Construction

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Abstract— **Recently power becomes a significant issue in clock network design for high-performance ICs because the clock network consumes a large portion of the total power in the whole system. Also, clock signal is the signal with the highest frequency in the whole system, which makes the transition time bound of the clock signal extremely tight. Hence, it is necessary to have transition time bounds to construct low-power clock trees in high performance systems. In this paper, we formulate the transition time bounded low-power clock tree construction problem. Buffer insertion, buffer sizing and wire sizing are employed to construct the low-power clock tree under a given transition time bound. We propose a top-down dynamic programming algorithm to solve the problem. Experimental results show that the transition time bound has a significant effect on power consumption. Therefore, we need to consider the trade-off between transition time and power consumption in clock tree design. In addition, the percentage of short-circuit power of the total power is not neglectable. Hence, it is not appropriate to neglect it. By carefully considering short-circuit power and transition time of buffers, we get accurate power consumption and transition time compared with SPICE simulation results.**

I. INTRODUCTION

Modern high-performance digital systems are designed with a target clock frequency. The clock frequency determines the processing speed of the system. Recently, as the working frequency of advanced digital systems has entered the gigahertz domain, the clock network design becomes much more challenging.

The primary objective of clock tree design is to minimize the signal skew at sinks. Other objectives are phase delay, wire length, area and power consumption. As technology advances, systems are operating at very high frequencies. This leads to much more power consumption and much shorter signal transition time. As a result, power and transition time becomes the key objectives of clock network design.

The increasing popularity of portable applications, the reliability of designs and the cost of cooling make the low power design a necessity. Clock network can consume a large percentage (15-45%) of the total system power [1]. Hence, it's important to optimize the power consumed by the clock network. As the working frequency exceeds 1GHz, the constraint of the transition time in the clock network becomes extremely tight. In state-of-the-art technologies, coupling capacitance and inductance of long wires have a significant impact on transition time. It is necessary to consider their effects in characterizing transition time. In general, the transition time should be 10-15% of the clock period [2]. Therefore, the high frequency of the system requires very small transition time. For instance, if we want to achieve 1GHz working frequency in a system, clock cycle time is 1ns and the designed transition time of the clock signal should be less than 150ps. Moreover, the transition time have effects on power consumption. Different transition time bounds will lead to different power optimization results. It is improper to optimize power without any transition time bound. There is a trade-off between the transition time and power consumption when optimizing the clock tree.

To optimize the power for clock tree, it is important to have a good estimate of power consumption. In a clock tree, wires and buffers contribute to the power consumption. For wires, the power is dissipated by charging and discharging the wire capacitance. The power consumption of buffers consists of two components. One is a switching power component, P_{SW}, which corresponds to the charging and discharging of the capacitance in buffers. The other is a short-circuit power component, P_{SC}. The first one is well characterized, but the second one has not been fully considered in the clock tree design. Short-circuit power is due to the simultaneous conduction of the PMOS and NMOS transistors during the input transitions. As power becomes a more serious problem, an accurate estimation of the power consumption is needed and in this context, studying P_{SC} is crucial for the cutting-edge VLSI technology. For the clock tree in a high-performance system, in order to achieve the short transition time and use less wire area, a large number of buffers have to be inserted in the network. The short-circuit power of the clock buffers will become a considerable part of the total power consumption. To estimate the power consumption accurately for power-driven clock tree design, we need consider the short-circuit power carefully.

Previous work on clock tree construction focused on zero or near zero-skew routing [3][4]. In addition to zero-skew, further work concentrated on routing clock tree with minimum total wire length and phase delay [5][6][7]. For the low power clock tree, Chen et al. discussed the clock power issue in SOC design in [8]. In [9], Duarte et al. studied and quantified the impact that various intensifying concerns associated with scaling will have on clock energy and their relative impact on the overall system. Their work showed the importance of clock power consumption and the necessity of considering it in design. Buffer insertion are tried to minimize the clock power by buffer insertion in [10] and [11]. Authors of [13] and [14] exploited similarities in the switching activity of the clocked modules to reduce the number of the gates for clock gating. For transition time (slew rate), Tellez et al. investigated the problem of computing a lower bound on the number of buffers required in the clock tree given a maximum clock slew rate constraint [12].

As far as we know, no work considered the trade-off between the power and transition time when optimizing the clock tree. A way to consider the transition time is trying to minimize the delay since the delay is related to the transition time. However, in the clock tree with a lot of buffers, the delay cannot characterize the transition time in the whole clock tree directly and accurately. Hence, it is necessary to give the transition time bound for all the places in the clock tree. In addition, the short-circuit power is either neglected or just mentioned without being fully considered in the optimization the clock tree.

In this paper, we formulate the transition time bounded low-power clock tree construction problem. For a balanced H-tree topology, we employ buffer insertion, buffer sizing and wire sizing to construct a clock tree which has the minimum power consumption (including switching power and short-circuit power) under a transition time bound. A dynamic programming approach is proposed to solve this problem. We carefully compute the transition time and total power consumption, which includes the switching power and short-circuit power, level by level. We also consider the area of the clock network by adding the weighted area to the objective function as a penalty so that we will not use too much chip area. Experimental results show

that the short-circuit power can be up to 17% of the total power consumption which is not a neglectable part. If the clock tree is not designed carefully, this percentage may even exceed 20%. In addition, the transition time bound affects the clock power significantly. With a tighter transition time bound, wider wires and larger buffers are used so that the power consumption of the clock tree is more than that with a looser bound. Therefore, there is a trade-off between transition time and power consumption, i.e., a trade-off between performance and power. We have to explore this design space when constructing a low power clock tree.

The remainder of the paper is organized as follows. In Section II, we formulate the transition time bounded low power clock tree construction problem. In Section III, a dynamic programming algorithm is proposed to solve the problem using buffer insertion, buffer sizing and wire sizing. Experimental results and discussions are given in Section IV. Finally, we conclude the paper in Section V.

II. PROBLEM FORMULATION

In this section, we formulate the transition time bounded low-power clock tree construction problem. In the advanced technologies, the coupling capacitance becomes dominant for the wire capacitance. In addition, the effect of the inductance becomes much more significant in the high frequency clock network today. The carefully designed shielding and routing of the H-trees result in predictable capacitive and inductive characteristics [15]. The shielding also reduces noise coupled into nearby signal lines from the clock lines. Therefore, we employ the Sandwich Balanced H-Tree (SBHT) [16] topology for the clock tree, as shown in Figure 1.

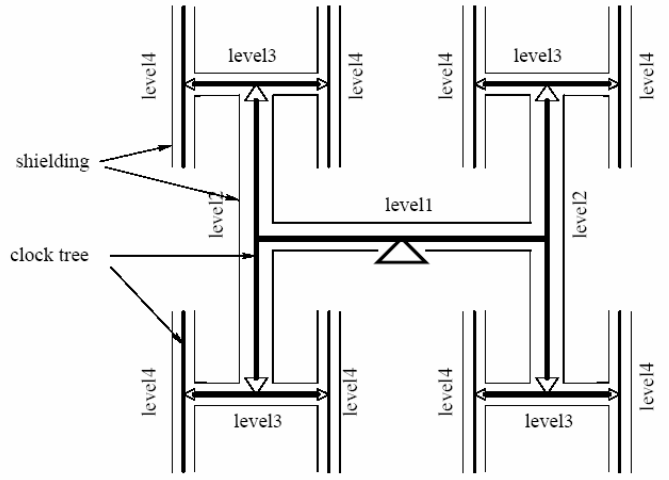

Figure 1. Sandwich Balanced H-Tree(SBHT)

Due to the balance of this kind of clock tree, we make wire width the same for all the wires in the same level and insert the same type of buffer (if needed) in the same level to achieve the zero skew. Though simple, this kind of clock tree is widely used in industry at the top level of clock network. It distributes the clock signal to many small clock regions. For those small regions, local clock tree will further send clock signal to all the sinks (flip-flops).

For a rooted clock tree T, S is the number of levels, the clock tree root buffer is B_{root} and input transition time of the root buffer $t_{in}(root)$. B_{lib} is the buffer library from which the buffers are chosen for buffer insertion. Sink buffer is B_{sink}. The bound of the input transition time for buffers is t_{bound}. The input transition time for buffers in level i is $t_B(i)$. We formulate the transition time bounded low-power clock tree construction problem as following:

Transition time bounded low-power clock tree construction problem:

Given the Sandwich Balanced H-Tree (SBHT) topology, B_{root}, $t_{in}(root)$, B_{sink}, B_{lib} and t_{bound}, construct a clock tree T to minimize the total power consumption (including switching power and short-circuit power) and area, such that $t_B(i)<t_{bound}(i=[1\ldots S])$.

III. MODEL AND ALGORITHM

A. Buffer Model and Wire Model

In this section, we present the models for buffers and wires we use in our algorithm.

For a buffer, the switching power is the power to charge and discharge capacitance in the buffer. It only depends on the buffer size. However, the transition time and short circuit power are not just related to the buffer size. The input transition time and output capacitance have effects as well. Hence, the buffer model needs to include the buffer size, input transition time and output capacitance. The buffer model is shown in Figure 2. t_{in} and t_{out} are input and output transition time of the buffer, B is the buffer type, and Cl is the load capacitance of buffer's output. Here we model the downstream circuit as a single effective capacitor.

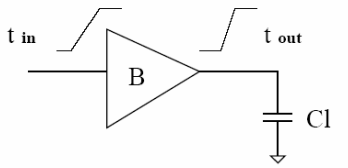

Figure 2. Buffer Model

There are many models for the output transition time and short-circuit power of buffers [18][19][20]. However, they are either not accurate or excessively complex. Therefore, we employ SPICE simulation to construct a look-up table for the buffers in the buffer library. The variables of the table is B_{type}, t_{in} and Cl. The table gives out the output transition time and short-circuit power that correspond to a (B_{type}, t_{in}, Cl) group.

For the wires, we use the Π type RLC model. The power consumed by a wire is the switching power to charge and discharge the wire capacitance. For the transition time after a wire, we employ the PERI method [21] to compute the output transition time based on input transition time and Π model of wire. According to PERI method, the output transition time is the root-mean square of the output transition time of step input and input transition time:

$$t_{out}^2 = \sqrt{t_{in}^2 + t_{step}^2} \quad (1)$$

The output transition time of step input t_{step} is computed based on RLC network charging process.

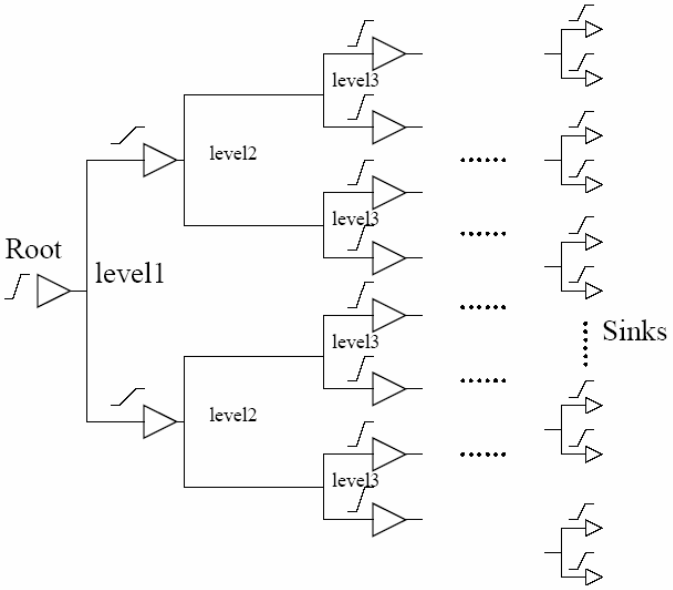

Figure 3. Buffered H-Tree

B. Dynamic Programming Algorithm

We propose a dynamic programming algorithm to solve the transition time bounded low-power clock tree construction problem formulated in Section II.

In order to achieve the low-power objective, we apply buffer insertion, buffer sizing and wire sizing in clock tree construction.

First, the H-tree is divided into several levels. Buffers are inserted at the end of wires in each level. Each level has wires with or without buffers at the end, as shown in Figure 3. (e.g., level 1 and level 3 have buffers but level 2 has no buffer in it) The inserted buffers are from the buffer library B_{lib}. For each level, discrete wire widths are chosen to do the wire sizing.

Then, based on the input transition time of the root buffer, for each possible load capacitance Cl_0 we use the model in Section III A. to get the output transition time $t_{out}(0)$ and power consumption P_0 (including switching power and short-circuit power) of the root buffer. Then, we use $t_{out}(0)$ as the input transition time of level 1 of the clock tree, $t_{in}(1)=t_{out}(0)$. We try all possible widths w_1 and load capacitance Cl_1 to compute the transition time after the wire, $t_{wire}(1)$ and power consumption of the wire capacitance in level 1, $P_{wire}(1)$. Then we consider buffer insertion in level 1, first we check whether $t_{wire}(1)<t_{bound}$ or not. If not, we neglect this solution because the transition time is out of bound. If yes, we try all buffers in the buffer library B_{lib} and compute the output transition time $t_{out}(1)$ and power consumption $P_B(1)$ (including switching power and short-circuit power) of all buffers in level 1. The total power consumption from the clock root to level 1 is obtained by $P(1)=P(0)+P_{wire}(1)+P_B(1)$. $P_B(1)=0$ when no buffers are inserted. Again, we use the output transition time of level 1 $t_{out}(1)$ as the input transition time of level 2, $t_{in}(2)= t_{out}(1)$. Using $t_{in}(2)$, we can compute the output transition time after level 2 and total power consumption of the tree from root to level 2 for each wire width w_2 and load capacitance Cl_2. We repeat this process level by level until reach the sink buffers. Transition time bound is only considered at the inputs of buffers because the worst transition time occurs after wires. Due to the limit of pages, we do not prove it here. Pruning is used to reduce the number of solutions in each level. We get the solutions $(P(i); t_{out}(i); Cl_i)(i=0...S)$ for each level, prune the worse solutions and propagate the potentially best solutions to the next level. The pruning scheme will be detailed in Part C.

Figure 4 shows the algorithm. $t_{in}(i)$, $t_{out}(i)$ and Cl_i are the input transition time, output transition time and effective capacitive load of level i, $P(i)$ is the total power from root to level i.

Algorithm for transition time bounded low-power clock tree construction problem

Input: S, B_{root}, $t_{in}(root)$, B_{sink}, B_{lib} and t_{bound}
Output: B_i (buffers inserted in level i),
w_i (wire width in level i)
for all possible Cl_0 of B_{root} do
get solutions $(P_0, t_{out}(0), Cl_0)$
for each level $i \in [1..S]$ do
for each solution $(P_{i-1}, t_{out}(i-1), Cl_{i-1})$ of level i-1
$t_{in}(i) = t_{out}(i-1)$
for each $(t_{in}(i), w_i, B_i, Cl_i)$
generate the solution $(P_i, t_{out}(i), Cl_i)$ with bound: $t_B(i) < t_{bound}$
pruning the newly gernerated solution
return the final solution $(w[1..S], B[1..S])$ with P_S is minimium

Figure 4. Algorithm

C. Pruning

In Part B, since we have many choices for the buffer sizes and wire widths, a huge number of solutions will be created. In order to reduce the run time, we prune the solutions created at each level.

We have two kinds of pruning schemes. The first one is based on the observation that for two successive levels without buffers in between, the lower level should have the same or smaller wire width. Therefore, for the two adjacent levels without buffers at the end of the higher level, we can prune the solutions with wider wires in the lower level than in the higher level. We show two levels with the wire modeled by RLC network in Figure 5. It has been proved that the higher level should use wider wires than lower level for the RC tree to get a better signal delay [22]. We believe that for the RLC tree, it is the same case.

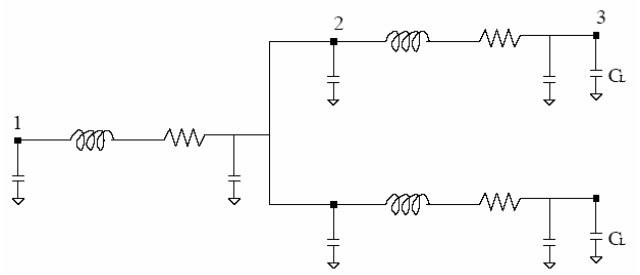

Figure 5. Transition time calculation model

The other pruning scheme is based on power and transition time. For solutions in one level, we eliminate the solutions with the same load capacitance, larger upstream (including current level) power consumption and larger output transition time at this level. We can do this kind of pruning because if the load capacitance of some level is the same, the difference between two clock trees only depends on the tree from root to this level. If one tree have larger transition time at the current level, for any downstream solution the downstream tree will consume more power due to the larger short-circuit power. That is to say, larger transition time leads to larger power consumption of downstream tree. If the upstream tree consumes more power too, the total tree will consume more power. Therefore, we can prune this solution with larger upstream (including current level) power consumption and larger output transition time.

Table 1. Technology Parameters

R_s	0.0917Ω/square
C_a	53.2aF/μm^2
C_f	14.1aF/μm
C_x	16.5aF/μm
Buffer Size	×1, ×2, ×3, ×4, ×8, ×12, ×16, ×20

IV. EXPERIMENTAL RESULTS

The parameters used in the program is based on Sandwich Balanced H-Tree (SBHT) [16], 0.1 μm technology, we use 0.05 μm as the incremental step for wire width. Area capacitance (C_a), fringing capacitance (C_f) and coupling capacitance (C_x) are considered in our model, as shown in Table 1. We have 8 buffer types in buffer library. For inductance, we use Ruehli's formula [23] for Partial Mutual Inductance and Grover's formula [24] for Partial Self Inductance.

Table 2 shows the 4 different clock trees we construct for 5, 6, 7, 8 levels on a 1cm*1cm chip under the transition time bound of 180ps. In the table, "w" means wire width, the unit is μm; "B" means the buffer type. The reported runtime is on a Linux Machine with a Xeon 3.06GHz CPU. Figure 6 shows the trade-off between the transition time bound and power consumption for 6-level clock tree. We can see that the looser the transition time bound, the less the power consumption. The power consumption under 140ps bound is about 40% more than the power consumption under 600ps bound. In fact, this trade-off is the trade-off between performance and power. More important, if we do not give any bound on transition time, we can achieve lower power consumption. However, the design will be harmed in performance.

Table 3 shows the power and transition time at sinks under the transition time bound of 180ps (our algorithm vs SPICE simulation). The unit of transition time is pico-second, and the unit of power is fJ/cycle. Our algorithm can achieve the accuracy with less than 2.5% error for sink transition time and 2% error for power consumption.

Table 2. Wire Widths and Buffer Sizes in Clock Trees

Tree Levels	1		2		3		4		5		6		7		8	Runtime
	w	B	w	B	w	B	w	B	w	B	w	B	w	B	w	
5-level	0.2	×7	0.2	×5	0.1	×5	0.1	×3	0.1							0.5s
6-level	0.2	×7	0.2	×5	0.1	×5	0.1	×4	0.1	×3	0.1					2.3s
7-level	0.2	×7	0.2	×5	0.1	×5	0.1	×4	0.1	×4	0.1	×3	0.1			17s
8-level	0.2	×7	0.2	×5	0.1	×5	0.1	×4	0.1	×4	0.1	×2	0.1	×3	0.1	2m 8s

Table 3. Sink Transition Time and Power Consumption Ours vs SPICE

# of levels	Sink Transition Time			Power Consumption		
	Ours	SPICE	Error	Ours	SPICE	Error
5	146.2	148.2	-1.35%	4287	4304	-0.39%
6	146.0	147.9	-1.28%	6552	6661	-1.64%
7	159.5	156.0	2.24%	9217	9394	-1.88%
8	159.9	156.1	2.34%	14547	14840	-1.97%

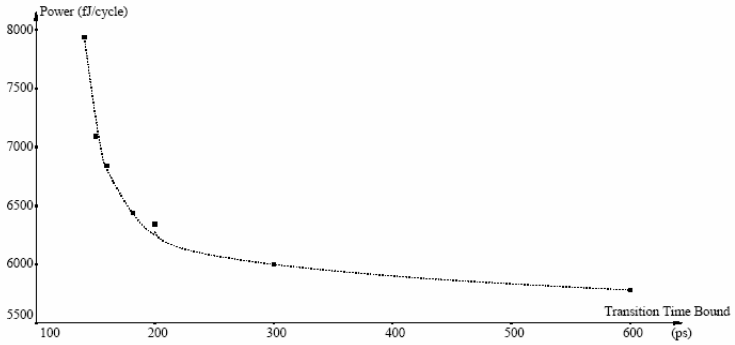

Figure 6. Transition Time Bound vs Power Consumption

The percentage of the *Psc* of total power consumption for clock trees with 5, 6, 7 and 8 levels are 17.217%, 15.673%, 16.723% and 9.966%, respectively. Therefore, the short-circuit power is not a neglectable part of the total power consumption and it has to be considered when optimizing the power.

V. CONCLUSION

To construct a low-power clock tree, it is necessary to have a transition time bound to assure the performance of the system. This bound can affect the power optimization result significantly. In addition, in order to estimate the clock power accurately for power optimization, short-circuit power needs to be considered. In this paper, we propose an effective method to construct a buffered clock tree with minimum power consumption (including switching power and short-circuit power) under a transition time bound. From the experimental results, we can see that the transition time bound has a significant effect on the power optimization result. Therefore, there is a trade-off between the power consumption and the transition time, which shows the necessity to consider these two factors at the same time in low-power clock tree optimization. The results also show that our approach is accurate in both power and transition time estimation compared with SPICE simulation results.

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