CprE 2810 HW12
ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

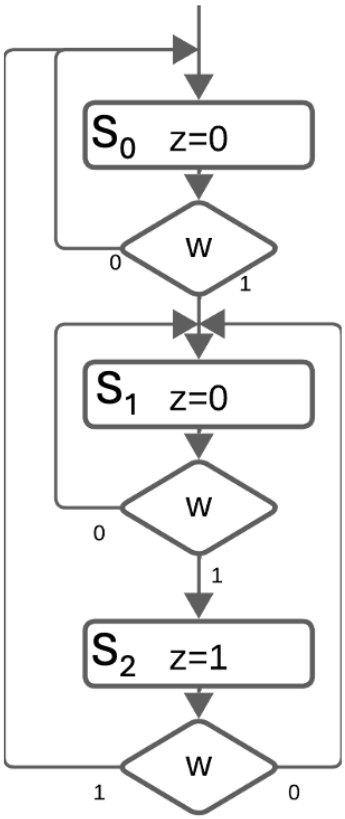
Counters, Analysis of Syn. Seq. Circuits, ASM charts/examples
Finish by Dec 1, 2025

Instructions

Complete the questions below to the best of your ability. Upload a PDF of your work to canvas.

Questions

P1 (15 points): The following ASM chart describes the control logic of a micro-chip.



a) (5 points) Is this a Moore or a Mealy machine? Justify your answer.
b) (5 points) Draw an equivalent state diagram of this chip.
c) (5 points) Derive the state table for this chip.

P2 (20 points): Design a synchronous 3-bit counter that cycles through the following sequence: 2 → 4 → 6 → 1 → 3 → 5 → 7 and then repeats. Use JK Flip-Flops.

a) (5 points) Draw the state diagram.
b) (10 points) Derive the state-assigned table and the JK excitation table for all three Flip-Flops.
c) (5 points) Write the simplified logic expressions for the J and K inputs of the most significant bit (MSB) Flip-Flop.

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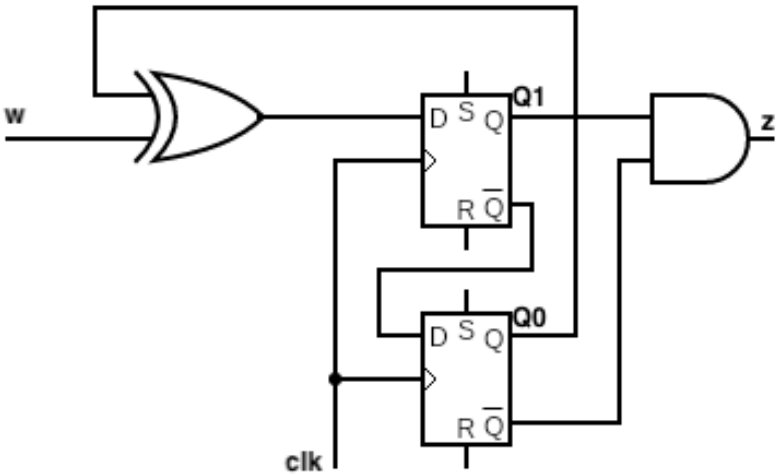
P3 (15 points): Derive the state table for the following circuit that uses positive-edge-triggered D Flip-Flops. What sequence of input values (W) causes the output Z to become 1? Assume the initial state (after reset) is Q1 Q0 = 00.



a) (10 points) Derive the state-assigned table and state table. (Present State Q1 Q0, Input w, Next State Y1 Y0, Output z).
b) (5 points) Draw the state diagram of this circuit.

P4 (20 points): Design an FSM with a single input W and an output Z. The circuit should detect three consecutive 1s on W. If W=1 for three or more consecutive clock cycles, Z should be 1. Otherwise, Z should be 0. Your circuit must use two positive-edge-triggered T Flip-Flops and a minimal number of other gates.

a) (5 points) Draw the state diagram. Don't forget the reset signal. Label states clearly (e.g., S0, S1, S2).
b) (10 points) Derive the state-assigned table. This table must include the present state, input, next state, output, and the excitation values for the T Flip-Flops.
c) (5 points) Write the simplified logic expressions for the T inputs (T1, T0) and the output Z.

P5 (30 points): Consider a counter that has a special counting sequence: 0,4,5,1,0,4,5,1, and so on. Design this counter with minimal number of states.

a) (5 points) Draw the state diagram for the counter
b) (5 points) Construct the state-assigned table including the next state and output
c) (10 points) Draw the circuit diagram using T flip-flops
d) (10 points) Draw the circuit diagram using JK flip-flops