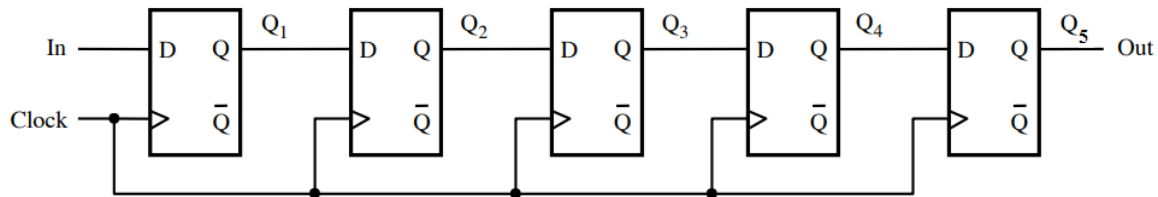


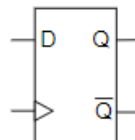
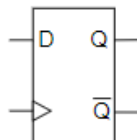
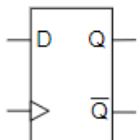
P1. (10 points): Complete the following table for the shift register shown below with the original values $Q_1Q_2Q_3Q_4Q_5$ Equivalent to 01010. Assume that each row represents one clock cycle.



Clock Cycle	In	$Q_1Q_2Q_3Q_4Q_5$
0	1	01010
1	1	
2	0	
3	1	
4	0	
5	0	
6	1	
7	0	

P2. (10 points) Complete the following circuit diagram to implement a 3-bit register. You may use any other logic gates or components to finish your work. The register has two control inputs (C1 and C0), three parallel input lines (I2, I1, and I0), and three output lines (Q2, Q1, and Q0). Depending on the values of C1 and C0, the register performs one of the four operations shown in this table. Clearly label all inputs, outputs, and pins.

C1	C0	Operation
0	0	Synchronous Reset (i.e., new $Q_2=0$ $Q_1=0$ $Q_0=0$)
0	1	Cyclic Shift Left (i.e., new $Q_2=Q_1$, new $Q_1=Q_0$, new $Q_0=Q_2$)
1	0	Cyclic Shift Right (i.e., new $Q_2=Q_0$, new $Q_1=Q_2$, new $Q_0=Q_1$)
1	1	Hold the current value (i.e., Q_2 Q_1 Q_0 stay unchanged)



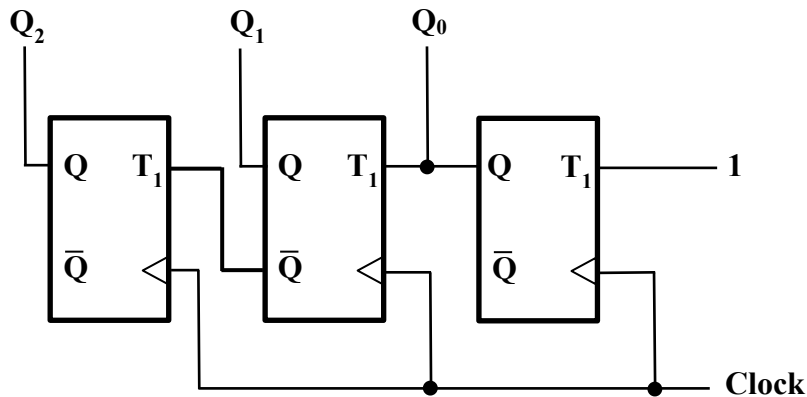
P3. (10 points)

Design a minimal cost circuit that implements the 4-input function $F = ((A \cdot B) + C) \cdot D$ using only 2-input NOR gates.

- (7 points) Draw the complete circuit diagram. Clearly label all inputs (A, B, C, D) and the output (F).
- (3 points) Prove the correctness of your design using Boolean algebra.

P4. (10 points)

For the counter shown below, list its **counting sequence** starting from state $Q_2Q_1Q_0=001$. Give the sequence in **binary** and the corresponding **hex** values. Continue until the sequence repeats.



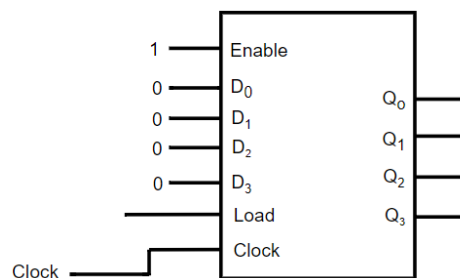
P5. (10 points)

Draw the following circuits:

- (5 points) Draw a circuit for a 3-bit synchronous up-counter using JK flip-flops.
- (5 points) Draw a circuit for a 4-bit asynchronous up-counter using D flip-flops.

P6. (15 points)

The figure below shows the starting design of a 4-bit counter with reset synchronization. Complete the circuit to make a modulo-10 counter. That is, the counting sequence is 0 – 9, then repeating. Explain your solution and give the Boolean expression for the Load input.



P7. (20 points) Consider an FSM with the following state table:

Present State	Next State		Output
	W=0	W=1	
A	A	B	0
B	A	C	1
C	C	D	2
D	C	A	3

- a) (4 points) Draw the state Diagram from the State Table:
- b) (4 points) Encode each state and outputs in (a) with binary numbers to build the following state-assigned table:

Present State Y_1Y_0	Next State		Output Z_1Z_0
	W=0 Y_1Y_0	W=1 Y_1Y_0	

- c) (4 points) Derive the minimal logic expressions for Y_1 , Y_0 , z_1 , and z_0 .
- d) (4 points) Draw the complete circuit diagram using D flip-flops and any additional logic gates required.
- e) (4 points) What does this FSM do? What happens when $w=0$? When $w=1$?

P8. (15 points) Register file with two write ports.

The lectures described a register file with four registers (each 2-bits wide) with one write port and one read port. Your task here is to modify that design to accommodate a second write port.

- a) (5 points) List the new components that you plan to add.
- b) (5 points) Explain your idea and how you plan to arbitrate between the two write ports, especially when they attempt to write to the same register.
- c) (5 points) Draw the circuit diagram for your register file.