CprE 2810 HW7

ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

Multiplexers and Decoders

Assigned Date: Eighth Week
Finish by Oct. 20, 2025

P1 (10 points). Design and construct a hierarchical multiplexer system.

a. Design a 8-to-1 multiplexer using a minimal number of 2-to-1 multiplexers. Draw the block diagram and clearly label all signals, including control lines.

b. Design a 8-to-1 multiplexer using a minimal number of 4-to-1 multiplexers. Draw the block diagram and clearly label all signals, including control lines.

P2 (15 points). Consider the following Boolean function:

$$F(A,B,C) = AB'C + A'B'C$$

a. Draw the truth table for this function.
b. Use the hierarchical divide-and-conquer method to partition the truth table. Write the value of the function for each of the smallest partitions. This will help you design the circuit in part c. Hint: the first partition is by A; the second partition is by B, but it is performed twice.
c. Draw a logic circuit that implements this function using **only** 2-to-1 multiplexers. No other logic gates are allowed. If you need to negate a signal you must use a multiplexer for that as well. Clearly label all signals and show the connections between the multiplexers. `

P3 (10 points). Implement a 3-to-8 decoder with enable using **only** 2-to-4 decoders with enable. How many do you need? Draw a circuit diagram.

P4 (15 points). Consider the Boolean function:

$$F(x,\ y,\ z) = x\overline{y} + xz + \overline{x}\,\overline{y}\,z$$

a. Derive a new expression that uses Shannon's theorem, with respect to x.
b. Derive a new expression that uses Shannon's theorem, with respect to y.
c. Derive a new expression that uses Shannon's theorem, with respect to z.

P5 (10 points). Answer the following questions about decoders and multiplexers. For all subparts, please explain your reasoning. Assume that all decoders are decoders with enable. No need to draw circuit diagrams for this problem.

a. How many 3-to-8 decoders and 8-to-256 decoders would you need if you must construct a 11-to-2048 decoder? Explain.

b. How would you implement a 256-to-1 multiplexer using a combination of 8-to-1 and 2-to-1 multiplexers? Explain.

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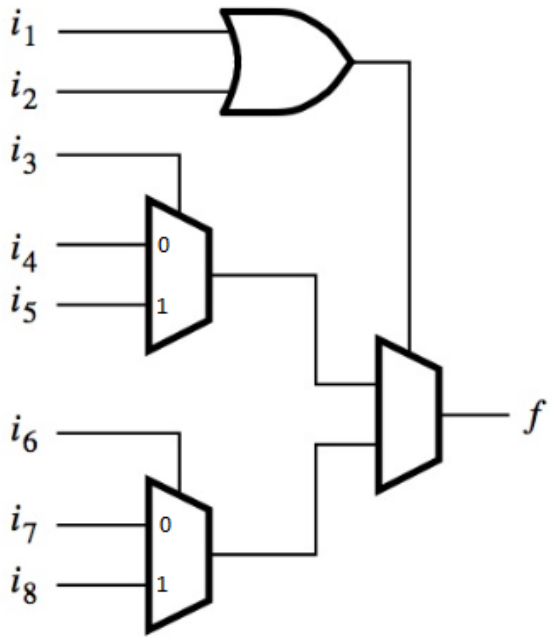
P6 (15 points). Consider the multiplexer-based circuit illustrated below. Show how this Boolean function

$$f(w_1, w_2, w_3) = w_1 \overline{w_2} w_3 + w_2 \overline{w_3} + w_1 w_2 w_3$$

can be implemented using only one instance of the provided circuit. Clearly explain how each input and selector in the circuit is used to implement the given function. Clearly state which signal is provided to which of the 'i' inputs. Assume that the variables w_1, w_2, and w_3 are given to you only in non-inverted form. The constants 0 and 1 are also provided.



P7 (10 points). Implement this function using **only** 4-to-1 multiplexers and no other logic gates

$$f = \overline{a}\, b\, \overline{c} + \overline{a}\, \overline{b}\, \overline{c} + a\, c$$

Start by rewriting the expression using Shannon's theorem such that it has four terms. Then, use only 4-to-1 multiplexers for the implementation. The inputs a, b, and c are available **only** in their non-inverted form. You can use the constants 0 and 1 as well.

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P8 (15 points). Implement the following functions using a single 4-to-1 multiplexer. Use the given variables for select lines and apply Shannon's theorem to derive an expression with four terms. Then, draw a circuit with one 4-to-1 Mux.

You may assume that you have additional gates readily available to implement the inputs of the multiplexer, but you don't need to use them. That is, for this problem, you only need to write a Boolean expression for each of the four inputs of the multiplexer. Use the simplified SOP expression for each of the inputs.

a. $F(A, B, C, D) = \sum m(0,2,4,7,9,10,11,13)$ with select lines A and B

b. $G(A, B, C, D) = \sum m(1,3,4,6,8,10,15)$ with select lines B and C

c. $H(A, B, C, D) = \prod M(0,2,5,6,9,11,12,13,14,15)$ with select lines C and D