Cpr E 281 HW04 ELECTRICAL AND COMPUTER ENGINEERING IOWA STATE UNIVERSITY

Minimization and Karnaugh Maps Assigned: Week 4 Due Date: Sep. 22, 2025

P1 (20 points): Given the behavioral Verilog code below:

```
module Q1(f, a, b, c);
output f;
input a, b, c;
assign f = (~(a | c) & b) | ~(c | ~(a & b);
endmodule
```

- a. Draw the circuit diagram.
- b. Rewrite using structural Verilog.

P2 (20 points): Given the logic expression $F(w, x, y, z) = \sum m(1, 5, 12, 14)$

- a. Draw the circuit for the expression F.
- b. Use a K-map to derive the simplest SOP expression for F.
- c. Redraw the circuit for F using the simplified SOP expression from b.
- d. Compare the costs of the circuits implementing the expressions in parts a and c in terms of the total number of gates plus the total number of inputs.

P3 (15 points): Given the expression $Q = \bar{A}BC\bar{D} + A\bar{B}C + A\bar{D}B + A\bar{B}\bar{C}\bar{D}$

- a. Use a K-map to derive the simplest POS expression for Q.
- b. Use a K-map to derive the simplest SOP expression for Q.
- c. Determine which circuit would produce a lower cost and draw that circuit.

P4 (15 points): Use Karnaugh Maps to derive the simplified POS expressions that correspond to the following expressions:

```
a. F(W,X,Y,Z) = \sum m(3,5,6,7,11,13,14,15)
b. Q(A,B,C,D) = (\overline{B} + C + D)(\overline{A} + B + C + D)(C + \overline{B})(\overline{C} + \overline{A} + \overline{D})
c. Z(I,K,L,M) = M\overline{K}\overline{L} + \overline{I}L\overline{K} + \overline{K}L
```

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P5 (20 points): Design a logic circuit with four inputs: a_1 , a_0 , b_1 , and b_0 . Let a_1 , a_0 represent the two-bit number A, while b_1 , b_0 represents the two-bit number B. The output of the circuit, F, should be 1 if and only if the sum of the two-bit values A + B is an even non-zero sum. Otherwise, F should be 0.

- a. Construct the truth table for this function, F.
- b. Using a K-Map, derive the simplest SOP expression.
- c. Draw the logic circuit based on the simplified SOP expression.
- d. Implement your simplified expression in Verilog.

P6 (10 points): For each expression below, derive the simplest POS expression using don't care terms for simplification wherever possible:

a.
$$Q_1(A, B, C) = \prod M(0, 2, 6, 7) + D(4, 5)$$

b.
$$Q_2(W, X, Y, Z) = \sum m(0,1,5,8,10,11,15) + D(3,4,13,14)$$