CprE 2810 EC-Lab
ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

Binary to Base64-Hex & LCD

Due: December 8, 2024

Extra Credit Lab (extra 1.5%)

In this assignment, you will create a Binary to Base64-Hex Converter and a register file with two read ports. The output of each read port will be mapped to a fixed position in the Liquid Crystal Display (LCD). You will then display the contents of two registers as characters on the LCD of the FPGA.

Disclaimers: Please read through the whole document before starting with this lab. DO NOT make changes to any of the provided files unless the instructions explicitly tell you to do so. Finally, please complete Lab 12 before attempting this lab.

How does the LCD work:

Download EC_Lab.zip and unzip it. Inside the folder is a project file labeled 'EC_Lab.qpf'. The LCD module consists of three essential files: LCD.v, LCD_Display.v, and reset_delay.v. You will also find a block of the LCD file in the BDF file. This file takes the 50 MHz clock and the data to be displayed in binary and outputs commands and data to the LCD. The reset_delay acts like a clock and allows for the initialization of the LCD. Finally, the LCD_Display module produces all of the commands and data that will be sent to the LCD.

Part 1: 6-bit Register File

For this part, create a register file with 8 registers and 2 read ports. Each register must be 6-bits wide. To accomplish this, start by copying your files from **lab12step2** (**regfile.v**, **Decoder3to8.v**, **Mux8_4b.v**, **reg4b.bdf**, **register.bsf**, and **register.bdf**). Add two more registers to your "reg4b". Then, change the input and output widths for the "Mux8_4b" from 4 bits to 6 bits.

Now open "regfile.v". Make the DATAP and DATAQ wires into outputs and remove the original outputs. Change the input and output data widths as well. Generate the symbol file for this new register file.

Part 2: 6-bit to Base64-Hex Converter

Open "base64.v". This module will take a 6-bit binary number and output its equivalent in Base64-Hex. The output is an 8-bit binary number equal to the ASCII value of the Base64 digit. The table on the next page shows the decimal, Base64, and ASCII hexadecimal equivalents of 1 digit in Base64. Use the table and case statements to create the Converter in "base64.v".

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Decimal	Base64	ASCII Hex
0	A	41
1	B	42
2	C	43
3	D	44
4	E	45
5	F	46
6	G	47
7	H	48
8	I	49
9	J	4A
10	K	4B
11	L	4C
12	M	4D
13	N	4E
14	O	4F
15	P	50
16	Q	51
17	R	52
18	S	53
19	T	54
20	U	55
21	V	56
22	W	57
23	X	58
24	Y	59
25	Z	5A
26	a	61
27	b	62
28	c	63
29	d	64
30	e	65
31	f	66

Decimal	Base64	ASCII Hex
32	g	67
33	h	68
34	i	69
35	j	6A
36	k	6B
37	l	6C
38	m	6D
39	n	6E
40	o	6F
41	p	70
42	q	71
43	r	72
44	s	73
45	t	74
46	u	75
47	v	76
48	w	77
49	x	78
50	y	79
51	z	7A
52	0	30
53	1	31
54	2	32
55	3	33
56	4	34
57	5	35
58	6	36
59	7	37
60	8	38
61	9	39
62	+	2B
63	/	2F

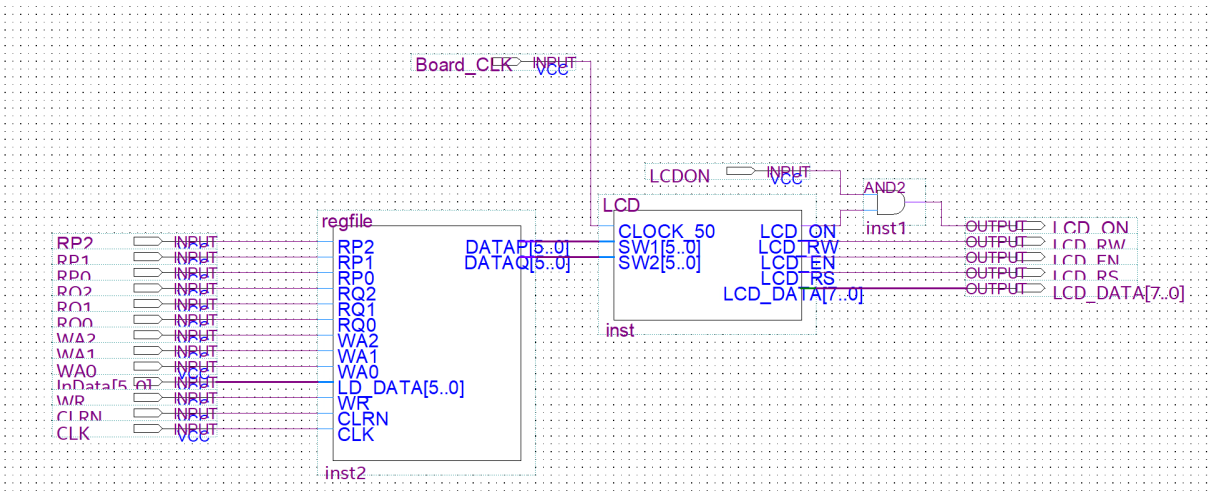
Part 3: Testing the Converter

Open "EC_Lab.bdf". You will see multiple Input and Output Pins, some of which have already been assigned. You will also see the symbol file for the LCD module. **Do Not Make Any Changes to the Pins and Assignments Provided.**

Add the Register File symbol to EC_Lab.bdf and connect all wires as given in the image below. Also, assign all the remaining pins in the same way as in **lab12step3.** In case some pins do not work on the board, include a table of the pin assignments changed in your writeup.

You can now input 6-bit numbers into the register file and use the LCD to view the contents of two registers (those that are selected on the read ports). Use the "LCDON" input to view output on the LCD. Since DATAP is wired to SW1 and DATAQ is wired to SW2, the output on the LCD will be "OUTPUT: {DATAP}{DATAQ}", where {DATAP} is the Base64 equivalent of DATAP and {DATAQ} is the Base64 equivalent of DATAQ.

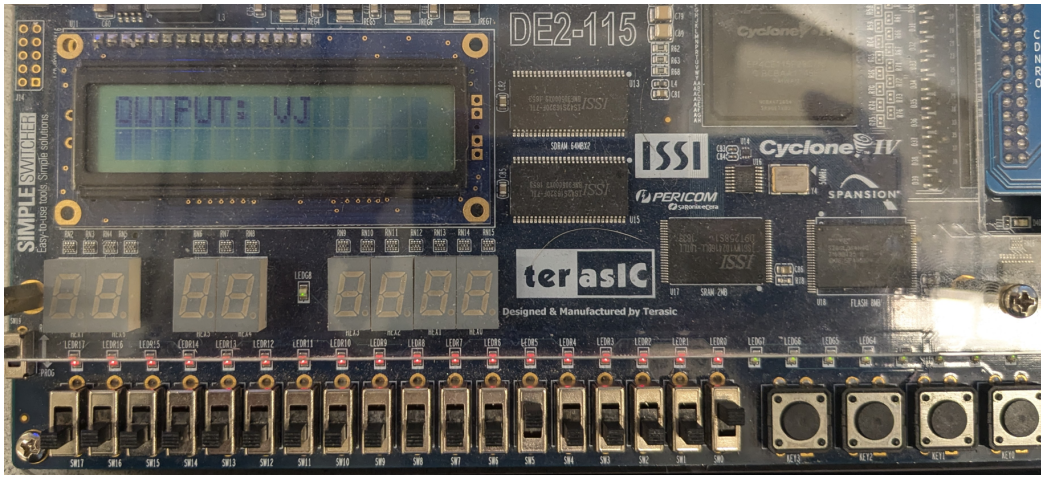
As you can see in the image, the read ports DATAP and DATAQ have been wired to the LCD inputs SW1 and SW2, respectively. This allows for any two registers to be mapped to the LCD, based on your RP and RQ values. For simplicity of testing, you may use only Registers Reg[0] and Reg[1].



What/How to Submit:

To get credit for this assignment, you need to submit a zip file on Canvas with your project files and a writeup by December 8, 2024 (at midnight). In addition, you must demonstrate your project to your TA during the time of lab 13 the following week.

You must include 3 pictures of the board in your writeup, which is part of your zip file. The first picture must show the configuration of the switches when you enter the first letter of your First Name in Reg[0]. The second image should show the same for the first letter of your Last Name in Reg[1]. The final image must show the LCD displaying your initials. An example Final Image is given below for the name Varun Jain.



Additional Reading:

https://homepages.thm.de/~hg53/hes-ws2122/aufgabe1/de2-115_mb.pdf

https://www.crystalfontz.com/products/document/936/CFAH1602B-NGG-JTVDatasheet_Rel2021-09-01.pdf

https://community.intel.com/t5/FPGA-SoC-And-CPLD-Boards-And/LCD-interfacing-with-the-de1-board/td-p/183470?attachment-id=38390