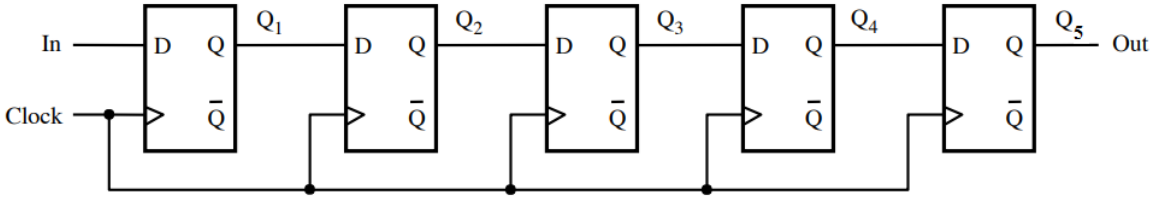
CprE 2810 HW10
ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

Registers & Counters
Finish by Nov. 11, 2024

P1. (10 points): Complete the following table for the shift register shown below. Assume that each row represents one clock cycle.

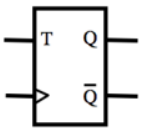


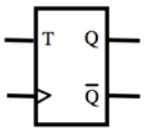
Time	In	Q_1	Q_2	Q_3	Q_4	Q_5
t=0	0	0	1	0	0	1
t=1	1					
t=2	0					
t=3	0					
t=4	1					
t=5	0					
t=6	1	0	1	0	0	1

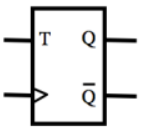
P2. (10 points) Complete the following circuit diagram to implement a 3-bit register. You may use any other logic gates or components to finish your work. The register has two control inputs (C1 and C0), three parallel input lines (I2, I1, and I0), and three output lines (Q2, Q1, and Q0). Depending on the values of C1 and C0, the register performs one of the following four operations:

C1	C0	Operation
0	**0**	**Hold the current value (i.e., Q2 Q1 Q0 stay unchanged)**
0	**1**	**Cyclic shift left (i.e., new Q2=Q1, new Q1=Q0, new Q0=Q2)**
1	**0**	**Load new data (i.e., new Q2=I2, new Q1=I1, new Q0=I0)**
1	**1**	**Invert all bits (i.e., new Q2=$\overline{Q}$2, new Q1=$\overline{Q}$1, new Q0=$\overline{Q}$0)**

Clearly label all inputs, outputs, and pins.



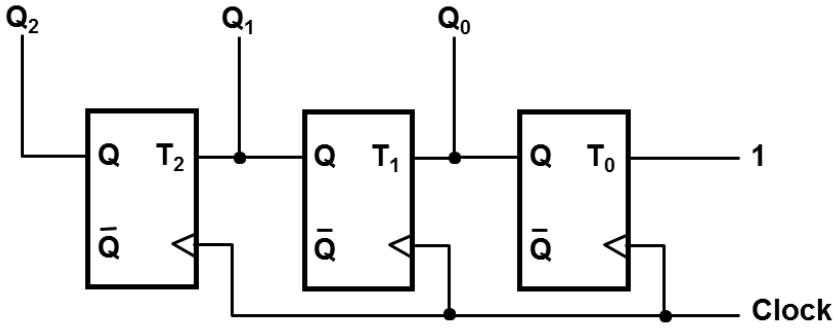




P3. (10 points)
For each subproblem draw a circuit and prove your solution using Boolean algebra.

- **a)** Implement a 3-input NAND gate with only 2-input NAND gates.
- **b)** Implement a 4-input NOR gate with only 2-input NOR gates.

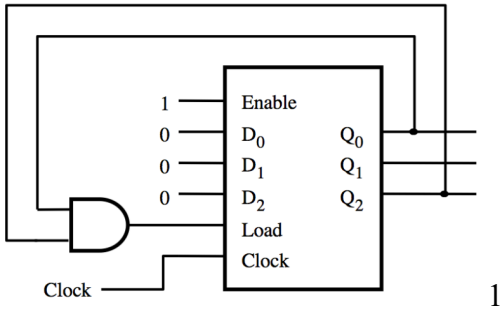
P4. (10 points)
What is the counting sequence of the following counter?
Assuming that the counter starts from $Q_2Q_1Q_0 = 000$.



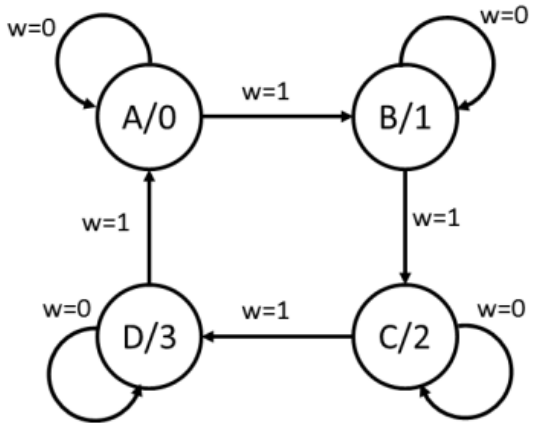
P5. (20 points)
Draw the following circuits:

a) (5 points) Draw a circuit for a 4-bit asynchronous up-counter using T flip-flops.
b) (5 points) Draw a circuit for a 4-bit synchronous up-counter using T flip-flops.
c) (5 points) Draw a circuit for a 3-bit synchronous up-counter using D flip-flops.
d) (5 points) Draw a circuit for a 3-bit ring counter using D flip-flops.

P6. (10 points)
The figure below shows the design of a modulo-6 counter with reset synchronization. Modify the circuit and make it a modulo-4 counter instead? That is, the counting sequence should be: 0, 1, 2, 3, 0, 1, 2, 3, 0, 1, and so on. Explain your solution.



P7. (20 points) Consider an FSM with the following state diagram:



a) (4 points) Complete the following state table based on the state diagram:

Present State	Next State		Output
	W=0	W=1	
A	A	B	0
B			
C			
D			

b) (4 points) Encode each state and outputs in (a) with binary numbers to build the following state-assigned table:

Present State Y_1Y_0	Next State		Output Z_1Z_0
	W=0 Y_1Y_0	W=1 Y_1Y_0	

c) (4 points) Derive the minimal logic expressions for Y1, Y0, z1, and z0.
d) (4 points) Draw the complete circuit diagram using D flip-flops and any additional logic gates required.
e) (4 points) What does this FSM do? What happens when w=0? When w=1?

P8. (10 points) Implement a JK Flip-Flop with a T Flip-Flop and any additional logic gates. Explain your solution. Provide your derivations of the characteristic table and the expressions for J and K. Draw the circuit diagram.