Cpr E 281 HW04
ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

Minimization and Karnaugh Maps
Assigned: Week 4
Due Date: Sep. 23, 2024

P1 (20 points): Given the behavioral Verilog code below:

```
module Q1(f, a, b, c);
    output f;
    input a, b, c;
    assign f = (~(a&c)|b)&(c|(~a&b);
endmodule
```

1. Draw the circuit diagram
2. Rewrite using structural Verilog

P2 (20 points): Given the logic expression F = $AB\bar{C}D + ABCD + ABC\bar{D} + A\bar{B}\bar{C}D$

a. Draw the circuit for the expression F
b. Use a K-map to derive the simplest SOP expression for F
c. Redraw the circuit for F using the simplified SOP expression from b
d. Compare the costs of the circuits implementing the expressions in parts a and c in terms of the total number of gates plus the total number of inputs

P3 (15 points): Derive the simplified SOP expressions that correspond to the following K-maps:

F_1

C \ AB	00	01	11	10
0	0	1	1	1
1	1	0	1	0

F_2

YZ \ WX	00	01	11	10
00	0	1	0	0
01	1	0	1	1
11	1	1	0	0
10	0	0	1	0

F_3

YZ \ WX	00	01	11	10
00	0	1	0	1
01	0	0	1	0
11	1	0	1	0
10	1	1	0	1

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P4 (15 points): Derive the simplified POS expressions that correspond to the following K-maps:

F_1

C \ AB	00	01	11	10
0	0	0	0	1
1	1	0	1	1

F_2

YZ \ WX	00	01	11	10
00	1	1	0	1
01	0	0	1	0
11	0	0	0	1
10	1	1	0	1

F_3

YZ \ WX	00	01	11	10
00	1	0	0	1
01	0	1	0	1
11	0	1	0	0
10	1	0	0	1

P5 (10 points): Use Karnaugh Maps to convert the following expressions to simplified SOP expressions:

a. $Q_1(A,B,C,D) = AB\bar{C} + AB + BC\bar{D} + A\bar{B}\bar{C}D$

b. $Q_2(A,B,C,D) = \sum m(1,3,4,7)$

P6 (10 points): Use Karnaugh Maps to convert the following expressions to simplified POS expressions:

a. $Q_1(A,B,C,D) = (A + \bar{B} + D)(\bar{A} + \bar{B} + C)(A + C + D)(B + \bar{D})$

b. $Q_2(A,B,C,D) = \prod M(2,5,7,9)$

P7 (10 points): For each expression below, derive the simplest SOP expression using don't care terms for simplification wherever possible:

a. $H_1(a,b,c) = \sum m(0,3,6,7)$ + D(1,4)

b. $H_2(a,b,c,d) = \prod M(1,5,9,11,13)$ + D(3,6,7,10)