Name and Student ID:\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ Lab Section:\_\_

Date:\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

**PRELAB:**

**Q1.** Read section 3.0 and fill in the truth table below for Design 1 (*the farmer’s problem*). Then use it to construct the POS expression.

|  |  |  |  |
| --- | --- | --- | --- |
| **Cabbage** | **Goat** | **Wolf** | **Alarm** |
| 0 | 0 | 0 |  |
| 0 | 0 | 1 |  |
| 0 | 1 | 0 |  |
| 0 | 1 | 1 |  |
| 1 | 0 | 0 |  |
| 1 | 0 | 1 |  |
| 1 | 1 | 0 |  |
| 1 | 1 | 1 |  |

POS Logic Expression: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

TA Initials: \_\_\_\_\_\_\_\_\_

**Q2.** Read section 4.0 and fill in the truth table below for Design 2 (*adding the farmer*). Then use it to construct the SOP expressions.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Farmer** | **Cabbage** | **Goat** | **Wolf** | **Alarm** |
| 0 | 0 | 0 | 0 |  |
| 0 | 0 | 0 | 1 |  |
| 0 | 0 | 1 | 0 |  |
| 0 | 0 | 1 | 1 |  |
| 0 | 1 | 0 | 0 |  |
| 0 | 1 | 0 | 1 |  |
| 0 | 1 | 1 | 0 |  |
| 0 | 1 | 1 | 1 |  |
| 1 | 0 | 0 | 0 |  |
| 1 | 0 | 0 | 1 |  |
| 1 | 0 | 1 | 0 |  |
| 1 | 0 | 1 | 1 |  |
| 1 | 1 | 0 | 0 |  |
| 1 | 1 | 0 | 1 |  |
| 1 | 1 | 1 | 0 |  |
| 1 | 1 | 1 | 1 |  |

Canonical SOP Logic Expression: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

Simplified SOP Logic Expression: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

TA Initials: \_\_\_\_\_\_\_\_\_

**LAB:**

**3.0** Simulation results demonstrate correct code. TA Initials:

Schematic (FPGA) \_\_\_\_\_\_\_\_

Structural (ModelSim) \_\_\_\_\_\_\_\_ Behavioral (ModelSim) \_\_\_\_\_\_\_\_

**4.0** Simulation results demonstrate correct code. TA Initials: \_\_\_\_\_\_\_\_\_