Cpr E 281 LAB1
ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

Introduction to FPGA Programming in Quartus Prime, and the DE2-115 Development and Education Board

PRELAB!

Read the entire lab and **complete** the prelab questions (Q1-Q3) on the answer sheet **before** coming to the laboratory.

1.0 Objectives

In this lab you will get familiar with the concept of using the computer as an experimental tool, to enforce the theory learned in class. You will also have an introduction to the CAD (computer aided design) tool we will be using in this course: **Altera Quartus Prime**. And, you will learn to use truth tables, logic expressions, and circuit design. We will apply the knowledge using the DE2-115 board to observe how these concepts relate to each other.

2.0 Setup

The laboratory is equipped to provide hardware and software needed to perform the labs. A TA should also be present and is a good resource for questions. The time you spend in lab will be more productive, and you will have a better lab experience if you read, and complete, as much of the lab as possible before you arrive. When you arrive at the lab you should find an available desktop computer. You should also have a lab answer sheet. Record your answers to the questions on the answer sheet and then hand it in when the lab is completed (don't forget to write your names).

To begin, create a file folder for CPRE 281 inside your network drive directory (**U:\ Drive**). Each lab will eventually have its own subfolder inside **U:\CPRE281.**

Download zipped lab files from the course webpage on Blackboard/course website and **extract the files** into **U:\CPRE281.** Now you should have path **U:\CPRE281\Lab01** for Lab #1 files in your network drive directory. Ask your TA if you need assistance.

You are ready to run **Quartus Prime** software. Click on the Windows Start Button go through **Intel FPGA 20.1.1.720 Standard Edition** then click on **Quartus (Quartus Prime 20.1)** to run the software.

Open a file in Quartus Prime

- Left-Click on the *Open File* icon from the icon bar (second icon from your left), or select **File>Open Project** from the dropdown menu.
- Click on the downward arrow in the **Address bar** box. Make sure the directory looks like **U:\CPRE281\Lab01\…\lab1step1**; navigate to the file from the U:\ via "This PC" if it does not. It is important that the address begins with U:\ and not "\\my.files.iastate.edu\"; Quartus 20.1 will not compile from filepaths that begin with the latter.

- Select ***lab1step1.qpf*** (ensure the file extension is *.qpf*, otherwise you will not be able to compile) and click **Open**.
- Click Yes on the Dialog box to upgrade project if it opens up.

A simple AND circuit

- The circuit has already been started for you, and it should have two inputs labeled A and B, and is missing an output. Double-click on the **lab1step1** icon in the **Project Navigator** window to view the **Block Design File (*lab1step1.bdf)***.
- In order to create the output pin double click on the blank area to the right of the circuit. This will bring up the **Symbol** dialog. In the **Name** field type "**output**" and then press **OK**. Left-click to place the output pin on the diagram.
- The pin can be renamed by double-clicking on the pin (you may also right click on it and select **Properties**). Rename the output pin to C.
- Connect pin C to the output of the AND gate by dragging it over so that the pin touches the output of the AND gate and releasing it. Then you can grab it again and move it away from the AND gate and a wire should appear connecting the two.

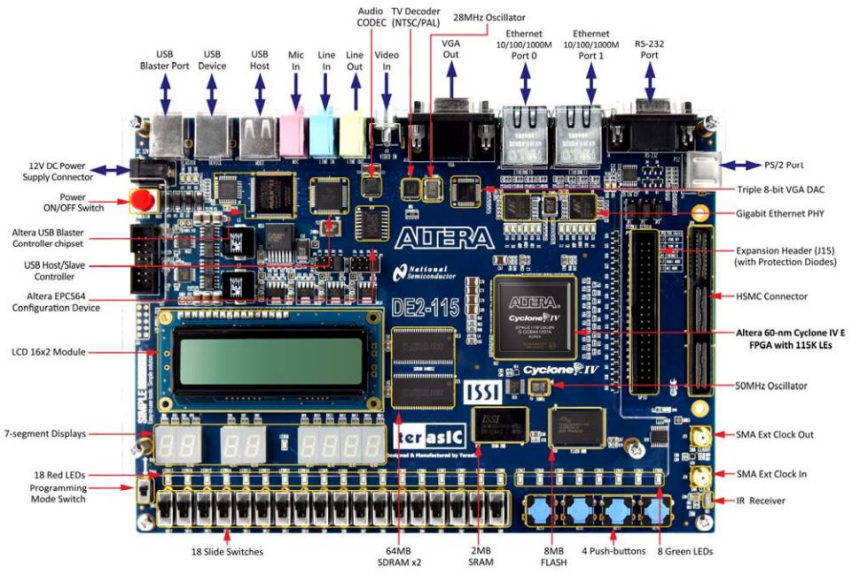
Compile the circuit

- Select **Processing>Start Compilation** (save your changes if prompted).
- A warning dialogue box may pop up when the compilation is finished. Ignore the warnings for now and click the *OK* button. If you have any other errors fix them now.

3.0 Hardware Testing – DE2-115 Board

The DE2-115 board contains a Field Programmable Gate Array (FPGA). This chip is a fabric of gates that can be programmed in order to create digital circuits. The FPGA can be programmed with the digital circuit you just created. The DE2-115 board also contains a variety of switches, LEDs, an LCD, seven segment displays, and many other I/O devices. The FPGA is directly connected to the devices on the DE2-115 board. By assigning the appropriate pin on the FPGA your circuit can be wired to the various I/O devices. For example, you can wire the toggle switches to the inputs of your circuit, and an LED to the output of your circuit.

Make sure that your DE2-115 board has 12V DC Power connected, and the USB cable connected to the USB Blaster Port. Then turn ON your board. Also make sure that the RUN/PROG switch on the board is set to RUN. The PROG selection is only used for active serial programming (AS mode), and we need to be in JTAG mode which is the RUN selection.



DE2-115 Specifications

FPGA

- Cyclone IV EP4CE115F29C7 FPGA and EPCS64 serial configuration device

I/O Devices

- Built-in USB Blaster for FPGA configuration
- 2 Gigabit Ethernet, RS-232, Infrared receiver
- Video Out (VGA 8-bit DAC)
- Video In (NTSC/PAL/SECAM/Multi-format)
- USB 2.0 (type A and type B)
- PS/2 mouse or keyboard port
- Line-in, Line-out, microphone-in (24-bit audio CODEC)
- Expansion header (38 signal pins)
- Mezzanine card

Memory

- 2 64-MB SDRAM, 2-MB SRAM, 8-MB Flash
- SD memory card slot

Switches, LEDs, Displays, and Clocks

- 18 slide switches
- 4 debounced pushbutton switches
- 18 red LEDs, 9 green LEDs
- Eight 7-segment displays

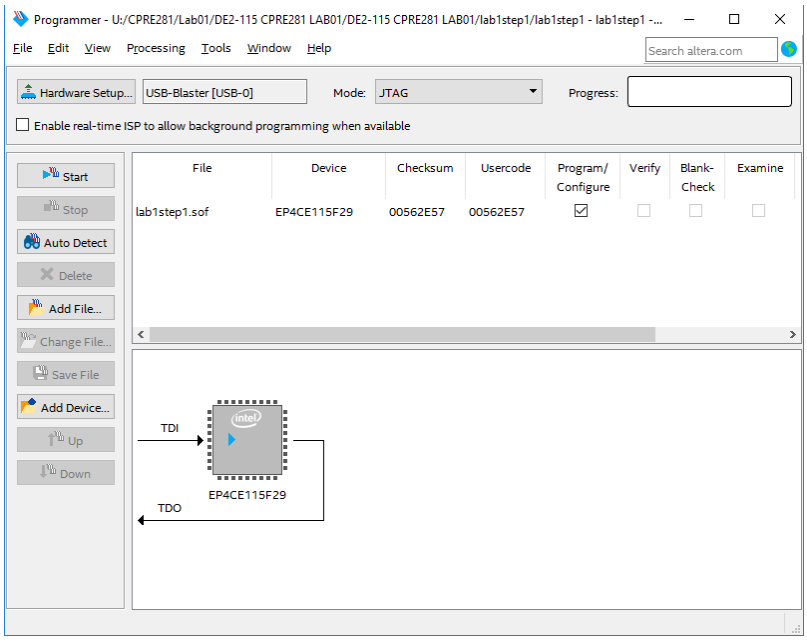
- 16 x 2 LCD display
- 50-MHz oscillator, 2 external SMA clock input/output

Assigning Pins

- Open the Pin Planner - **Assignments>Pin Planner.**
- Double-click in the *Location* cell for input pin A. This should bring up a drop down menu. Select **PIN_AD21** then press *Enter*. PIN_AD21 is connected to the toggle switch SW0_DB on the DE2-115 daughter board.
- In the same manner assign pin B to SW1_DB which is **PIN_AC21** on the FPGA, and assign the output pin C to the green LEDG1_DB which is **PIN_AG25** on the FPGA.
- Close the Pin Planner and **compile** the circuit again.

Programming the FPGA

- Open the Programmer – **Tools>Programmer.**
- Click the ***Hardware Setup…*** button.
- Under ***Currently selected hardware****:* select **USB-Blaster [USB-0]** and click *Close*.
- If your window looks like the one below click on the ***Start*** button.



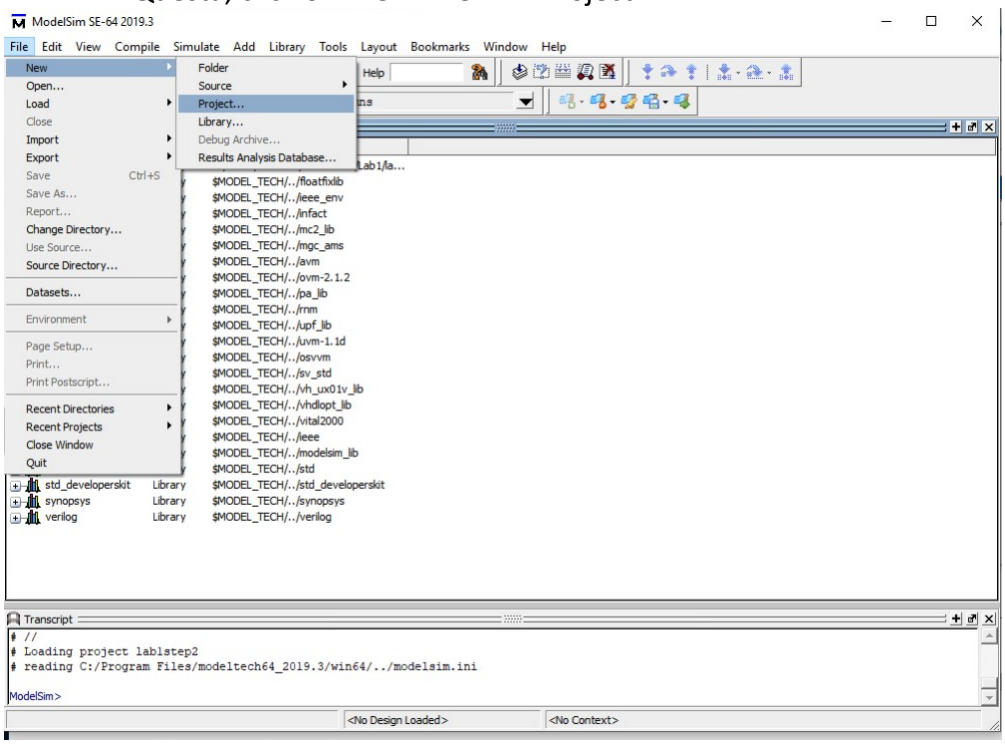
When the green LOAD LED (adjacent to the blue POWER LED) extinguishes, the FPGA will be programmed with your digital circuit. You may now test the behavior of your circuit. The Answer Sheet has a Truth Table for this circuit. Toggle the switches (inputs) and observe the LED (output). Record the results for the circuit's output on the right column of the Truth Table. When you are done, review your results with the TA, and have the TA sign their initials on your sheet. Finally, close the lab1step1 Quartus project.

4.0 Model Simulation in Questa

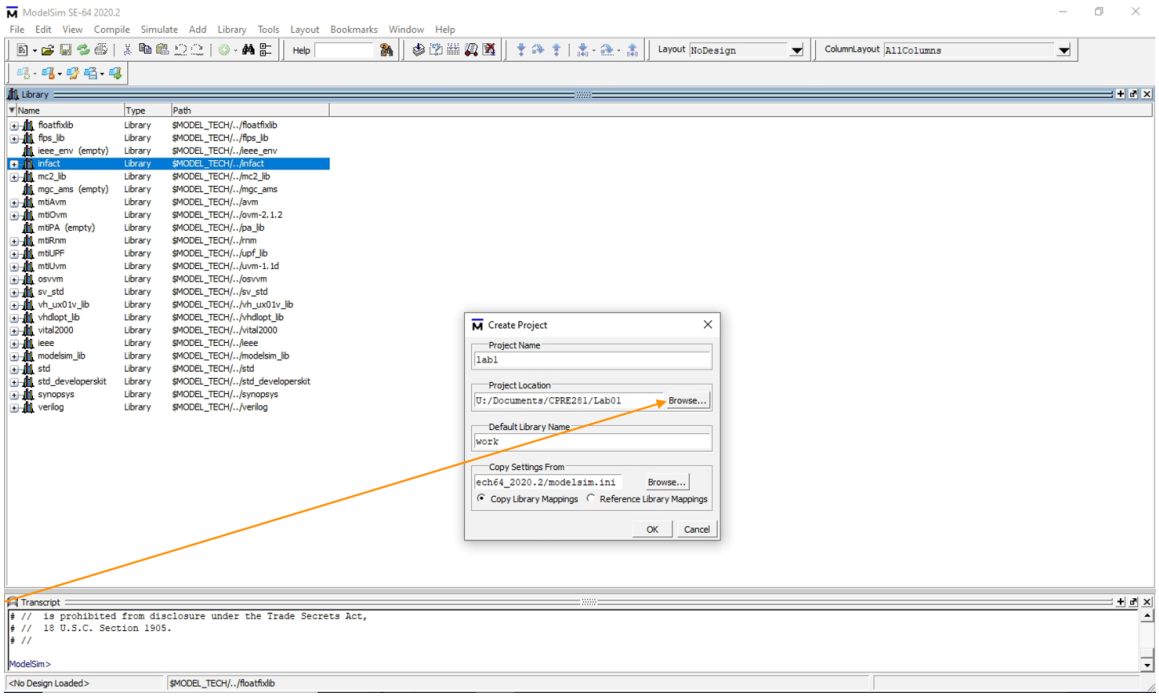
ModelSim software such as Questa ModelSim allows us to simulate digital circuits and tasks such as those normally performed on the Altera FPGA board. In addition, this software will be valuable when performing timing analysis in the future. You will use Questa to simulate the circuit done in part 3.0 and observe the output.

Creating a project in Questa

- Open Questa by searching for "Questa" in the Windows search box or by finding "Questa Sim" in the applications menu.
- Close the Important Information window, if applicable.
- In Questa, click on File → New → Project…



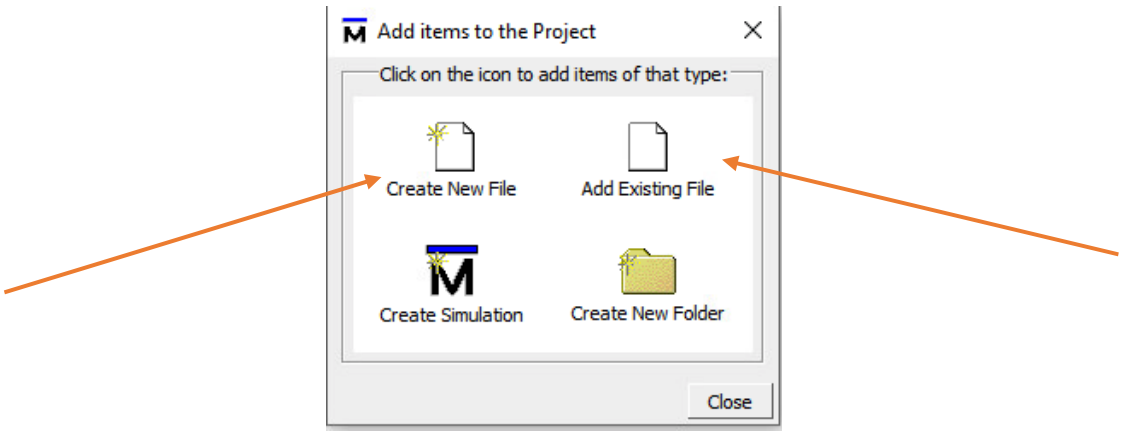
- Name your project "lab1step1"
- Set the project location to the location of the lab1step1.v file. This should be, for example, the lab1step1 folder.



- This lab1step1.v is a Verilog file; the details of Verilog will be discussed later in the semester, but for now, you only need to know that lab1step1.v is a replication of the circuit you just observed in Quartus.

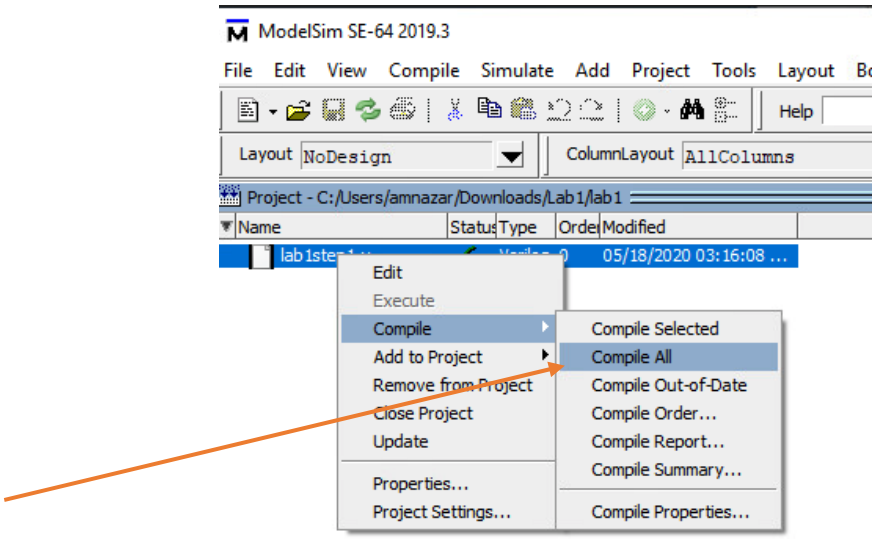
Adding a Verilog file to Questa

- From the "Add Items to the Project" window, select **Add Existing File**. If this window is not shown, then you can add files with File -> Open.



- Here, you should browse to lab1step1.v and click OK to add this Verilog file to the project.
- You should see lab1step1.v added to the project items. Close the Add Items to the Project window, if applicable.

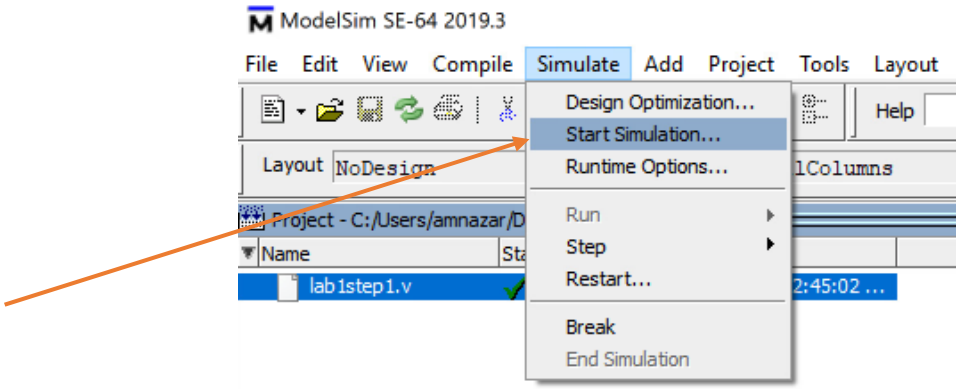
- Compile the newly added Verilog file by right-clicking it and selecting Compile → Compile All.



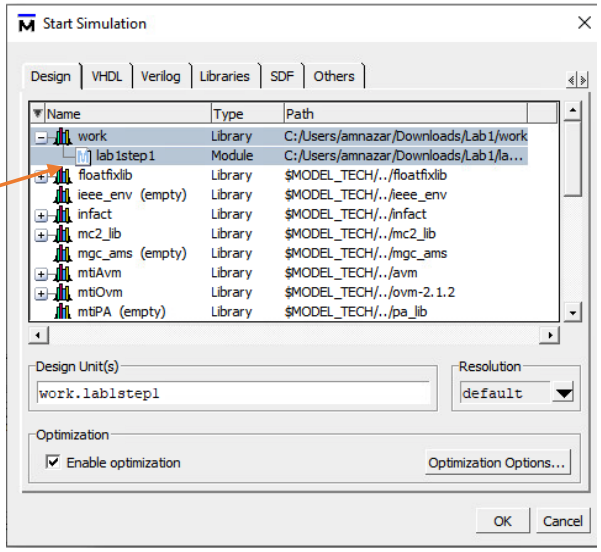
- On successful compilation, the blue question mark next to lab1step1.v will turn into a dark green check mark.

Simulating the Verilog file

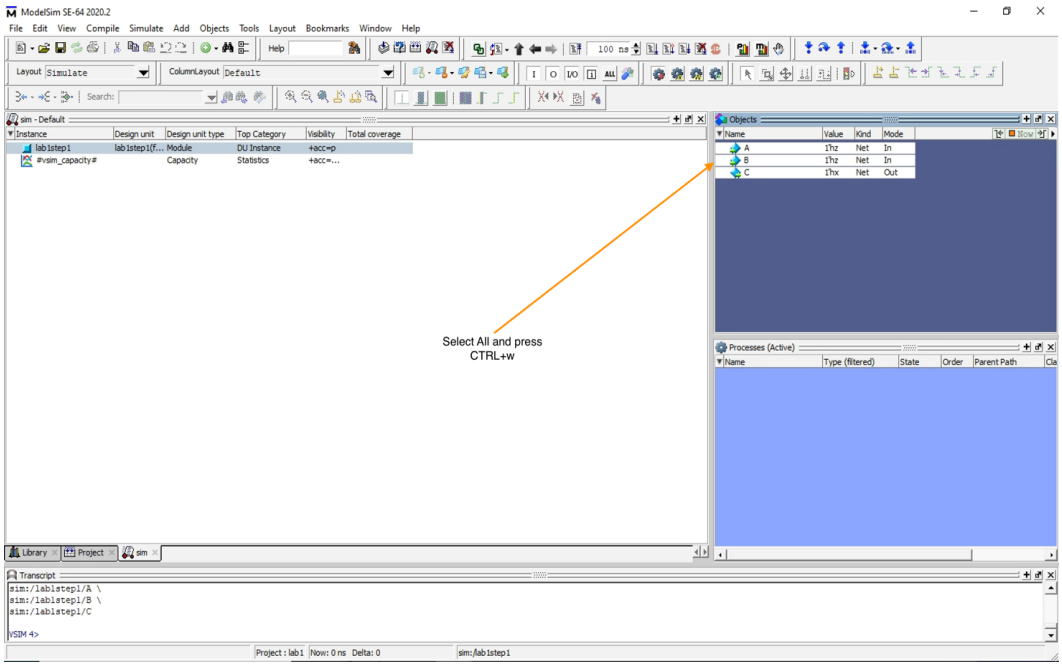
- After compiling lab1step1.v, you can begin simulation. From the main menu, select Simulate → Start Simulation as shown below.



- You will see a screen popup with many tabs. Ensure that the **Design** tab is selected.
- Locate the "work" library and expand it by clicking the [+]. This will reveal a lab1step1 module representing the lab1step1.v file.

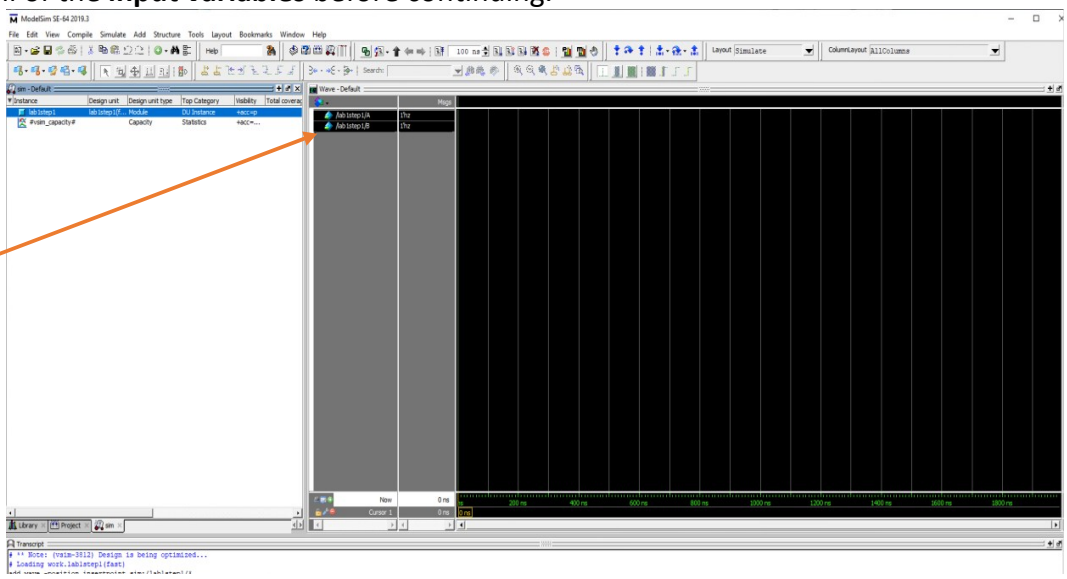


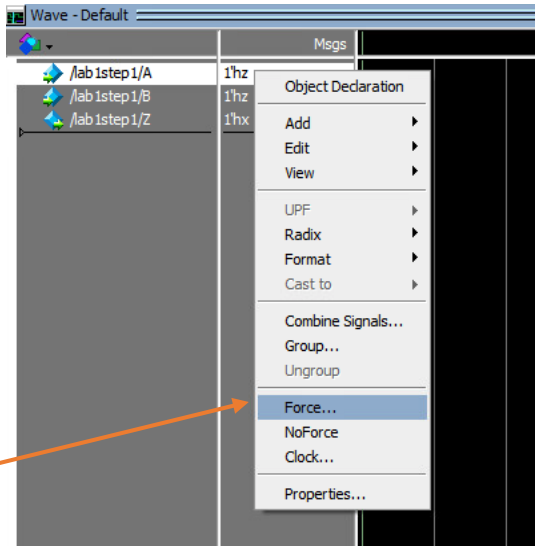
- Click on the lab1step1 module and click OK to begin simulation.
- After about 10 seconds, you will be taken to the **Sim** simulation environment. Here, a few subwindows may open, but if none open here, that is acceptable.
- If the Objects subwindow is not visible, select View → Objects to open it.
- In the Objects subwindow, you will see the inputs and output from the lab1step1.v file. Select all of these inputs and outputs by holding down Control or Shift and clicking them with the mouse.
- Once all the objects are selected, press **Ctrl-W** to add waveforms to these pins. This will also open the Wave subwindow, which can also be opened with View → Wave.



Edge-Case Testing

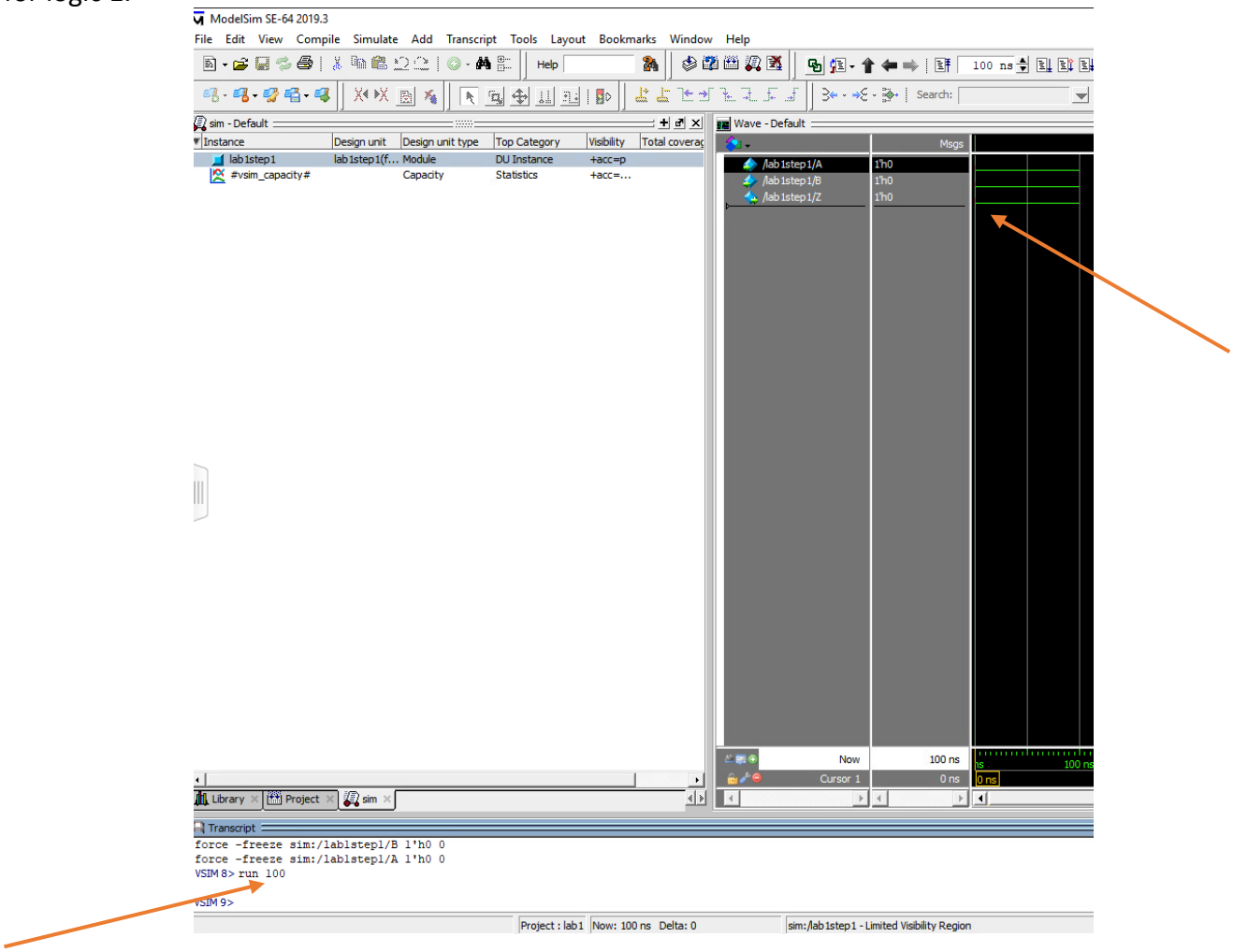
Now, it is time to test the circuit. Here, we will take the input variables and force them to desired values. It is important that you force values of the **input variables** and **not the output variables**. To force the value of an input, right-click the input variable and select **Force**, as shown below. This will allow the input value to be set to 0 (with the syntax **1'h0**) or 1 (with the syntax **1'h1**). The default value is **1'hz**, which represents an uninitialized or unconnected connection and can cause erroneous outputs. Make sure to force all of the **input variables** before continuing.





To observe the output based on the input, find the Command window at the bottom within the Questa simulation environment. Using commands in the Command

window, we can quickly tell Questa ModelSim to complete tasks instead of looking for them in the dropdown menus. When all inputs are forced to the desired value, type **run 100.** This will cause the simulation to simulate the output for 100 nanoseconds on the timing diagram. Observe that the waveform is down for logic 0 and the waveform is up for logic 1.



Simulate the output for the other input combinations of A and B by again selecting the inputs and right-clicking to select **Force**. Generate the output waveform by typing **run 100** in the command window. Once the output combinations are generated from all of the input combinations, discuss the results with your TA and have the TA mark their initials next to your answers.

5.0 Multi-level Circuits

We will now look at a more complex circuit. Open the files and follow the instructions. Read the previously outlined steps for opening a file if you are not sure how.

Circuit 1

- **Open** the *lab1step2.qpf* file. Even though this circuit is larger, its behavior can still be shown on a Truth Table. The circuit has multiple logic gates, a single output, and three inputs. You do not have to add anything to this circuit. Notice that pin W is assigned to SW2_DB which is **PIN_AB21** on the FPGA.
- Use the DE2-115 board to toggle the inputs on the gates to determine how the input combinations affect the output.
- Compile the design and then program the FPGA with the new circuit. Record the circuit's behavior on your answer sheet.

You can discuss the results with your TA. When you are done, have the TA mark his/her initials next to your answers.

Circuit 2

- **Open** the *lab1step3.v* in Questa. Notice that the Truth Table on the answer sheet for this circuit is blank.
- You need to fill in all possible input and output combinations in the Truth Table.
- Use the Questa waveform simulation to simulate all eight combinations of the input variables.
- Record each input combination and resulting output.

You can discuss the results with your TA. When you are done, have the TA mark his/her initials next to your answers.

6.0 Finished

You are done with this lab. Ensure that all lab files are closed. Exit Quartus Prime or Questa ModelSim, log off the computer, power down the DE2-115 board, and hand in your answer sheet. **Don't forget to write down your name, student ID and your lab section number**.