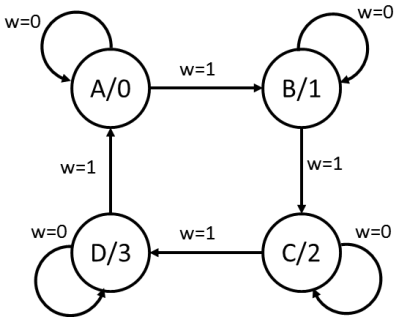
CprE 281 HW10

ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

Basic Design Steps, State-Assignment Problems, Moore & Mealy Machines

Assigned Date: Eleventh Week
Finish by Nov. 12, 2022

P1. (20 points) Consider a FSM with the following state diagram:



a) (5 points) Complete the following state table based on the state diagram:

Present State	Next State		Output
	W=0	W=1	
A	A	B	0
B			
C			
D			

b) (5 points) Encode each state and outputs in (a) with binary numbers to build the following state-assigned table:

Present State Y_1Y_0	Next State		Output Z_1Z_0
	W=0 Y_1Y_0	W=1 Y_1Y_0	

a. (5 points) Derive the minimal logic expressions for Y1, Y0, z1, and z0.

b. (5 points) Draw the complete circuit diagram using D flip-flops and any additional logic gates that are required.

c. (5 points) What does this FSM do? What happens when w=0 and w=1?

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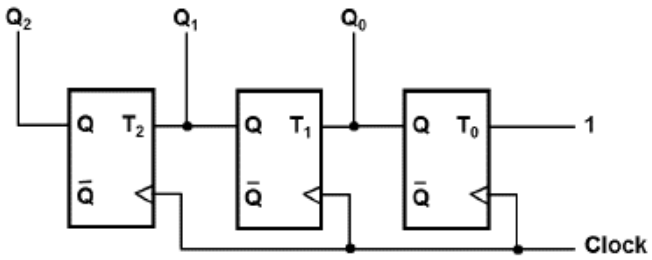
P2 (20 points): Draw the state diagram for a Moore FSM that has a 1-bit input P and a 1-bit output Q. P will be either 1 or 0 on any particular clock cycle. Q=0 if P has been 1 for an even number of clock cycles; Q=1 if P has been 1 for an odd number of clock cycles.

a. Draw the state diagram for this Moore FSM.
b. Draw the state table for this FSM.
c. Draw a state assigned table for this FSM. The state should be the same as the output: Q.
d. Draw the truth table for this FSM's next-state variable.
e. Derive the expression for the next state variable and the output Q.
f. Draw the circuit for this FSM. If done properly, the circuit you create will implement a component that you have seen before. What component have you implemented?

P3. (10 points) The circuit below looks like a counter. What is the sequence that this circuit counts-in? (Assuming Q is initially 000)



P4. (20 points) Design a 4-bit register with both shift and parallel load features. The inputs of the register include a 2-bit control code X Y, a 4-bit input value I3 I2 I1 I0, and a clock signal. The outputs of the register are the 4 bits Q3 Q2 Q1 Q0 corresponding to the value stored in the register. You are allowed to use any number of D flip-flops, muxes of any size, decoders and encoders of any sizes, AND gates, OR gates, and NOT gates. (Notice that you do not need all of them.) The operations of the register are defined below:

X Y	Operation
0 0	Load new date (i.e., new Q3=I3, new Q2=I2, new Q1=I1, new Q0=I0) changed)
0 1	Shift left (i.e., new Q3=Q2, new Q2=Q1, new Q1=Q0, new Q0=I0)
1 0	Shift right (i.e., new Q3=I3, new Q2=Q3, new Q1=Q2, new Q0=Q1)
1 1	Hold the current value stored (i.e., Q3 Q2 Q1 Q0 are not changed)

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P5. (15 points) Consider a register file containing *eight* 16-bit registers, two input ports and three output ports. To implement the register file, we need **W** number of **X**-to-**Y** decoders, and **Z** number of 16-bit **Q**-to-1 multiplexers. Specify the values for **W, X, Y, Z** and **Q.**

P6. (15 points) A state machine has one input X in addition to the clock input and one output Q. The value of Q is 1 if the total number of 1's in the sequence of input P is either a multiple of 2 or 3. Draw the state transition diagram for the state machine using as few states as possible. Is this a Moore or Mealy machine? Why?