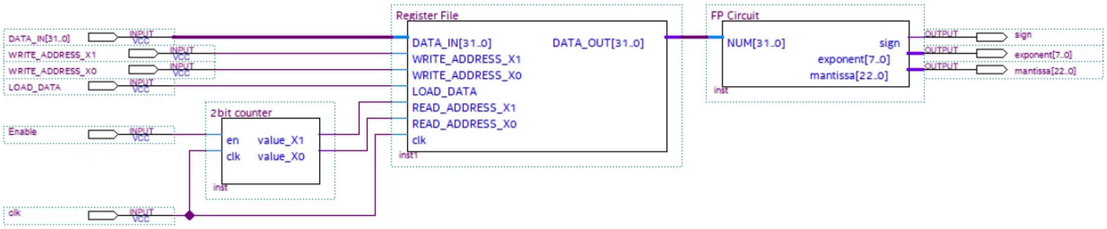
Cpr E 281 HW09
ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

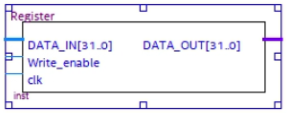
Midterm 2 Practice
Due Date: Oct. 31, 2022

P1 (30 points): Floating Point Register File.
Consider the circuit below. This circuits iterates through a list of four floating point numbers stored in a register file and finds the sign, exponent, and mantissa portion of each number.



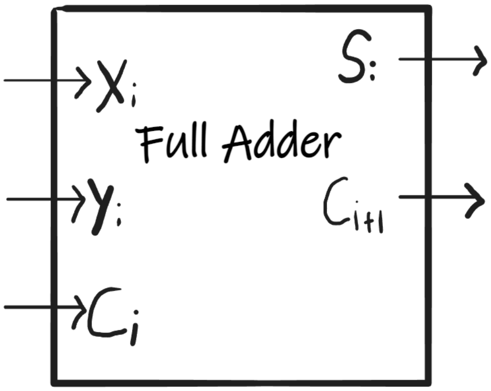
A) (10 points) The following four floating point numbers are currently stored in the register file. For each number find the values for **sign**, **exponent**, and **mantissa**. (Ex: 3.0, sign = 0, exponent = 10000000_2 , mantissa = $10000000000000000000000_2$.)
   a. 23
   b. -127
   c. -53
   d. 1.6

B) (10 points) Use any number of 32-bit registers, 2-to-4 decoders, 32-bit 4-to-1 multiplexers, and any necessary gates to construct a register file that can store four floating point numbers. Use the following design for your 32-bit registers.



C) (10 points) Implement a 2-bit counter to iterate through all four values stored in the register file.
   a. Use TFF to design the 2-bit counter
   b. Use DFF to implement the 2-bit counter

P2 (15 points): Consider the Full Adder:



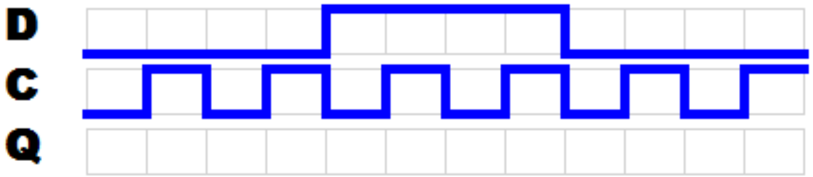
a. Draw the truth table for this Full Adder circuit

b. Write the Canonical **SOP** expression for this Full Adder

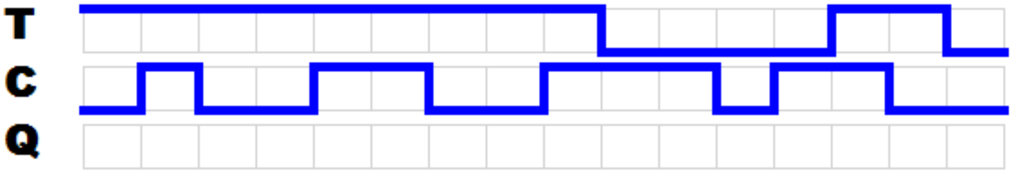
c. Implement the Full adder with a **minimal** number of 4-to-1 multiplexors and **No Other Logic Gates**. Assume that the input signals are available **Only** in their non-inverted form, along with constants 0 and 1. Clearly label all inputs, outputs, and pins of your circuit

P3 (20 points): Complete the following timing diagrams for the specified components. The clock is C. You may assume that Q is initially at 0 unless specified otherwise.

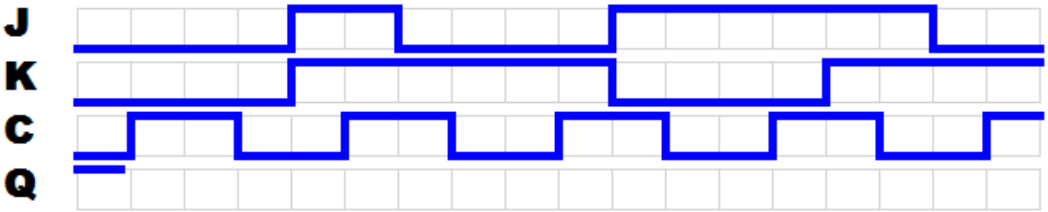
A: A positive-edge-triggered D Flip-Flop (DFF).



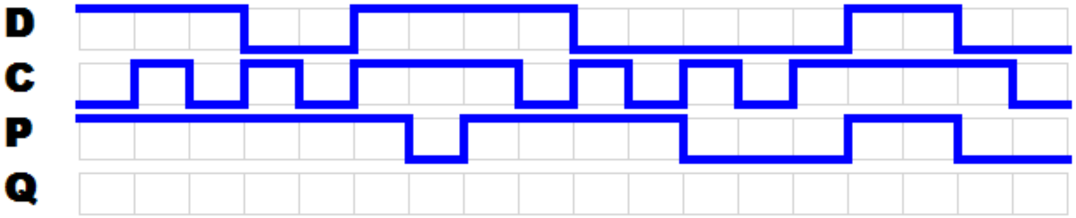
B: A negative-edge-triggered T Flip-Flop (TFF).



C: A positive-edge-triggered JK Flip-Flop (JKFF).



D: A negative-edge-triggered DFF with active-low Preset P (preset occurs when P=0).



P4 (15 points): Number Conversions:

a. Convert -$\mathbf{163}_{10}$ to binary using sign and magnitude notation

b. Convert the following 32-bit float number (in IEEE 754 format) to decimal: **1100 0001 1000 1000 0000 0000 0000 0000**

c. Write down the 32-bit floating point representation (in IEEE 754 format) for $\mathbf{15.0}_{10}$

d. Convert $\mathbf{-53}_{10}$ to and **8-bit** binary number in 2's complement representation

e. Convert $\mathbf{-42}_{10}$ to and **8-bit** binary number in 1's complement representation

P5 (12 points): A given register file can support storing values in its 32 registers. Each register is designed to hold numbers ranging from -25 to +25 (in 2's complement) with no additional bits beyond those necessary to hold numbers in this range. Answer the following questions:

A: What is the **width** of the LD_DATA bus? (Note that **width** is the number of bits)

B: What is the width of each register?

C: What is the width of the RA bus?

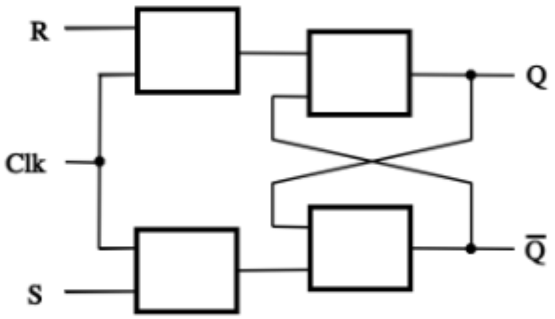
D: What is the width of the WA bus?

E: How many DFFs exist in this register file?

F: What type of decoder is used in this register file?

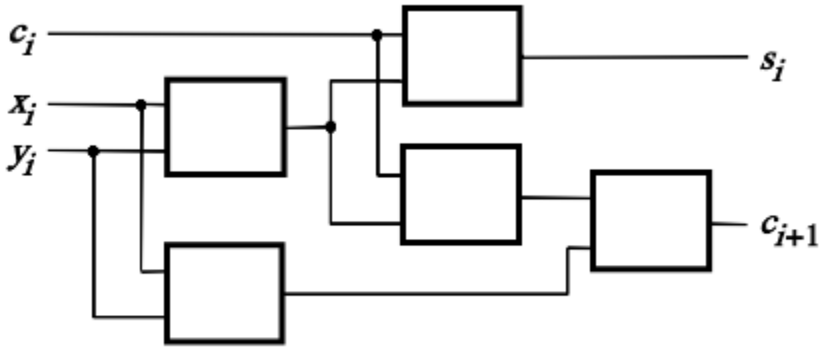
P6 (8 points): Given the inputs, outputs, and wires of a familiar circuit, fill in the names of the logic gates inside the square blocks. Also, write the **name** of each circuit.

a)



Circuit name:

b)



Circuit name: