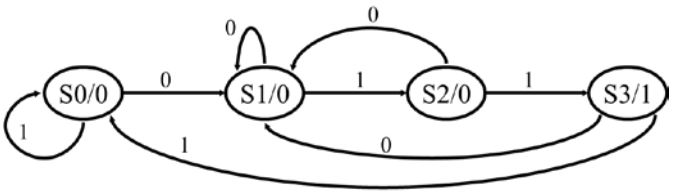
Recitation #11 Solutions

1.



2. State-assigned table for next state:

q2	q1	q0	Input I	Q2	Q1	Q0
0	0	0	0	0	0	0
0	0	0	1	0	0	1
0	0	1	0	0	1	0
0	0	1	1	0	1	1
0	1	0	0	1	0	0
0	1	0	1	1	0	1
0	1	1	0	1	1	0
0	1	1	1	1	1	1
1	0	0	0	0	0	0
1	0	0	1	0	0	1
1	0	1	0	0	1	0
1	0	1	1	0	1	1
1	1	0	0	1	0	0
1	1	0	1	1	0	1
1	1	1	0	1	1	0
1	1	1	1	1	1	1

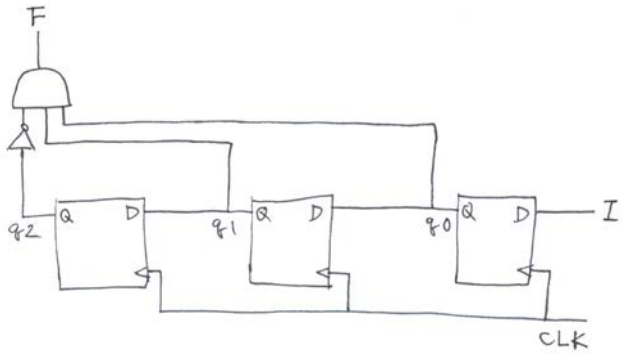
Q2 = q1
Q1 = q0
Q0 = I

State-assigned table for output:

q2	q1	q0	Output F
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

F = q2'.q1.q0

Circuit diagram:

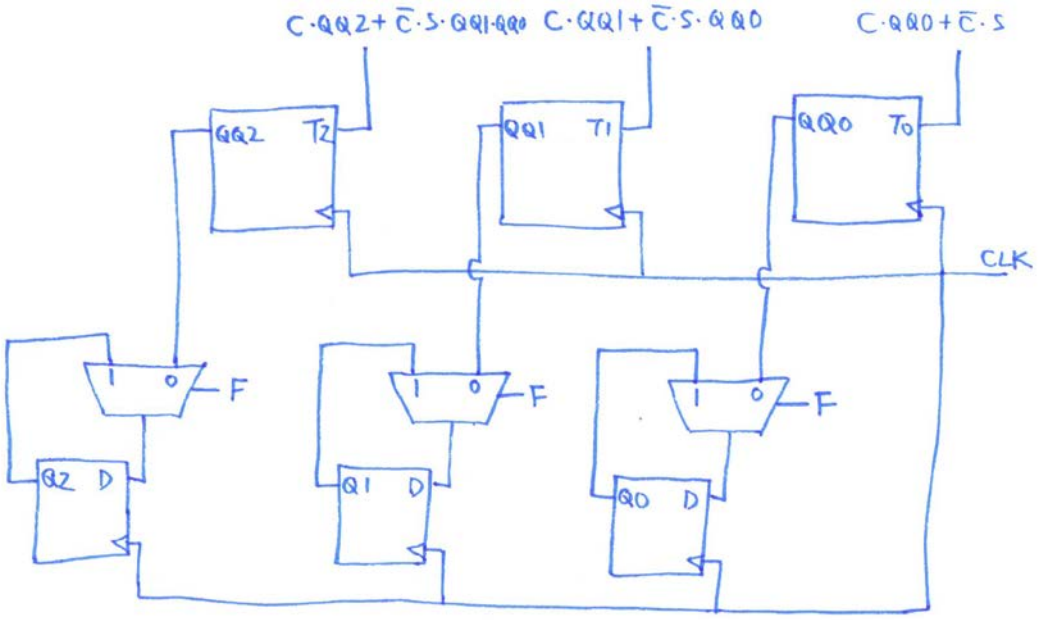


3. Let S be the Start/Stop signal, C be the Clear signal, and F be the Freeze signal.
We first design a 3-bit synchronous up-counter with Start/Stop and Clear using T flip-flops.
Assume the current count value is QQ2 QQ1 QQ0.

S	C	Behavior	T2	T1	T0
0	0	Keep count value	0	0	0
0	1	Clear	QQ2	QQ1	QQ0
1	0	Increment count value	QQ1.QQ0	QQ0	1
1	1	Clear	QQ2	QQ1	QQ0

T2 = C.QQ2 + C'.S.QQ1.QQ0
T1 = C.QQ1 + C'.S.QQ0
T0 = C.QQ0 + C'.S

Then we add the Freeze feature using some D flip-flops and multiplexers.
The value displayed is Q2 Q1 Q0.



4. Solution not provided.