DE2-115 Board I/O Pin Assignments: Switches, LEDs, and 7-Segment Displays

Table 1: Daughter Board Pin assignments

Signal Name	FPGA Pin No.	Description
SW3_DB	PIN_AB22	Rocker Switch[3]
SW2_DB	PIN_AB21	Rocker Switch[2]
SW1_DB	PIN_AC21	Rocker Switch[1]
SW0_DB	PIN_AD21	Rocker Switch[0]
KEY1_DB	PIN_AC19	Push-button[1]
KEY0_DB	PIN_AD19	Push-button[0]
LEDR3_DB	PIN_AF24	LED Red[3]
LEDR2_DB	PIN_AF25	LED Red[2]
LEDR1_DB	PIN_AE22	LED Red[1]
LEDR0_DB	PIN_AF22	LED Red[0]
LEDG1_DB	PIN_AG25	LED Green[1]
LEDG0_DB	PIN_AH25	LED Green[0]

Table 2: Pin assignments for slide switches

Signal Name	*FPGA Pin No.*	*Description*	*I/O Standard*
SW[0]	PIN_AB28	Slide Switch[0]	Depending on JP7
SW[1]	PIN_AC28	Slide Switch[1]	Depending on JP7
SW[2]	PIN_AC27	Slide Switch[2]	Depending on JP7
SW[3]	PIN_AD27	Slide Switch[3]	Depending on JP7
SW[4]	PIN_AB27	Slide Switch[4]	Depending on JP7
SW[5]	PIN_AC26	Slide Switch[5]	Depending on JP7
SW[6]	PIN_AD26	Slide Switch[6]	Depending on JP7
SW[7]	PIN_AB26	Slide Switch[7]	Depending on JP7
SW[8]	PIN_AC25	Slide Switch[8]	Depending on JP7
SW[9]	PIN_AB25	Slide Switch[9]	Depending on JP7
SW[10]	PIN_AC24	Slide Switch[10]	Depending on JP7
SW[11]	PIN_AB24	Slide Switch[11]	Depending on JP7
SW[12]	PIN_AB23	Slide Switch[12]	Depending on JP7
SW[13]	PIN_AA24	Slide Switch[13]	Depending on JP7
SW[14]	PIN_AA23	Slide Switch[14]	Depending on JP7
SW[15]	PIN_AA22	Slide Switch[15]	Depending on JP7
SW[16]	PIN_Y24	Slide Switch[16]	Depending on JP7
SW[17]	PIN_Y23	Slide Switch[17]	Depending on JP7

Table 3: Pin assignments for pushbutton (debounced) switches

Signal Name	*FPGA Pin No.*	*Description*	*I/O Standard*
KEY[0]	PIN_M23	Push-button[0]	Depending on JP7
KEY[1]	PIN_M21	Push-button[1]	Depending on JP7
KEY[2]	PIN_N21	Push-button[2]	Depending on JP7
KEY[3]	PIN_R24	Push-button[3]	Depending on JP7

Table 4: Pin assignments for LEDs

Signal Name	*FPGA Pin No.*	*Description*	*I/O Standard*
LEDR[0]	PIN_G19	LED Red[0]	2.5V
LEDR[1]	PIN_F19	LED Red[1]	2.5V
LEDR[2]	PIN_E19	LED Red[2]	2.5V
LEDR[3]	PIN_F21	LED Red[3]	2.5V
LEDR[4]	PIN_F18	LED Red[4]	2.5V
LEDR[5]	PIN_E18	LED Red[5]	2.5V
LEDR[6]	PIN_J19	LED Red[6]	2.5V
LEDR[7]	PIN_H19	LED Red[7]	2.5V
LEDR[8]	PIN_J17	LED Red[8]	2.5V
LEDR[9]	PIN_G17	LED Red[9]	2.5V
LEDR[10]	PIN_J15	LED Red[10]	2.5V
LEDR[11]	PIN_H16	LED Red[11]	2.5V
LEDR[12]	PIN_J16	LED Red[12]	2.5V
LEDR[13]	PIN_H17	LED Red[13]	2.5V
LEDR[14]	PIN_F15	LED Red[14]	2.5V
LEDR[15]	PIN_G15	LED Red[15]	2.5V
LEDR[16]	PIN_G16	LED Red[16]	2.5V
LEDR[17]	PIN_H15	LED Red[17]	2.5V
LEDG[0]	PIN_E21	LED Green[0]	2.5V
LEDG[1]	PIN_E22	LED Green[1]	2.5V
LEDG[2]	PIN_E25	LED Green[2]	2.5V
LEDG[3]	PIN_E24	LED Green[3]	2.5V
LEDG[4]	PIN_H21	LED Green[4]	2.5V
LEDG[5]	PIN_G20	LED Green[5]	2.5V
LEDG[6]	PIN_G22	LED Green[6]	2.5V
LEDG[7]	PIN_G21	LED Green[7]	2.5V
LEDG[8]	PIN_F17	LED Green[8]	2.5V

Using the 7-segment Displays

The DE2 Board has eight 7-segment displays. These displays are arranged as two pairs and a group of four, with the intent of displaying numbers of various sizes. Applying a low logic level to a segment causes it to light up, and applying a high logic level turns it off. Each segment in a display is identified by an index from 0 to 6, with the positions given in Figure 1. Note that the dot in each display is unconnected and cannot be used. Table 4 shows the assignments of FPGA pins to the 7-segment displays.

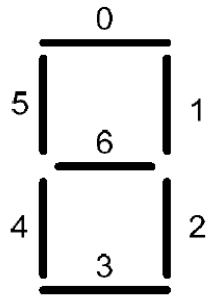

Figure 1: Position and index of each segment in a 7-segment display.

Table 5: Pin assignments for 7-segment displays

Signal Name	FPGA Pin No.	Description	I/O Standard
HEX0[0]	PIN_G18	Seven Segment Digit 0[0]	2.5V
HEX0[1]	PIN_F22	Seven Segment Digit 0[1]	2.5V
HEX0[2]	PIN_E17	Seven Segment Digit 0[2]	2.5V
HEX0[3]	PIN_L26	Seven Segment Digit 0[3]	Depending on JP7
HEX0[4]	PIN_L25	Seven Segment Digit 0[4]	Depending on JP7
HEX0[5]	PIN_J22	Seven Segment Digit 0[5]	Depending on JP7
HEX0[6]	PIN_H22	Seven Segment Digit 0[6]	Depending on JP7
HEX1[0]	PIN_M24	Seven Segment Digit 1[0]	Depending on JP7
HEX1[1]	PIN_Y22	Seven Segment Digit 1[1]	Depending on JP7
HEX1[2]	PIN_W21	Seven Segment Digit 1[2]	Depending on JP7
HEX1[3]	PIN_W22	Seven Segment Digit 1[3]	Depending on JP7
HEX1[4]	PIN_W25	Seven Segment Digit 1[4]	Depending on JP7
HEX1[5]	PIN_U23	Seven Segment Digit 1[5]	Depending on JP7
HEX1[6]	PIN_U24	Seven Segment Digit 1[6]	Depending on JP7
HEX2[0]	PIN_AA25	Seven Segment Digit 2[0]	Depending on JP7
HEX2[1]	PIN_AA26	Seven Segment Digit 2[1]	Depending on JP7
HEX2[2]	PIN_Y25	Seven Segment Digit 2[2]	Depending on JP7
HEX2[3]	PIN_W26	Seven Segment Digit 2[3]	Depending on JP7
HEX2[4]	PIN_Y26	Seven Segment Digit 2[4]	Depending on JP7
HEX2[5]	PIN_W27	Seven Segment Digit 2[5]	Depending on JP7
HEX2[6]	PIN_W28	Seven Segment Digit 2[6]	Depending on JP7

Signal Name	FPGA Pin No.	Description	I/O Standard
HEX3[0]	PIN_V21	Seven Segment Digit 3[0]	Depending on JP7
HEX3[1]	PIN_U21	Seven Segment Digit 3[1]	Depending on JP7
HEX3[2]	PIN_AB20	Seven Segment Digit 3[2]	Depending on JP7
HEX3[3]	PIN_AA21	Seven Segment Digit 3[3]	Depending on JP7
HEX3[4]	PIN_AD24	Seven Segment Digit 3[4]	Depending on JP7
HEX3[5]	PIN_AF23	Seven Segment Digit 3[5]	Depending on JP7
HEX3[6]	PIN_Y19	Seven Segment Digit 3[6]	Depending on JP7
HEX4[0]	PIN_AB19	Seven Segment Digit 4[0]	Depending on JP7
HEX4[1]	PIN_AA19	Seven Segment Digit 4[1]	Depending on JP7
HEX4[2]	PIN_AG21	Seven Segment Digit 4[2]	Depending on JP7
HEX4[3]	PIN_AH21	Seven Segment Digit 4[3]	Depending on JP7
HEX4[4]	PIN_AE19	Seven Segment Digit 4[4]	Depending on JP7
HEX4[5]	PIN_AF19	Seven Segment Digit 4[5]	Depending on JP7
HEX4[6]	PIN_AE18	Seven Segment Digit 4[6]	Depending on JP7
HEX5[0]	PIN_AD18	Seven Segment Digit 5[0]	Depending on JP7
HEX5[1]	PIN_AC18	Seven Segment Digit 5[1]	Depending on JP7
HEX5[2]	PIN_AB18	Seven Segment Digit 5[2]	Depending on JP7
HEX5[3]	PIN_AH19	Seven Segment Digit 5[3]	Depending on JP7
HEX5[4]	PIN_AG19	Seven Segment Digit 5[4]	Depending on JP7
HEX5[5]	PIN_AF18	Seven Segment Digit 5[5]	Depending on JP7
HEX5[6]	PIN_AH18	Seven Segment Digit 5[6]	Depending on JP7
HEX6[0]	PIN_AA17	Seven Segment Digit 6[0]	Depending on JP7
HEX6[1]	PIN_AB16	Seven Segment Digit 6[1]	Depending on JP7
HEX6[2]	PIN_AA16	Seven Segment Digit 6[2]	Depending on JP7
HEX6[3]	PIN_AB17	Seven Segment Digit 6[3]	Depending on JP7
HEX6[4]	PIN_AB15	Seven Segment Digit 6[4]	Depending on JP7
HEX6[5]	PIN_AA15	Seven Segment Digit 6[5]	Depending on JP7
HEX6[6]	PIN_AC17	Seven Segment Digit 6[6]	Depending on JP7
HEX7[0]	PIN_AD17	Seven Segment Digit 7[0]	Depending on JP7
HEX7[1]	PIN_AE17	Seven Segment Digit 7[1]	Depending on JP7
HEX7[2]	PIN_AG17	Seven Segment Digit 7[2]	Depending on JP7
HEX7[3]	PIN_AH17	Seven Segment Digit 7[3]	Depending on JP7
HEX7[4]	PIN_AF17	Seven Segment Digit 7[4]	Depending on JP7
HEX7[5]	PIN_AG18	Seven Segment Digit 7[5]	Depending on JP7
HEX7[6]	PIN_AA14	Seven Segment Digit 7[6]	3.3V

Table 6: Pin assignments for clock inputs

Signal Name	*FPGA Pin No.*	*Description*	*I/O Standard*
CLOCK_50	PIN_Y2	50 MHz clock input	3.3V
CLOCK2_50	PIN_AG14	50 MHz clock input	3.3V
CLOCK3_50	PIN_AG15	50 MHz clock input	Depending on JP6
SMA_CLKOUT	PIN_AE23	External (SMA) clock output	Depending on JP6
SMA_CLKIN	PIN_AH14	External (SMA) clock input	3.3V