Cpr E 281 HW08

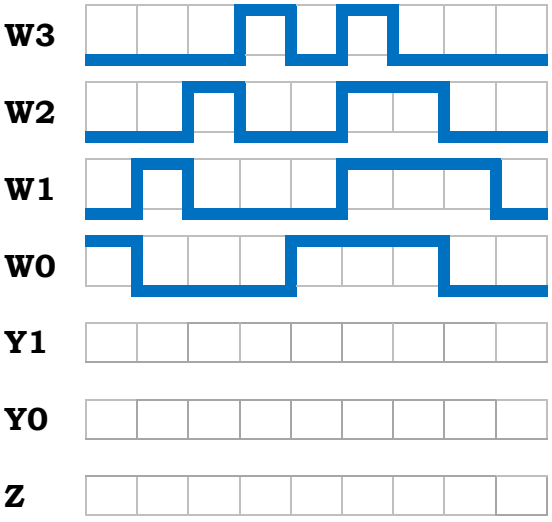
ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

Building Blocks

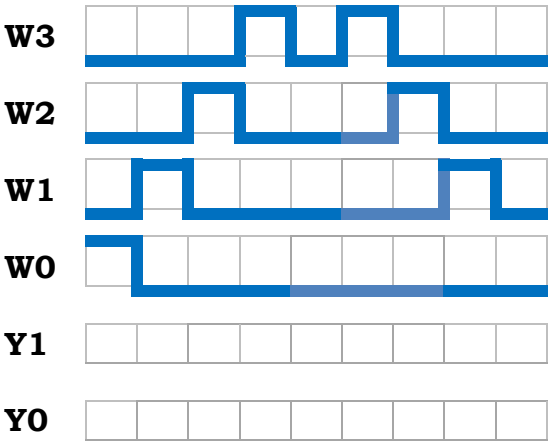
Due Date: Oct. 25, 2021

P1 (10 points): Fill in the timing diagrams below:

a) For a 4-to-2 priority encoder.



b) For a 4-to-2 binary encoder.



P2. (10 points) Consider the following truth table for the function $f(a, b, c, d)$.

a	***b***	***c***	***d***	***f***
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

a) Implement f using one 4-to-16 decoder and a minimal number of gates.

b) Implement f using two 2-to-4 decoders, one 4-to-1 multiplexer, and a minimal number of gates.

P3 (20 points): 8-to-1 multiplexer

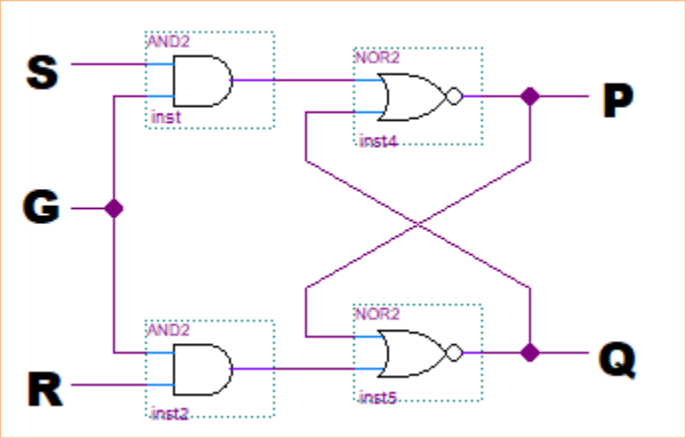
a) Write the Boolean function for an 8-to-1 multiplexor that has inputs $\{X_0, X_1, X_2, X_3, X_4, X_5, X_6, X_7\}$ and select lines {A, B, C}.

b) Implement the multiplexer using AND, OR, and NOT gates.

c) Implement the multiplexer using 2-to-1 multiplexers and a minimal number of additional gates

d) Implement the multiplexer using 4-to-1 multiplexers and a minimal number of additional gates

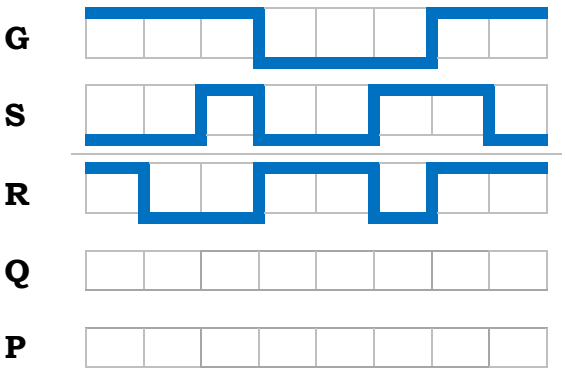
P4 (10 points): Consider the SR Latch shown below.



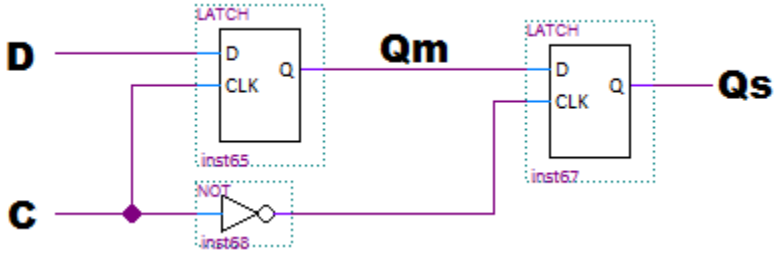
a) Complete the characteristic table.

G	S	R	Q	P
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

b) Complete the timing diagram shown below for outputs Q and P.

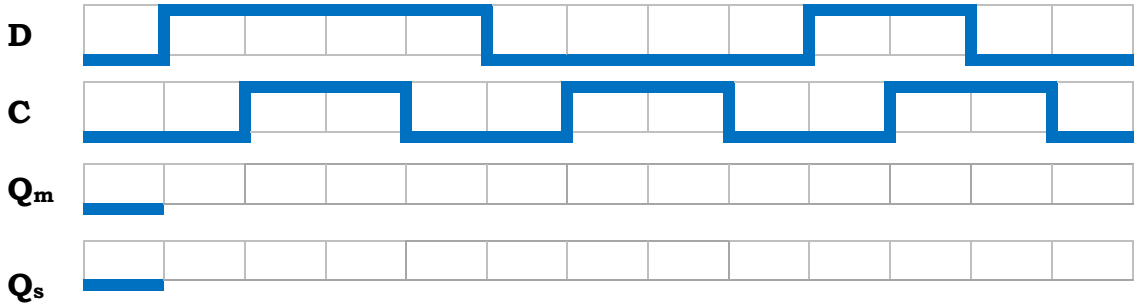


P5 (15 points): Answer the following questions based on the circuit shown below.



a) The latch that appears (twice) in the above circuit is a D Latch. Show the characteristic table for a D Latch.

b) Fill in the timing diagram for the values shown above.

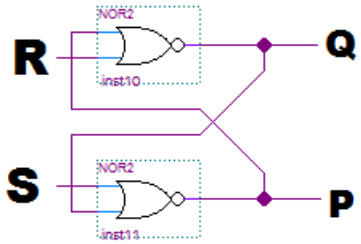


c) What is the name of this circuit? Is it a positive or negative edge circuit?

P6 (15 points): We want to create an LM-latch with the characteristic table shown below:

L	M	Q	P
0	0	0	1
0	1	No change	No change
1	0	No change	No change
1	1	1	0

a) Show the characteristic table for the SR Latch shown below.



S	R	Q	P
0	0		
0	1		
1	0		
1	1		

b) For each input combination to the LM-latch characteristic table shown above, write the values of S and R that will produce the output combinations. Then derive expressions for S and R in terms of L and M.

c) Draw the completed circuit for the LM-latch with the characteristic table based on the expressions derived in part B.

P7 (20 points): Answer the following questions about the Negative-Edge-Triggered Master-Slave DFF with PRESET_N and CLEAR_N connections, as shown in Figure 5.12 from the book. Suppose that D=1 and CLK=0. Answer the following questions about Q.

a) Ignoring PRESET_N and CLEAR_N (assume that they are not connected), what effect does pulsing the clock have on Q in this circuit?

b) What effect does pulsing PRESET_N have on this circuit?

c) What effect does pulsing CLEAR_N have on this circuit?

d) What will be the value of Q if PRESET_N=0 and CLEAR_N=1?

e) What will be the value of Q if PRESET_N=0 and CLEAR_N=0?

f) What will be the value of Q if the clock is pulsed while PRESET_N=0?

g) What will be the value of Q if the clock is pulsed while CLEAR_N=0?

h) What will be the value of Q if the clock is pulsed while CLEAR_N=1 and PRESET_N=1?