

# **CprE 281: Digital Logic**

**Instructor: Alexander Stoytchev**

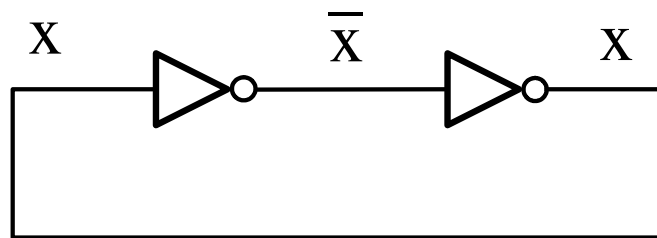
**<http://www.ece.iastate.edu/~alexs/classes/>**

# D Flip-Flops

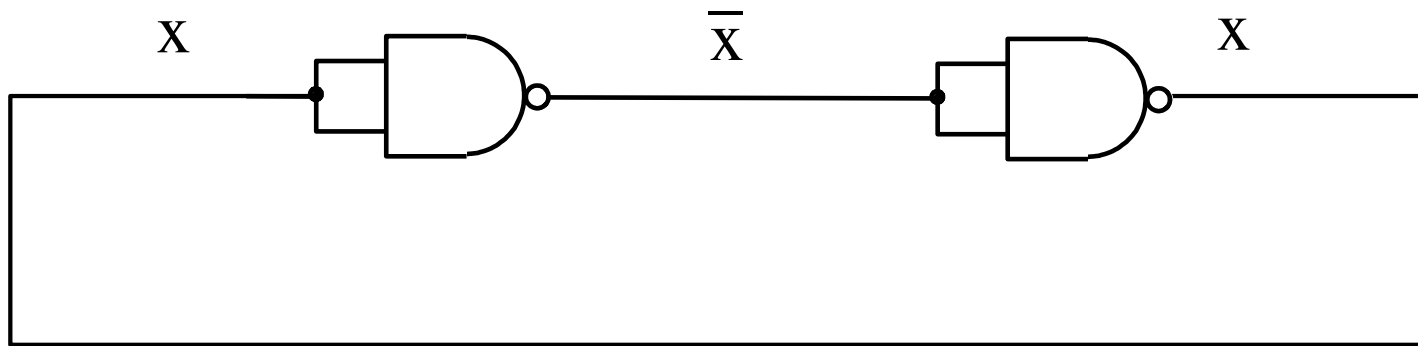
*CprE 281: Digital Logic  
Iowa State University, Ames, IA  
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# Quick Review

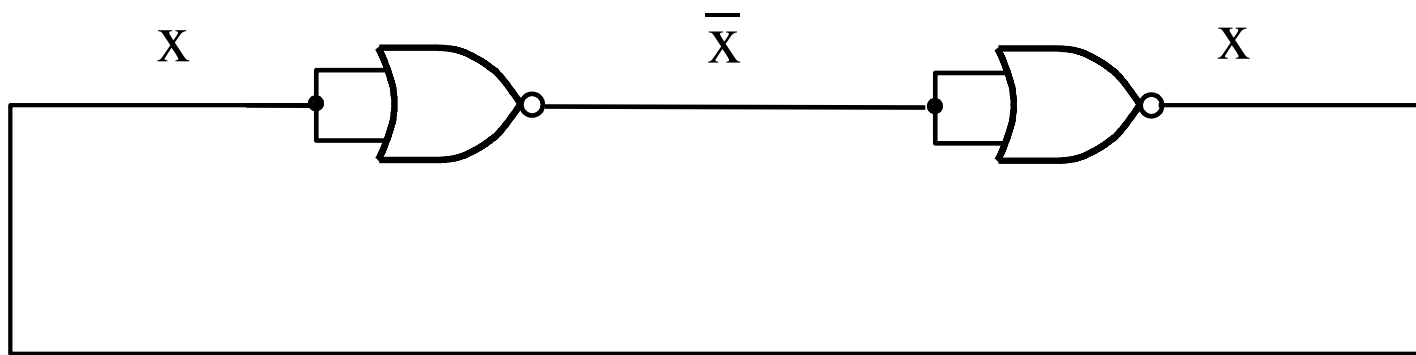
# A simple memory element with NOT Gates



# A simple memory element with NAND Gates

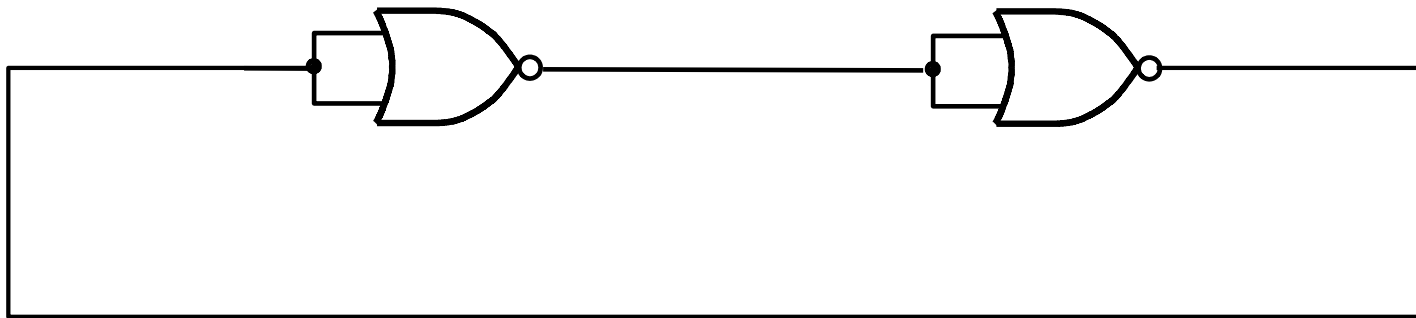


# A simple memory element with NOR Gates



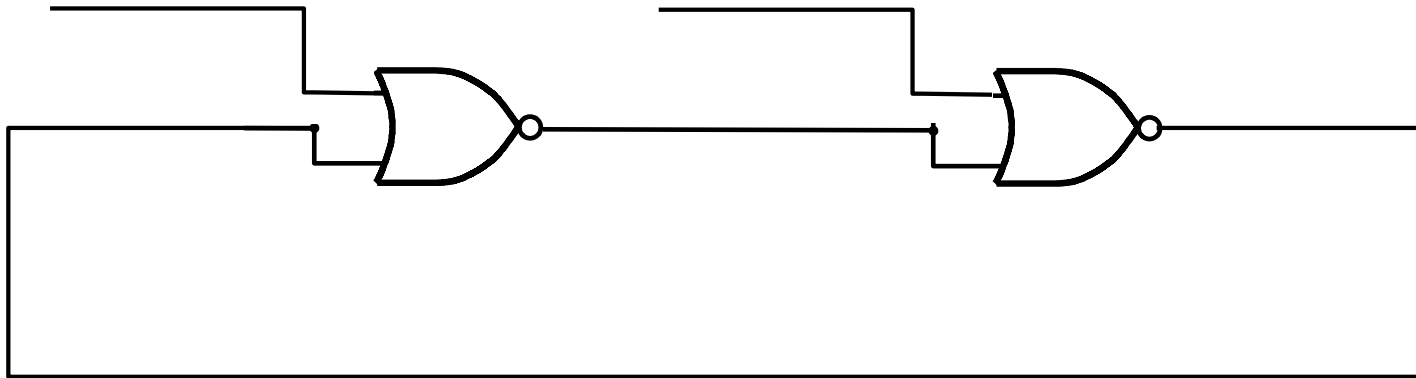
# Basic Latch

# A simple memory element with NOR Gates

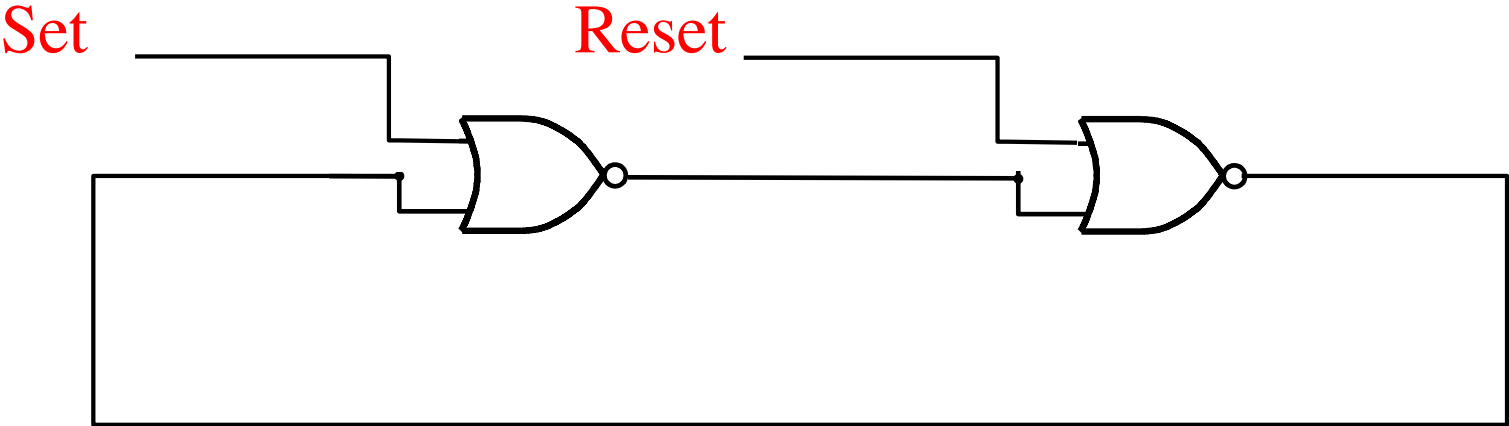




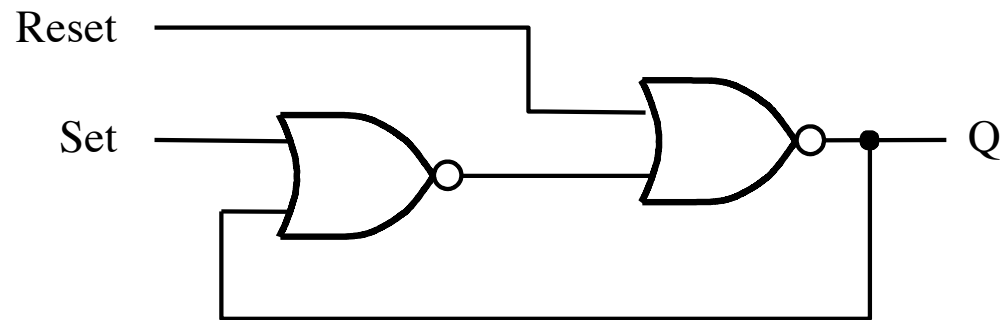
# A simple memory element with NOR Gates



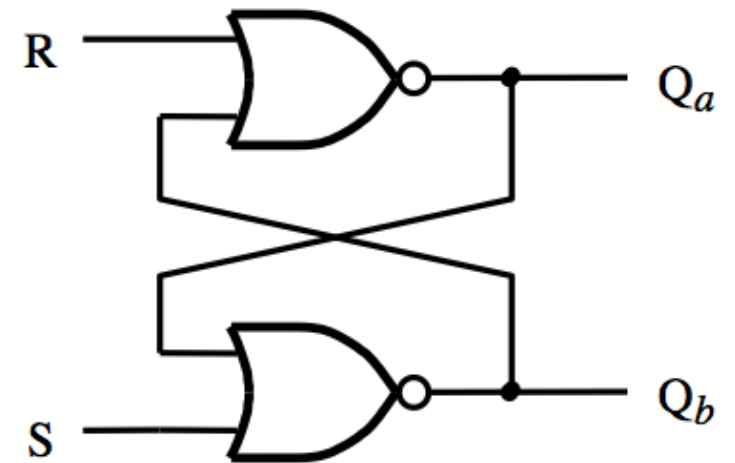
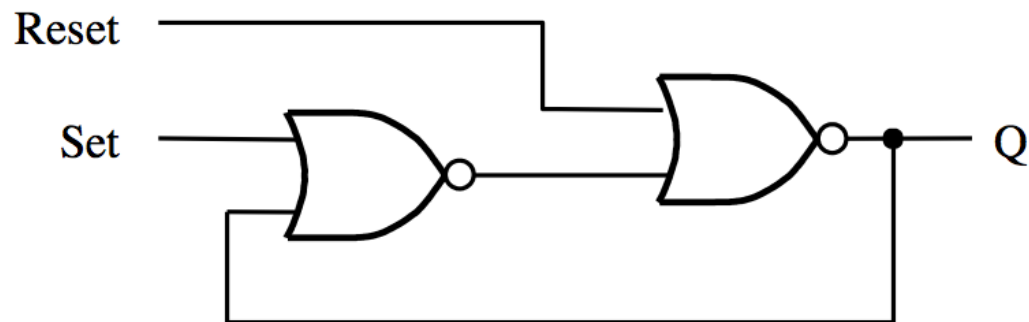
# A simple memory element with NOR Gates



# A memory element with NOR gates



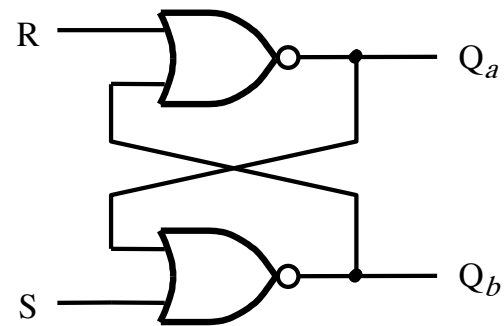
# Two Different Ways to Draw the Same Circuit



[ Figure 5.3 & 5.4 from the textbook ]

# Circuit and Characteristic Table for the Basic Latch

Note that  $Q_a$  and  $Q_b$  are inverses of each other!



(a) Circuit

S	R	$Q_a$	$Q_b$	
0	0	0/1	1/0	(no change)
0	1	0	1	
1	0	1	0	
1	1	0	0	

(b) Characteristic table

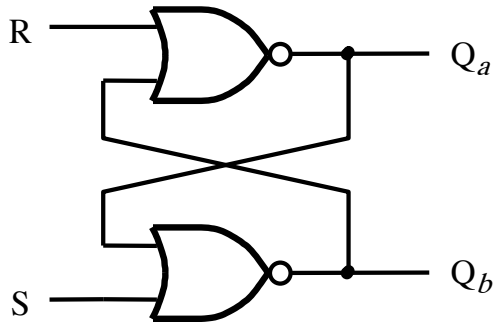
# Oscillations and Undesirable States

- **When  $S=1$  and  $R=1$  both outputs of the latch are equal to 0, i.e.,  $Q_a=0$  and  $Q_b=0$ .**
- **Thus, the two outputs are no longer complements of each other.**
- **This is undesirable as many of the circuits that we will build later with these latches rely on the assumption that the two outputs are always complements of each other.**
- **(This is obviously not the case for the basic latch, but we will patch it later to eliminate this problem).**

# Oscillations and Undesirable States

- An even bigger problem occurs when we transition from  $S=R=1$  to  $S=R=0$ .
- When  $S=R=1$  we have  $Q_a=Q_b=0$ . After the transition to  $S=R=0$ , however, we get  $Q_a=Q_b=1$ , which would immediately cause  $Q_a=Q_b=0$ , and so on.
- If the gate delays and the wire lengths are identical, then this oscillation will continue forever.
- In practice, the oscillation dies down and the output settles into either  $Q_a=1$  and  $Q_b=0$  or  $Q_a=0$  and  $Q_b=1$ .
- The problem is that **we can't predict** which one of these two it will settle into.

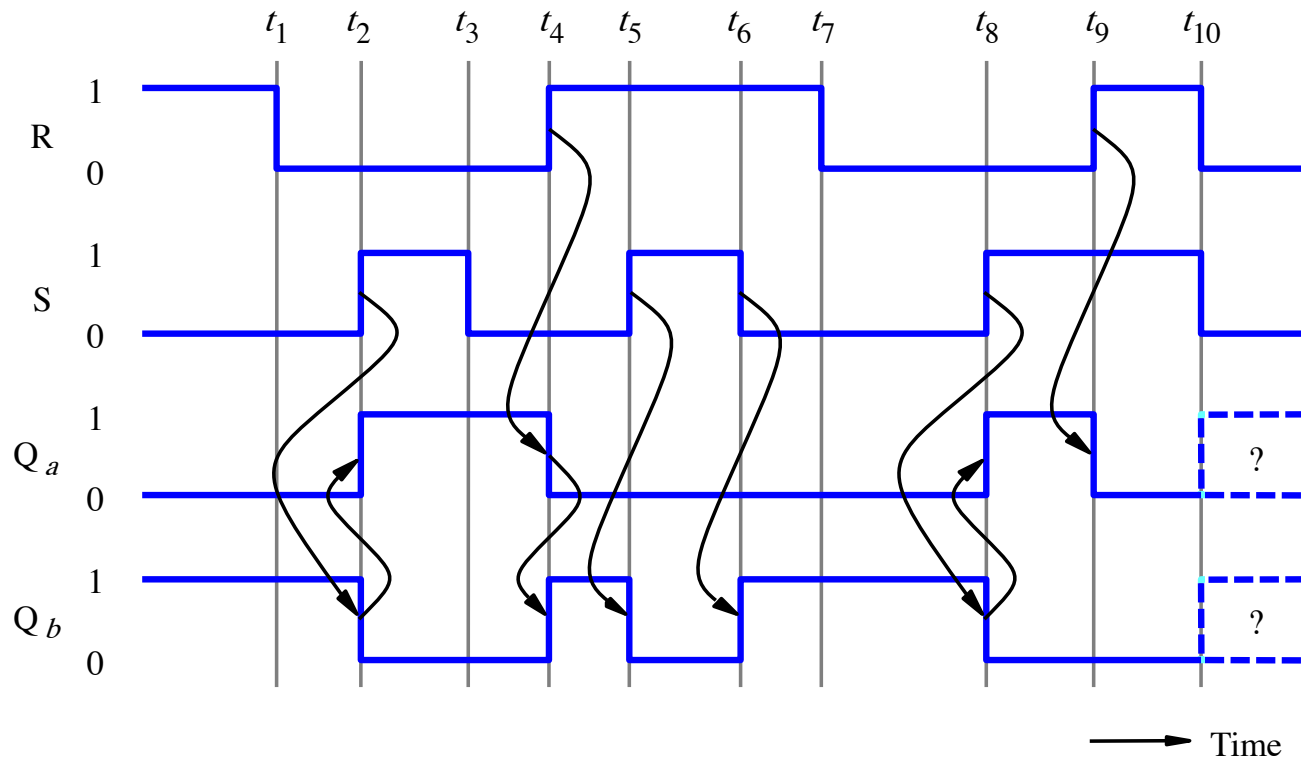
# Timing Diagram for the Basic Latch with NOR Gates



(a) Circuit

S	R	$Q_a$	$Q_b$
0	0	0/1	1/0 (no change)
0	1	0	1
1	0	1	0
1	1	0	0

(b) Characteristic table



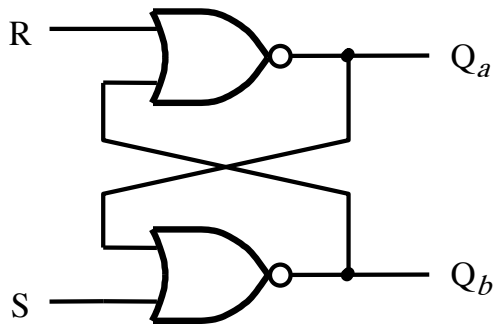
(c) Timing diagram

→ Time

[ Figure 5.4 from the textbook ]



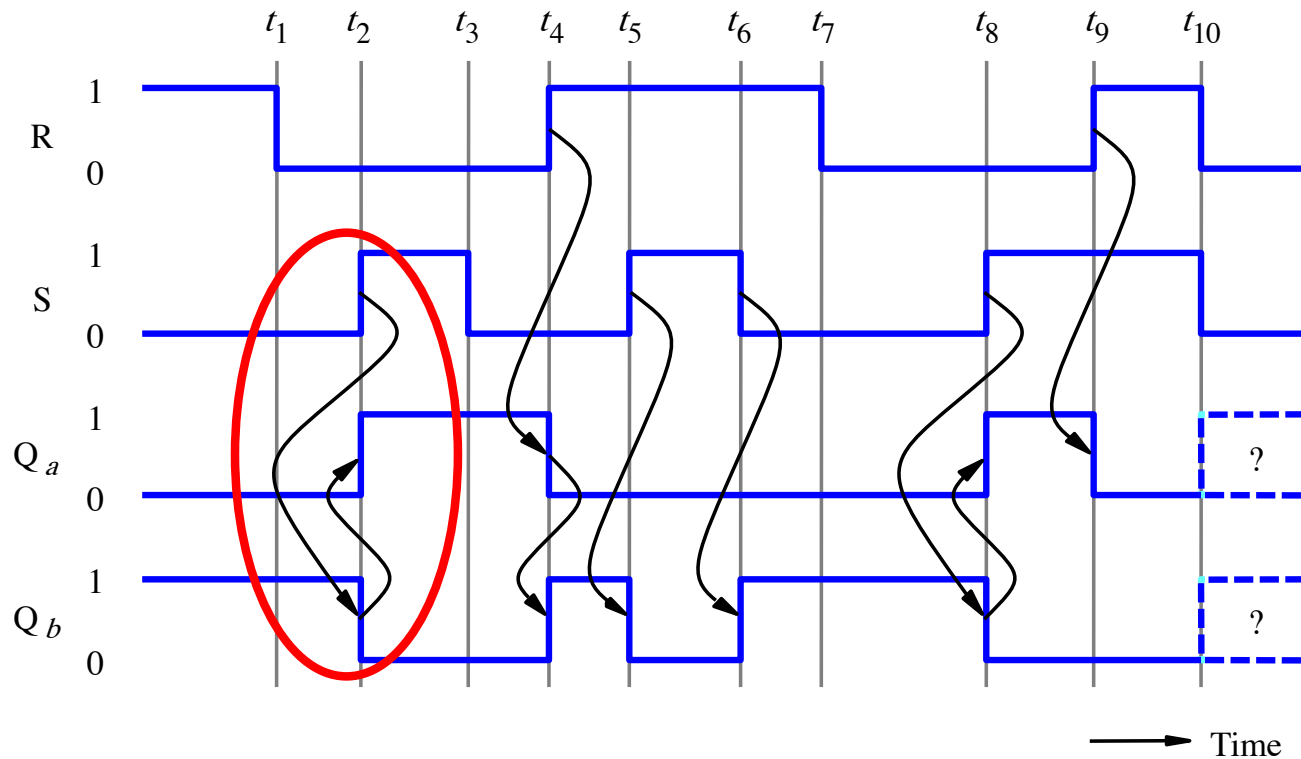
# Timing Diagram for the Basic Latch with NOR Gates



(a) Circuit

S	R	$Q_a$	$Q_b$
0	0	0/1	1/0 (no change)
0	1	0	1
1	0	1	0
1	1	0	0

(b) Characteristic table

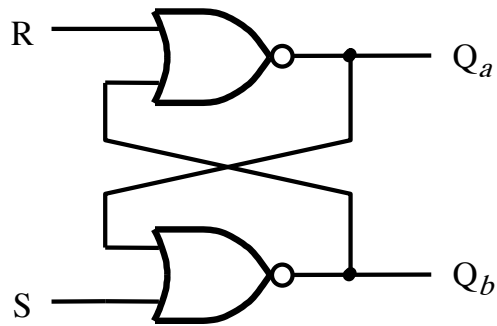


(c) Timing diagram

→ Time

[ Figure 5.4 from the textbook ]

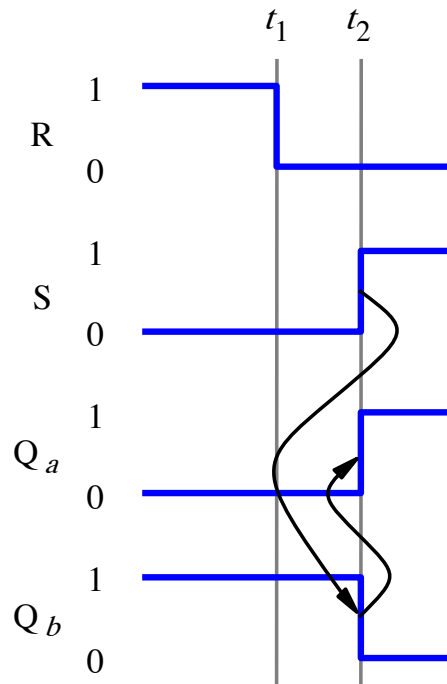
# Timing Diagram for the Basic Latch with NOR Gates



(a) Circuit

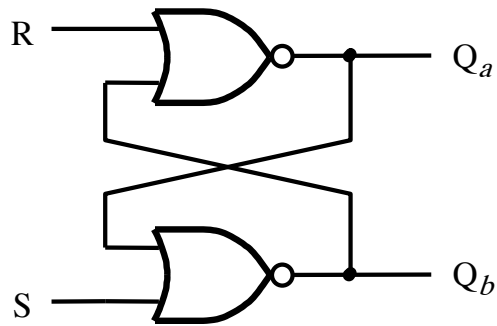
S	R	$Q_a$	$Q_b$	
0	0	0/1	1/0	(no change)
0	1	0	1	
1	0	1	0	
1	1	0	0	

(b) Characteristic table



(c) Timing diagram

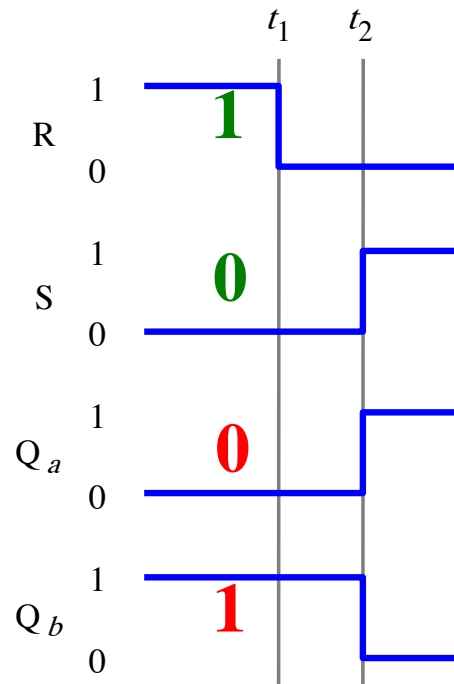
# Timing Diagram for the Basic Latch with NOR Gates



(a) Circuit

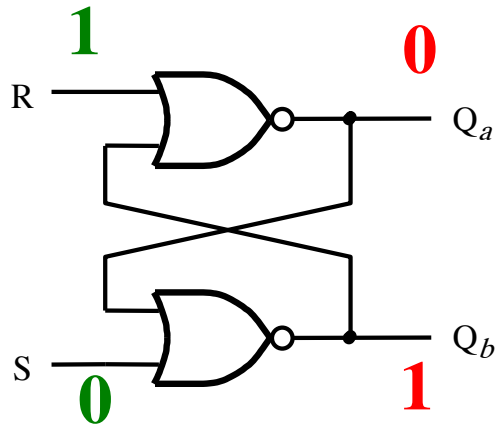
S	R	$Q_a$	$Q_b$	
0	0	0/1	1/0	(no change)
0	1	0	1	
1	0	1	0	
1	1	0	0	

(b) Characteristic table



(c) Timing diagram

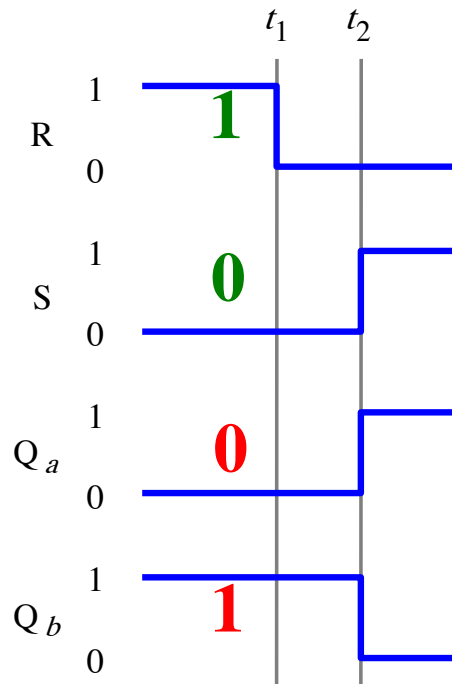
# Timing Diagram for the Basic Latch with NOR Gates



(a) Circuit

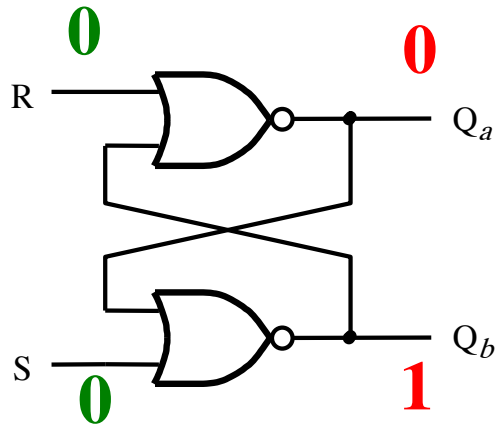
S	R	Q <sub>a</sub>	Q <sub>b</sub>	
0	0	0/1	1/0	(no change)
0	1	0	1	
1	0	1	0	
1	1	0	0	

(b) Characteristic table



(c) Timing diagram

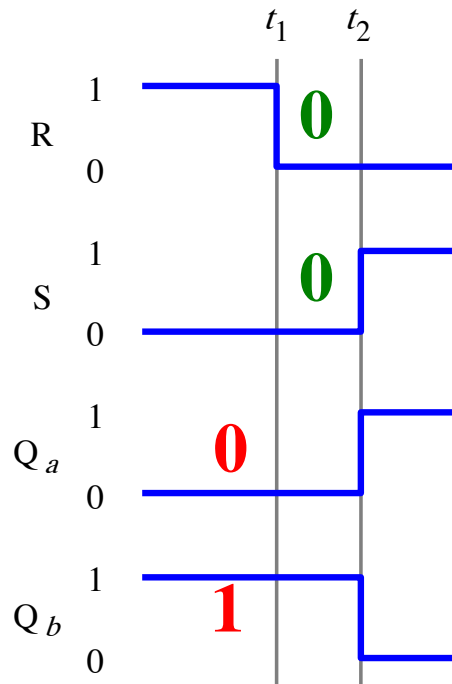
# Timing Diagram for the Basic Latch with NOR Gates



(a) Circuit

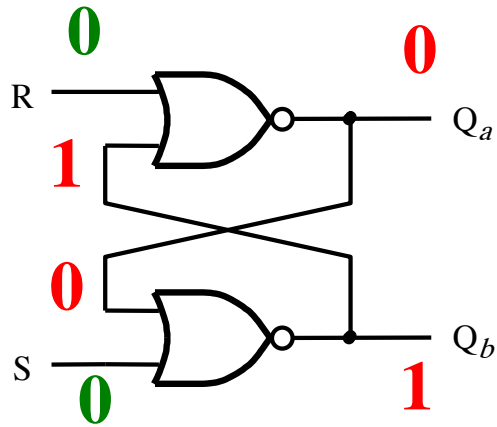
S	R	Q <sub>a</sub>	Q <sub>b</sub>	
0	0	0/1	1/0	(no change)
0	1	0	1	
1	0	1	0	
1	1	0	0	

(b) Characteristic table



(c) Timing diagram

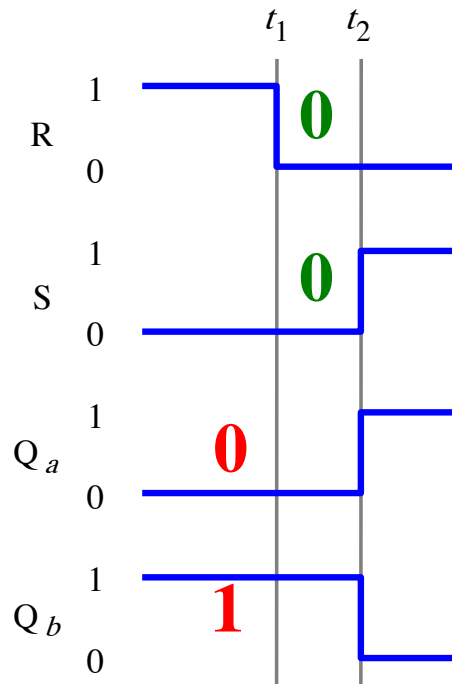
# Timing Diagram for the Basic Latch with NOR Gates



(a) Circuit

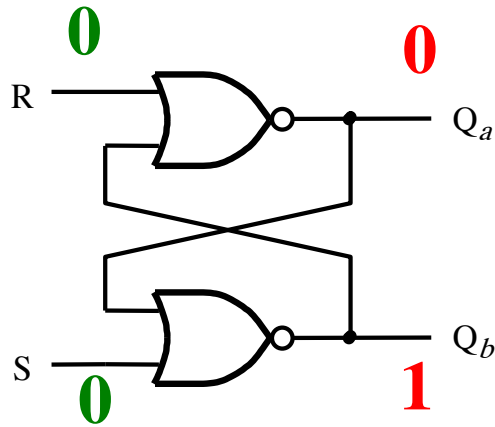
S	R	Q <sub>a</sub>	Q <sub>b</sub>	
0	0	0/1	1/0	(no change)
0	1	0	1	
1	0	1	0	
1	1	0	0	

(b) Characteristic table



(c) Timing diagram

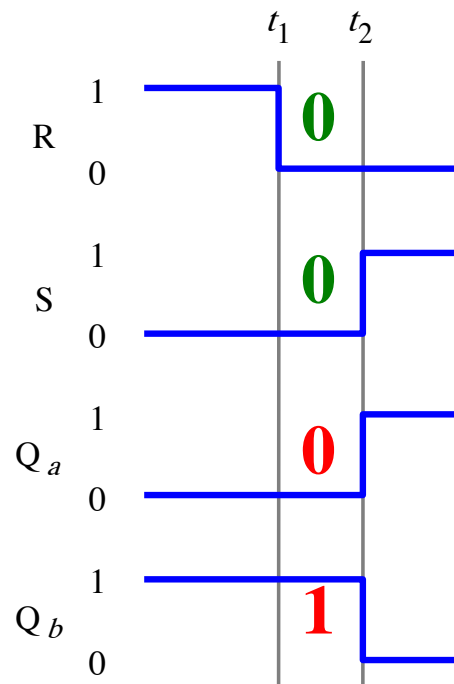
# Timing Diagram for the Basic Latch with NOR Gates



(a) Circuit

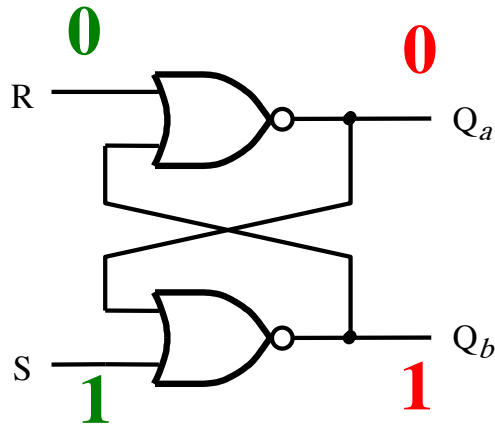
S	R	$Q_a$	$Q_b$	
0	0	0/1	1/0	(no change)
0	1	0	1	
1	0	1	0	
1	1	0	0	

(b) Characteristic table



(c) Timing diagram

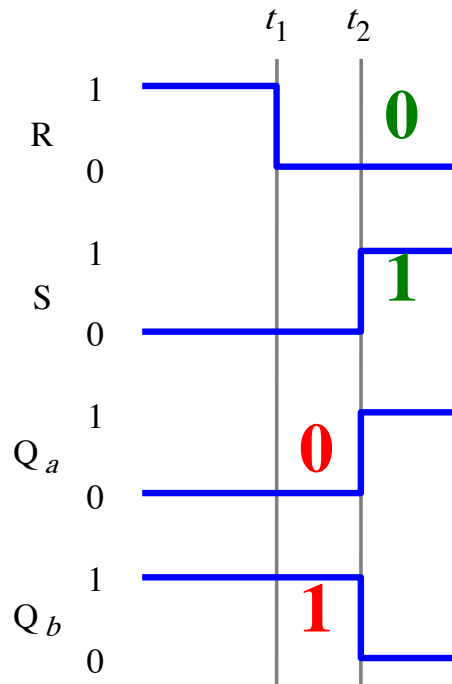
# Timing Diagram for the Basic Latch with NOR Gates



(a) Circuit

S	R	Q <sub>a</sub>	Q <sub>b</sub>	
0	0	0/1	1/0	(no change)
0	1	0	1	
1	0	1	0	
1	1	0	0	

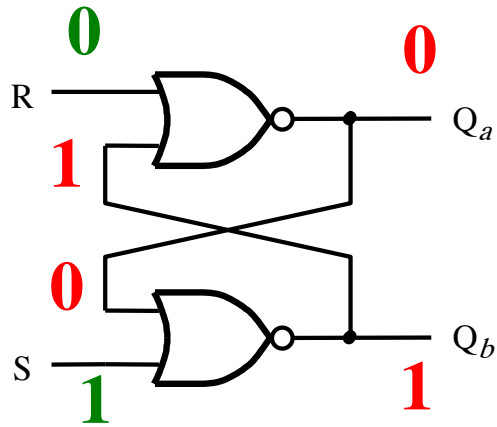
(b) Characteristic table



(c) Timing diagram



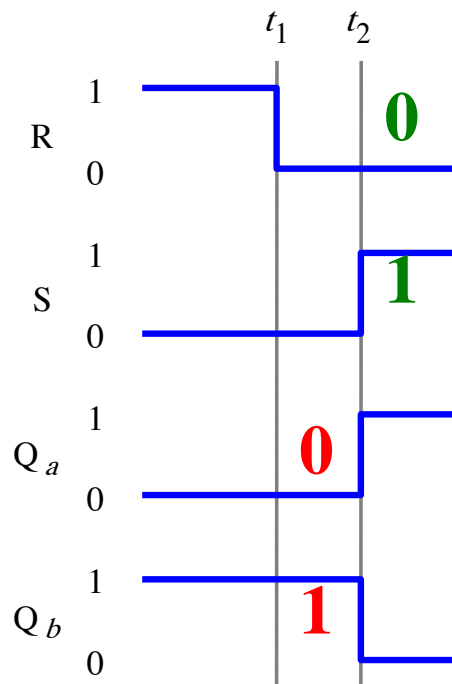
# Timing Diagram for the Basic Latch with NOR Gates



(a) Circuit

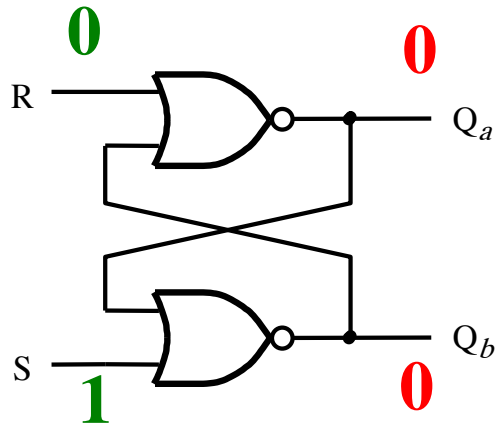
S	R	Q <sub>a</sub>	Q <sub>b</sub>	
0	0	0/1	1/0	(no change)
0	1	0	1	
1	0	1	0	
1	1	0	0	

(b) Characteristic table



(c) Timing diagram

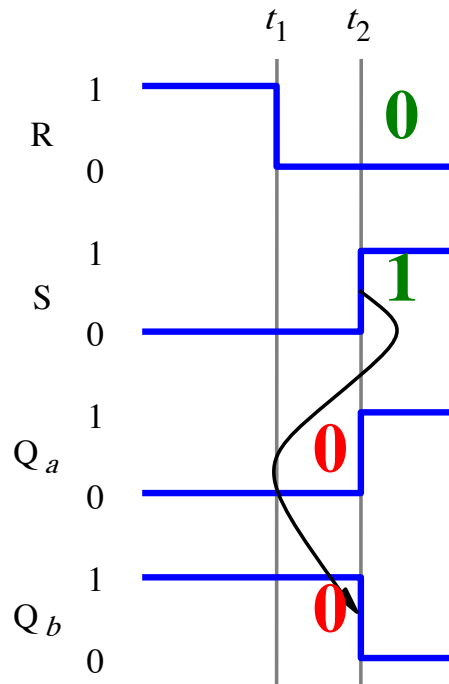
# Timing Diagram for the Basic Latch with NOR Gates



(a) Circuit

S	R	Q <sub>a</sub>	Q <sub>b</sub>	
0	0	0/1	1/0	(no change)
0	1	0	1	
1	0	1	0	
1	1	0	0	

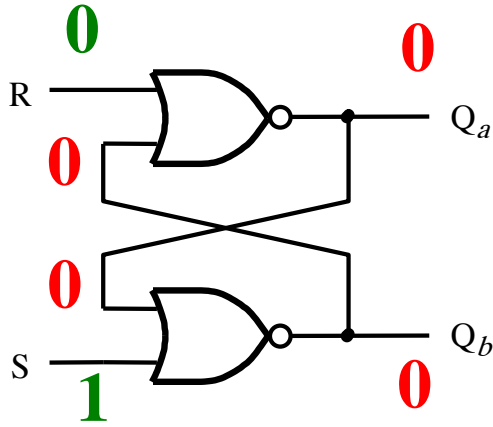
(b) Characteristic table



(c) Timing diagram

For a brief moment the latch goes through the undesirable state  $Q_a=0$  and  $Q_b=0$ .

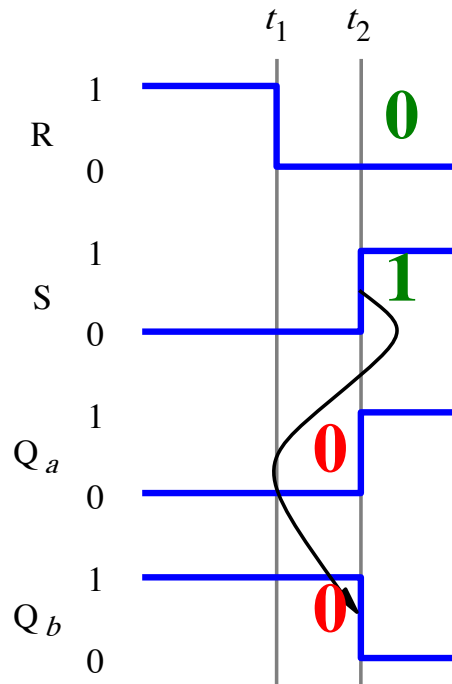
# Timing Diagram for the Basic Latch with NOR Gates



(a) Circuit

S	R	Q <sub>a</sub>	Q <sub>b</sub>	
0	0	0/1	1/0	(no change)
0	1	0	1	
1	0	1	0	
1	1	0	0	

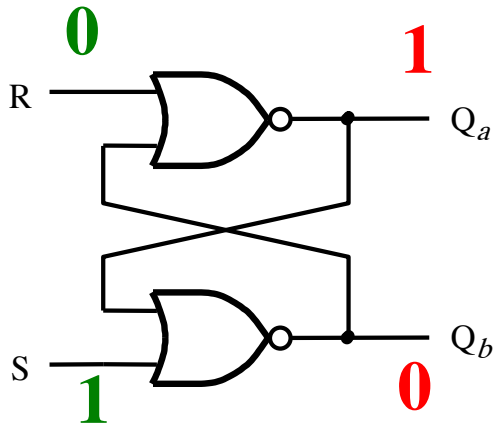
(b) Characteristic table



(c) Timing diagram

But these zeros loop around ...

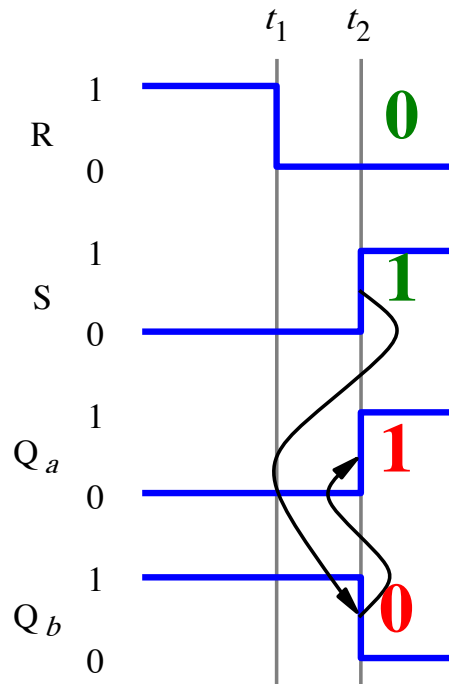
# Timing Diagram for the Basic Latch with NOR Gates



(a) Circuit

S	R	Q <sub>a</sub>	Q <sub>b</sub>	
0	0	0/1	1/0	(no change)
0	1	0	1	
1	0	1	0	
1	1	0	0	

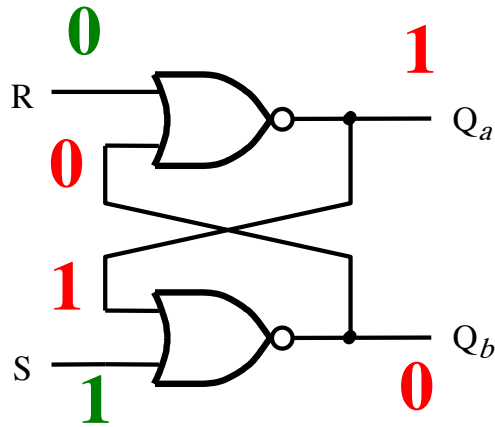
(b) Characteristic table



(c) Timing diagram

... and set it to  $Q_a=1$  and  $Q_b=0$ .

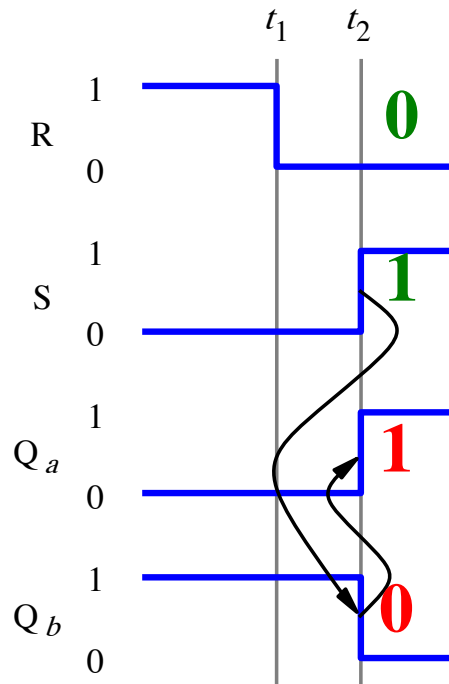
# Timing Diagram for the Basic Latch with NOR Gates



(a) Circuit

S	R	Q <sub>a</sub>	Q <sub>b</sub>	
0	0	0/1	1/0	(no change)
0	1	0	1	
1	0	1	0	
1	1	0	0	

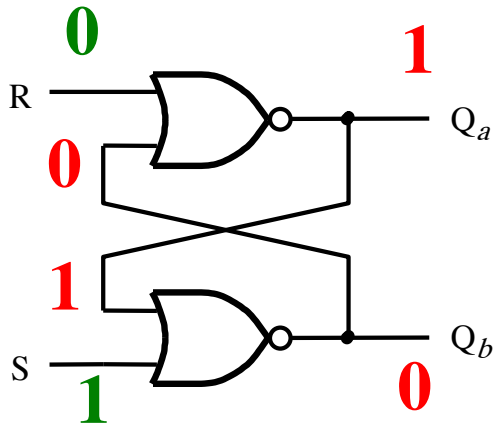
(b) Characteristic table



(c) Timing diagram

The new values also loop around ...

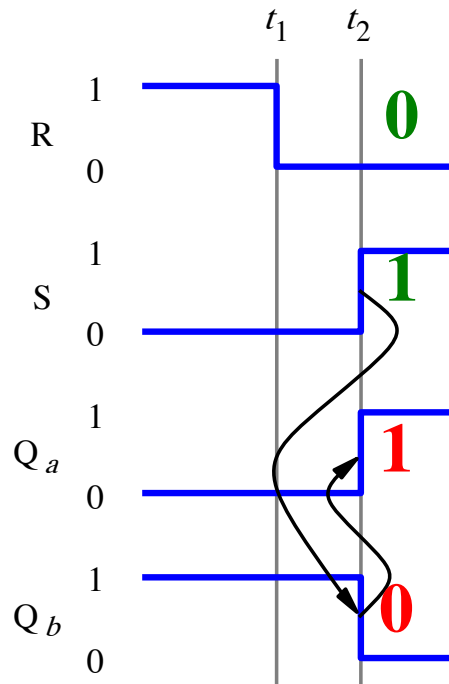
# Timing Diagram for the Basic Latch with NOR Gates



(a) Circuit

S	R	Q <sub>a</sub>	Q <sub>b</sub>	
0	0	0/1	1/0	(no change)
0	1	0	1	
1	0	1	0	
1	1	0	0	

(b) Characteristic table

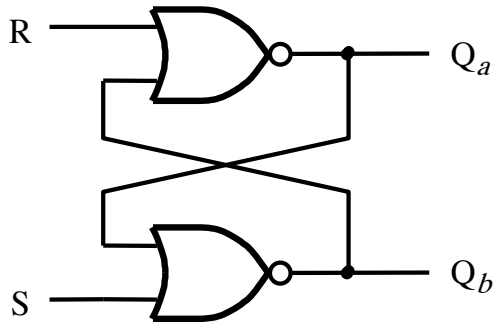


(c) Timing diagram

... but they leave the outputs the same.



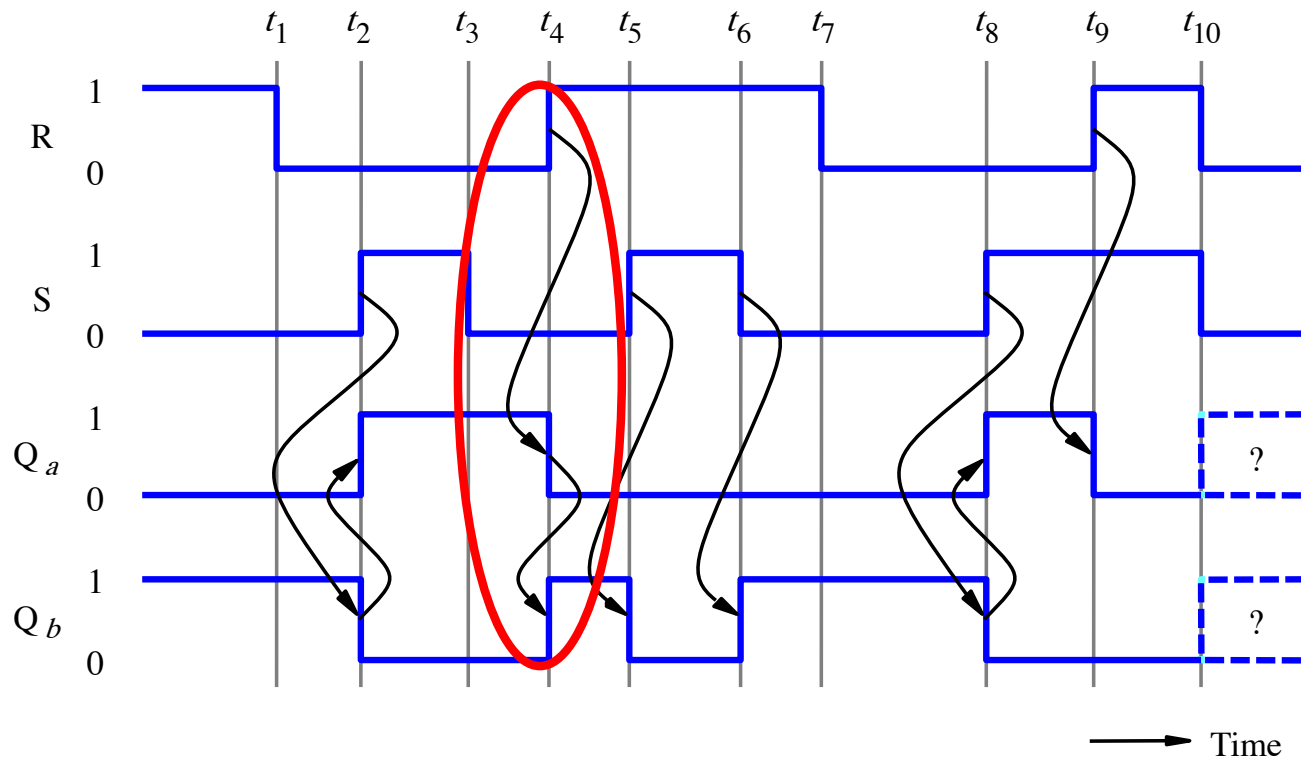
# Timing Diagram for the Basic Latch with NOR Gates



(a) Circuit

S	R	$Q_a$	$Q_b$
0	0	0/1	1/0 (no change)
0	1	0	1
1	0	1	0
1	1	0	0

(b) Characteristic table

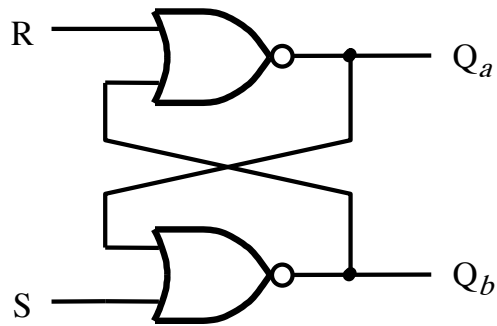


(c) Timing diagram

[ Figure 5.4 from the textbook ]



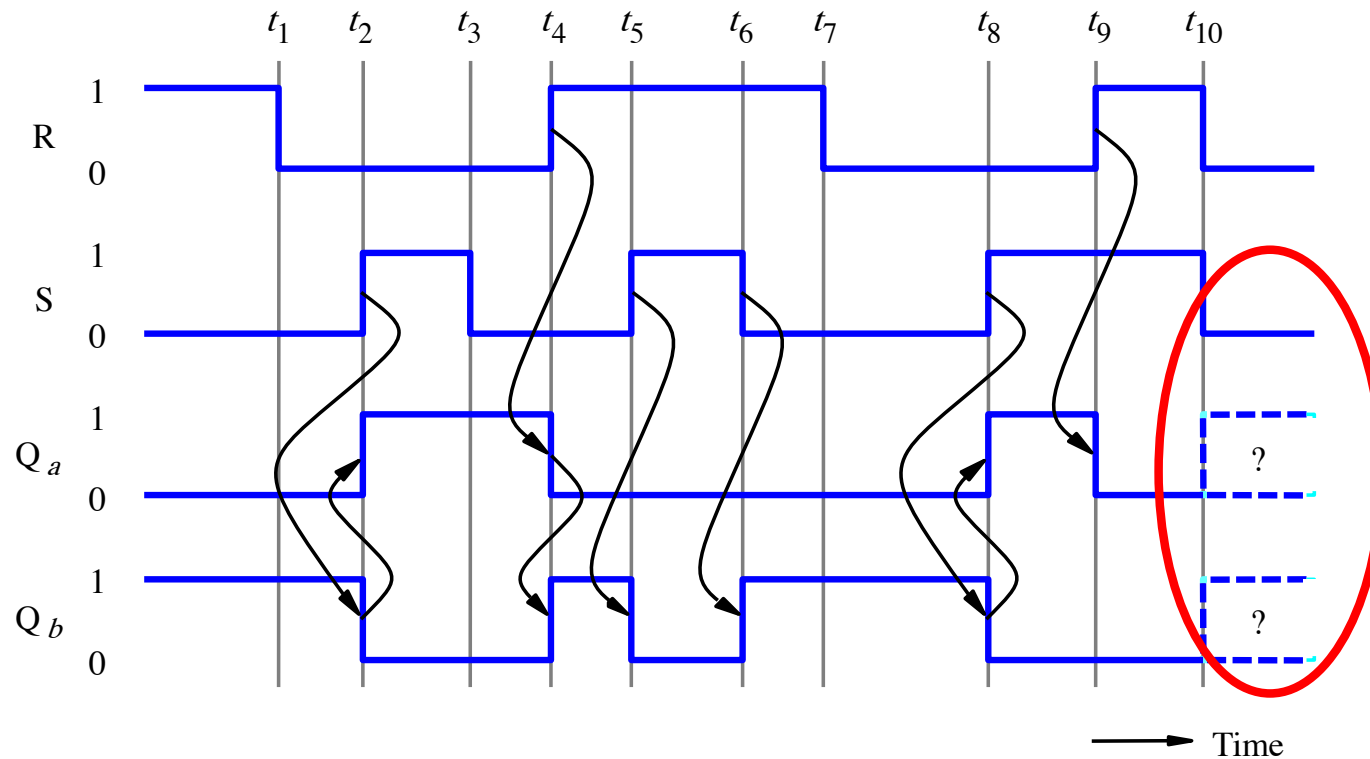
# Timing Diagram for the Basic Latch with NOR Gates



(a) Circuit

S	R	$Q_a$	$Q_b$
0	0	0/1	1/0 (no change)
0	1	0	1
1	0	1	0
1	1	0	0

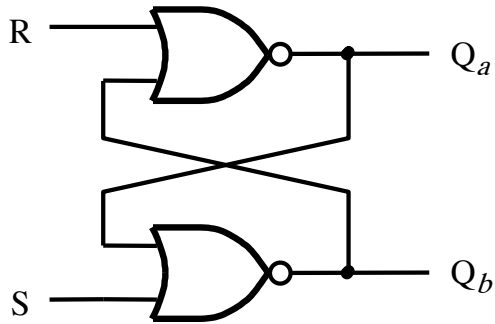
(b) Characteristic table



(c) Timing diagram

[ Figure 5.4 from the textbook ]

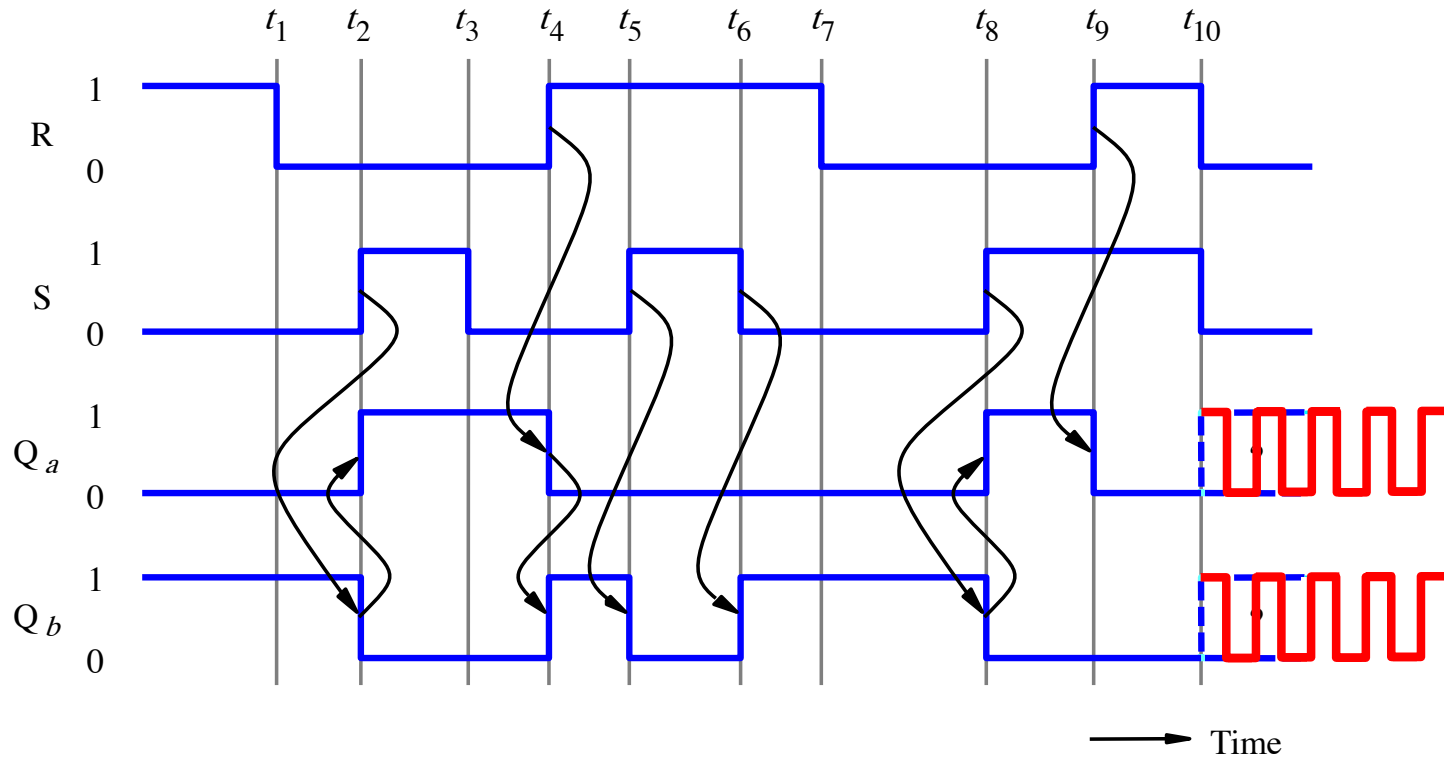
# Timing Diagram for the Basic Latch with NOR Gates



(a) Circuit

S	R	$Q_a$	$Q_b$
0	0	0/1	1/0 (no change)
0	1	0	1
1	0	1	0
1	1	0	0

(b) Characteristic table

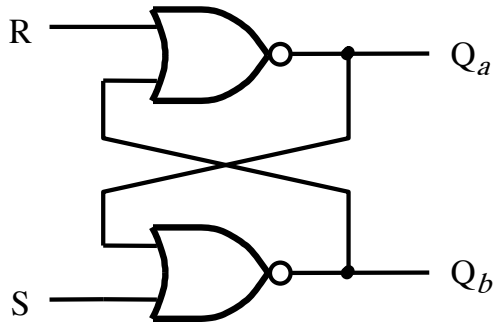


(c) Timing diagram

→ Time

[ Figure 5.4 from the textbook ]

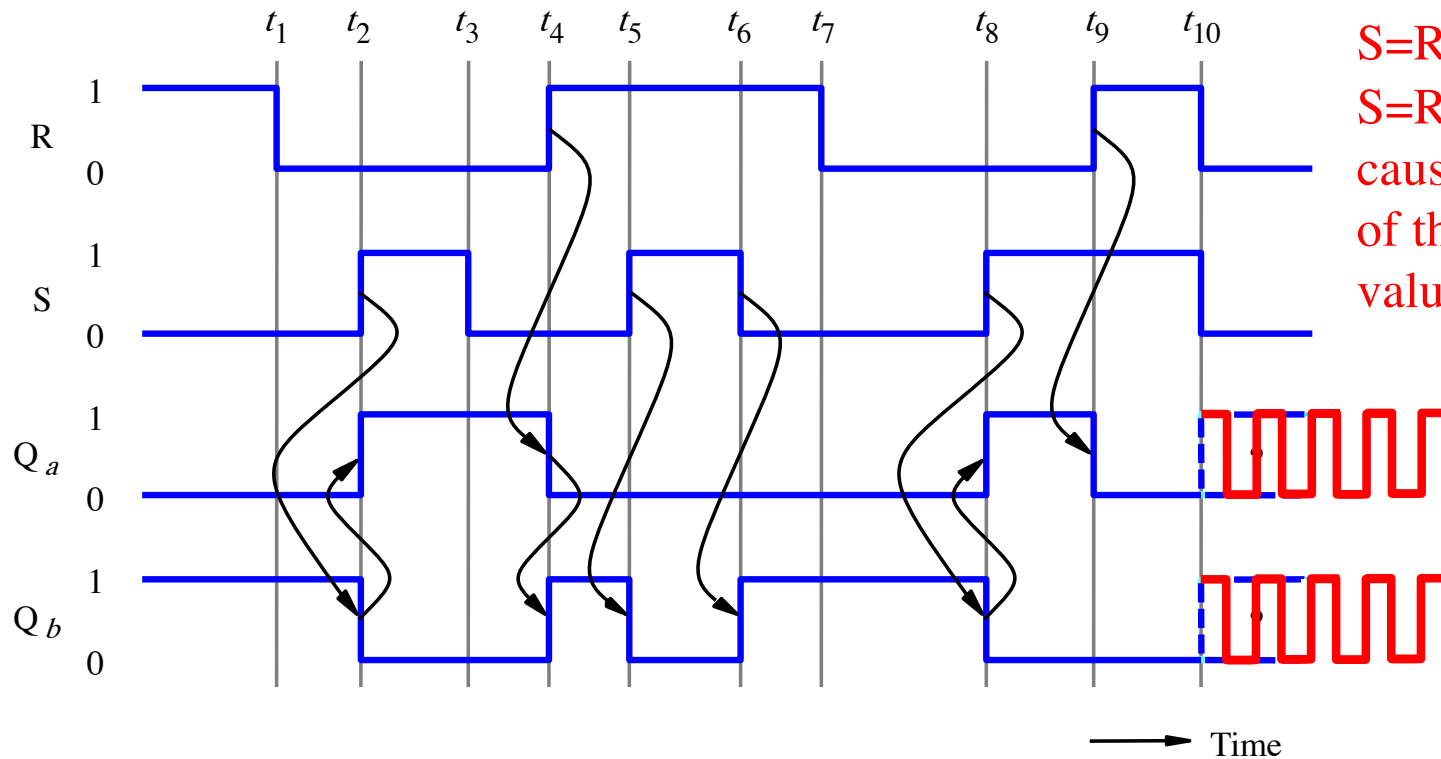
# Timing Diagram for the Basic Latch with NOR Gates



(a) Circuit

S	R	$Q_a$	$Q_b$
0	0	0/1	1/0 (no change)
0	1	0	1
1	0	1	0
1	1	0	0

(b) Characteristic table



A transition from  $S=R=1$  to  $S=R=0$  causes oscillations of the two output values  $Q_a$  and  $Q_b$ .

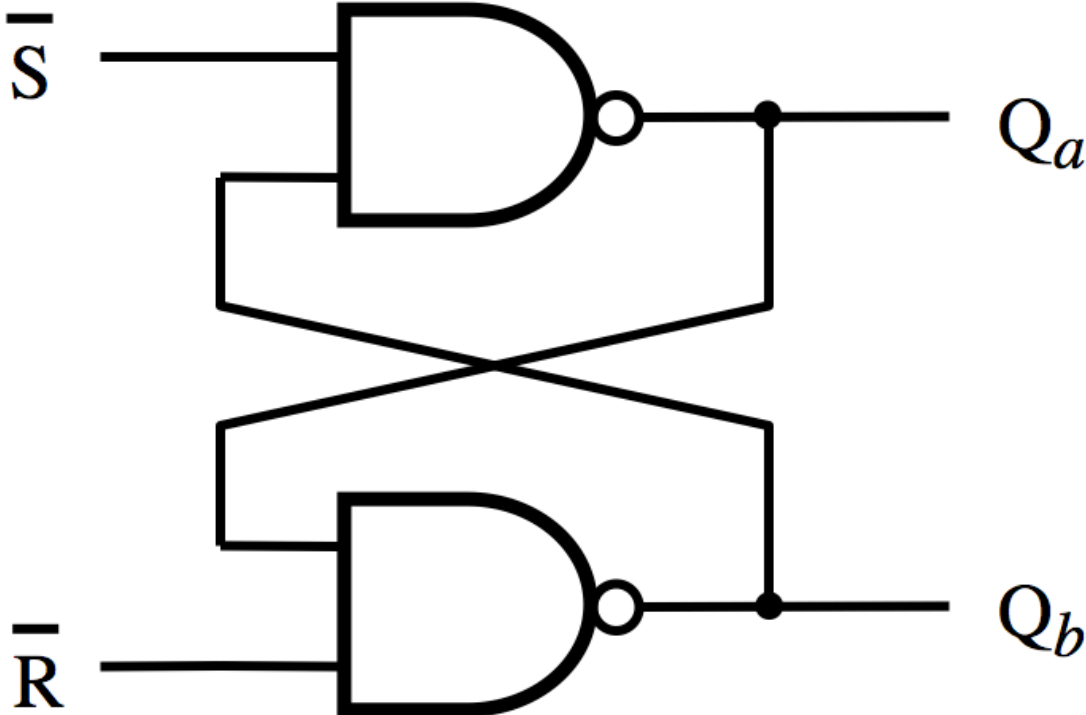
(c) Timing diagram

→ Time

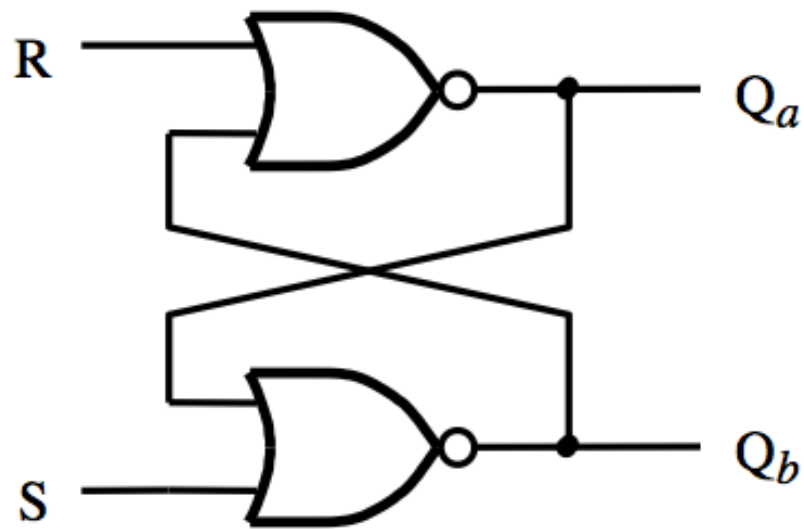
[ Figure 5.4 from the textbook ]

# **Basic Latch with NAND Gates**

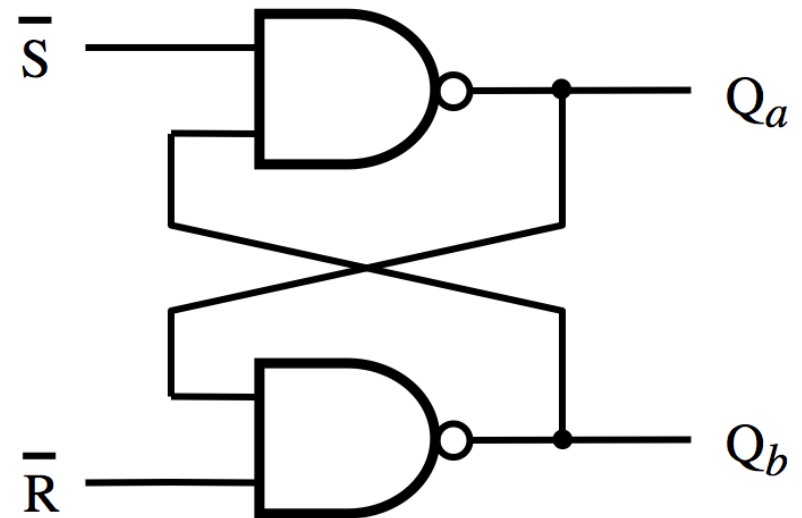
# Circuit for the Basic Latch with NAND Gates



## Basic Latch (with NOR Gates)



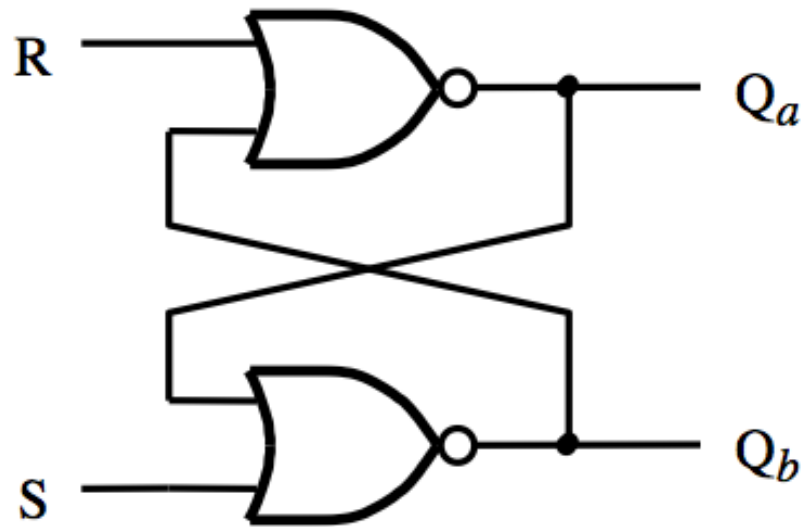
## Basic Latch (with NAND Gates)



Notice that in the NAND case the two inputs are swapped and negated.

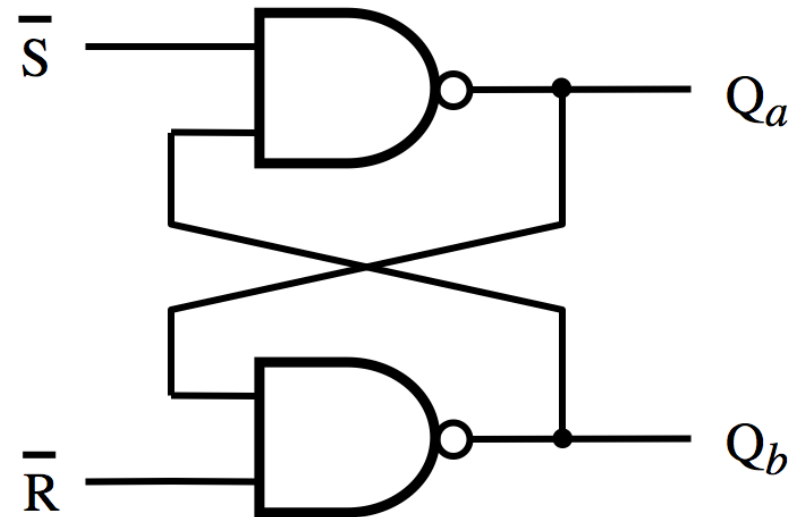
The labels of the outputs are the same in both cases.

# Basic Latch (with NOR Gates)



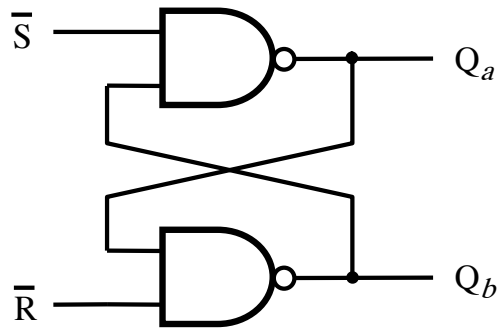
SR Latch

# Basic Latch (with NAND Gates)



$\bar{S}\bar{R}$  Latch

# Circuit and Characteristic Table



(a) Circuit

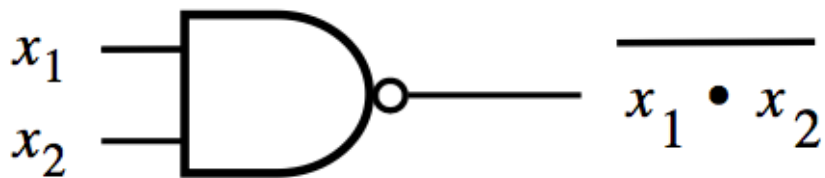
$\bar{S}$	$\bar{R}$	$Q_a$	$Q_b$
0	0	1	1
0	1	1	0
1	0	0	1
1	1	0/1	1/0 (no change)

(b) Characteristic table (version 1)

S	R	$Q_a$	$Q_b$
0	0	0/1	1/0 (no change)
0	1	0	1
1	0	1	0
1	1	1	1

(c) Characteristic table (version 2)

## NAND Gate

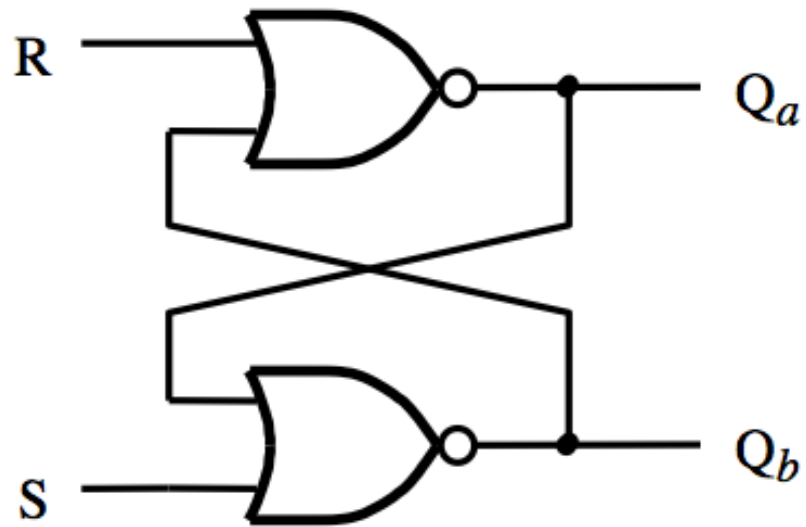


## NAND Gate Truth table

$x_1$	$x_2$	f
0	0	1
0	1	1
1	0	1
1	1	0

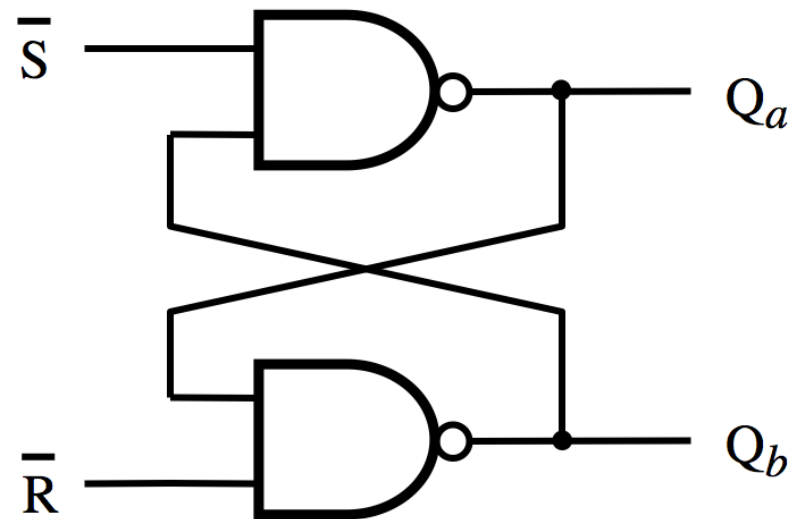


# Basic Latch (with NOR Gates)



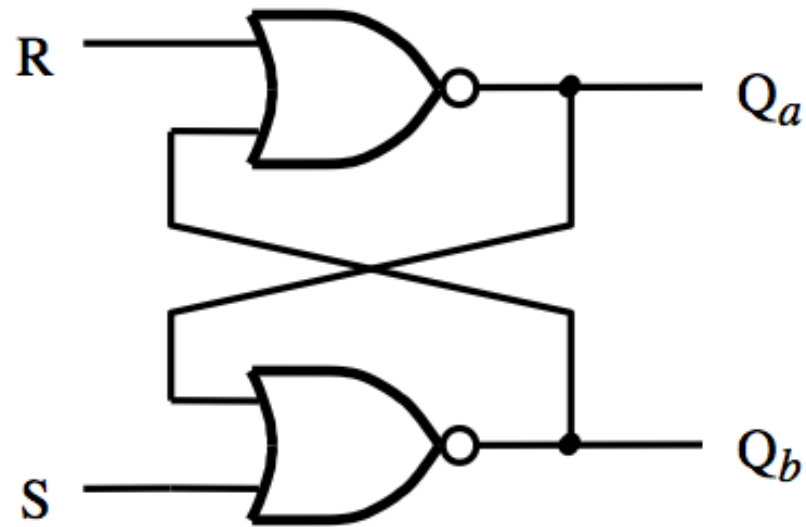
S	R	$Q_a$	$Q_b$	
0	0	0/1	1/0	(no change)
0	1	0	1	
1	0	1	0	
1	1	0	0	

# Basic Latch (with NAND Gates)



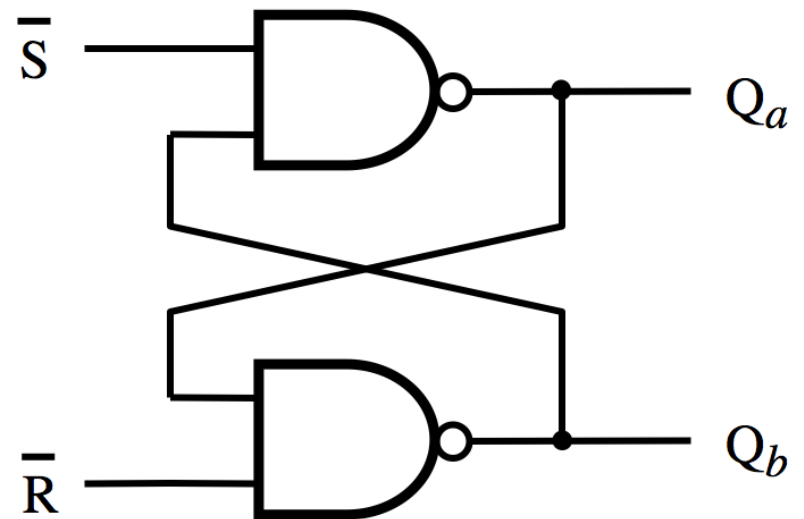
S	R	$Q_a$	$Q_b$	
0	0	0/1	1/0	(no change)
0	1	0	1	
1	0	1	0	
1	1	1	1	

# Basic Latch (with NOR Gates)



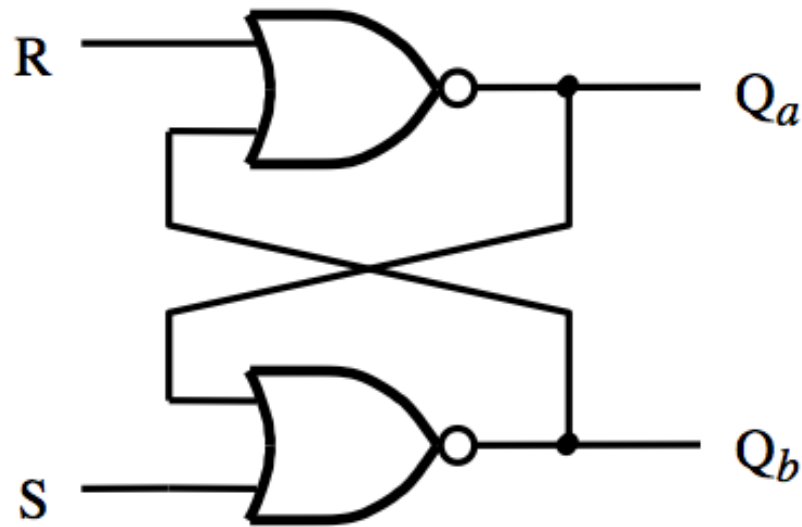
S	R	$Q_a$	$Q_b$	
0	0	0/1	1/0	(no change) <b>Latch</b>
0	1	0	1	<b>Reset</b>
1	0	1	0	<b>Set</b>
1	1	0	0	<b>Undesirable</b>

# Basic Latch (with NAND Gates)



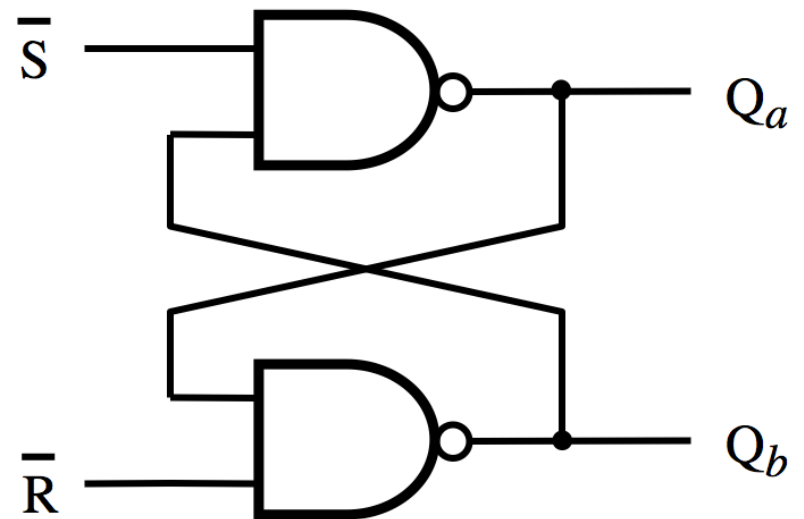
S	R	$Q_a$	$Q_b$	
0	0	0/1	1/0	(no change) <b>Latch</b>
0	1	0	1	<b>Reset</b>
1	0	1	0	<b>Set</b>
1	1	1	1	<b>Undesirable</b>

## Basic Latch (with NOR Gates)



S	R	$Q_a$	$Q_b$	
0	0	0/1	1/0	(no change) <b>Latch</b>
0	1	0	1	<b>Reset</b>
1	0	1	0	<b>Set</b>
1	1	0	0	<b>Undesirable</b>

## Basic Latch (with NAND Gates)



S	R	$Q_a$	$Q_b$	
0	0	0/1	1/0	(no change) <b>Latch</b>
0	1	0	1	<b>Reset</b>
1	0	1	0	<b>Set</b>
1	1	1	1	<b>Undesirable</b>

The two characteristic tables are the same  
(except for the last row, which is the undesirable configuration).

# Oscillations and Undesirable States

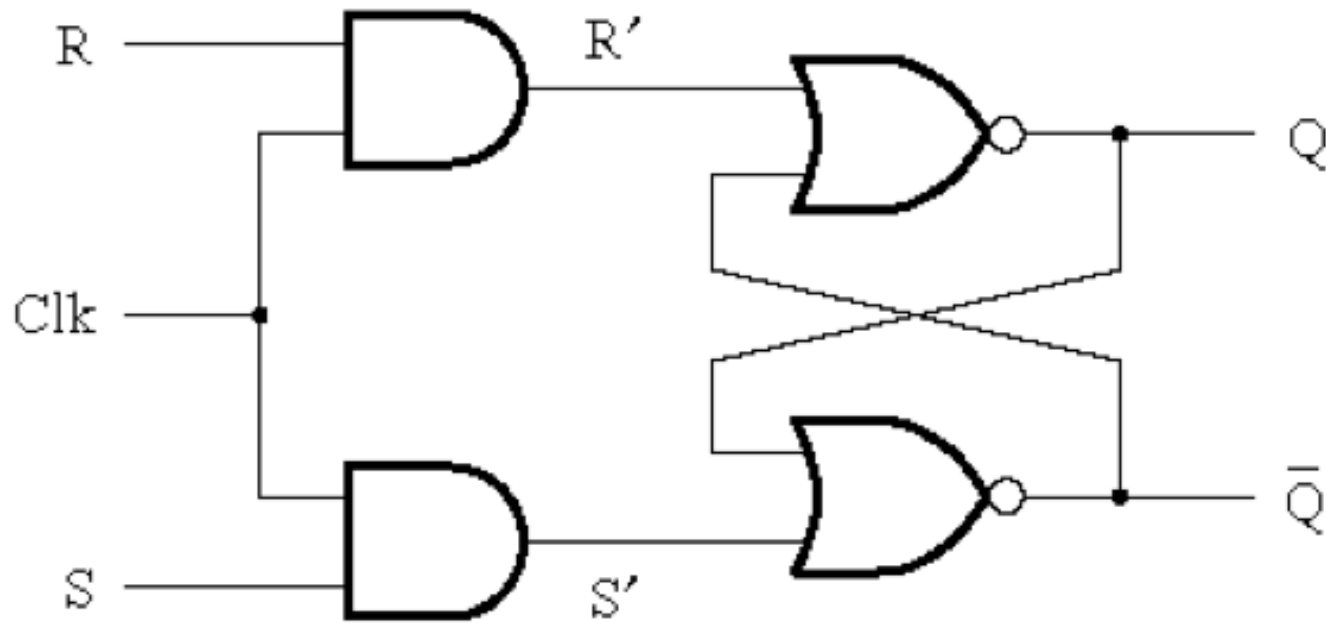
- **The basic latch with NAND gates also suffers from oscillation problems, similar to the basic latch implemented with NOR gates.**
- **Try to do this analysis on your own.**

# **Gated SR Latch**

# Motivation

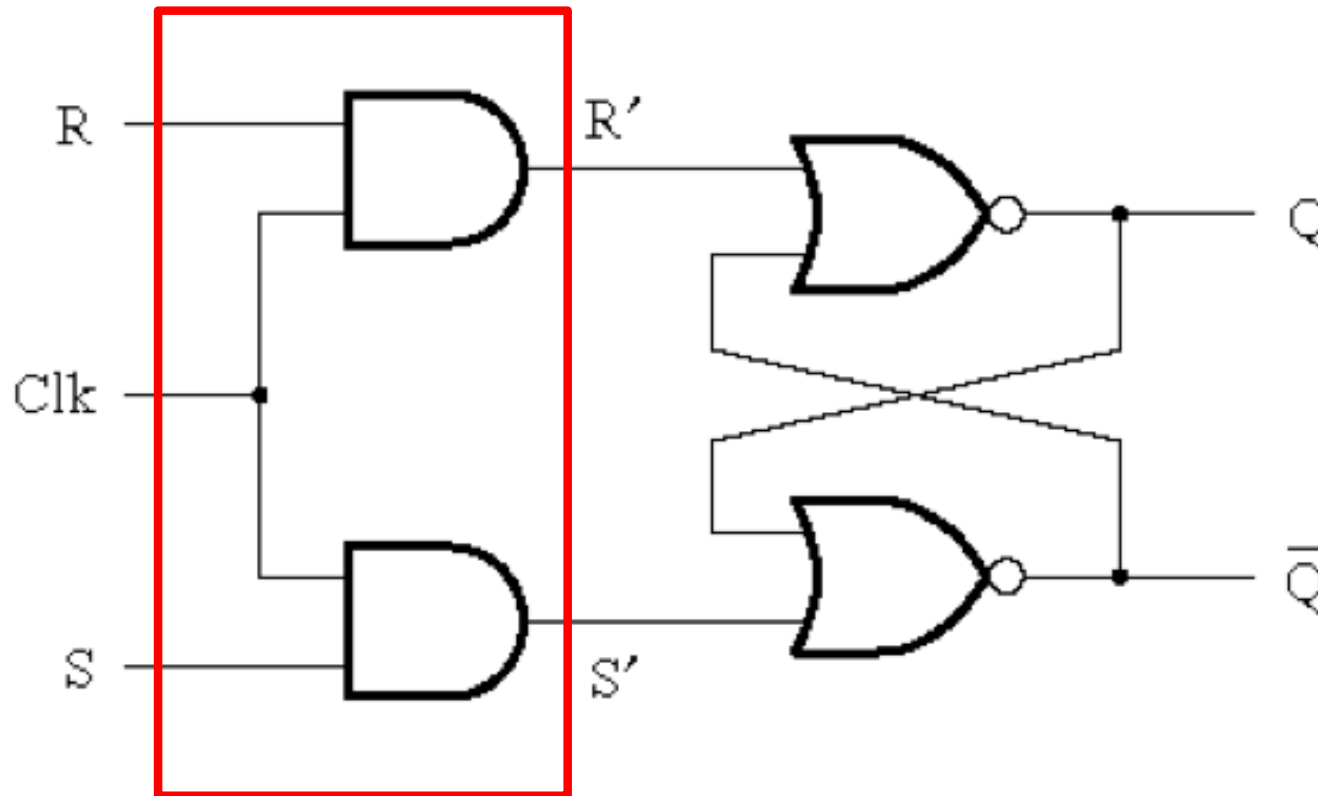
- **The basic latch changes its state when the input signals change**
- **It is hard to control when these input signals will change and thus it is hard to know when the latch may change its state.**
- **We want to have something like an Enable input.**
- **In this case it is called the “Clock” input because it is desirable for the state changes to be synchronized.**

# Circuit Diagram for the Gated SR Latch



[ Figure 5.5a from the textbook ]

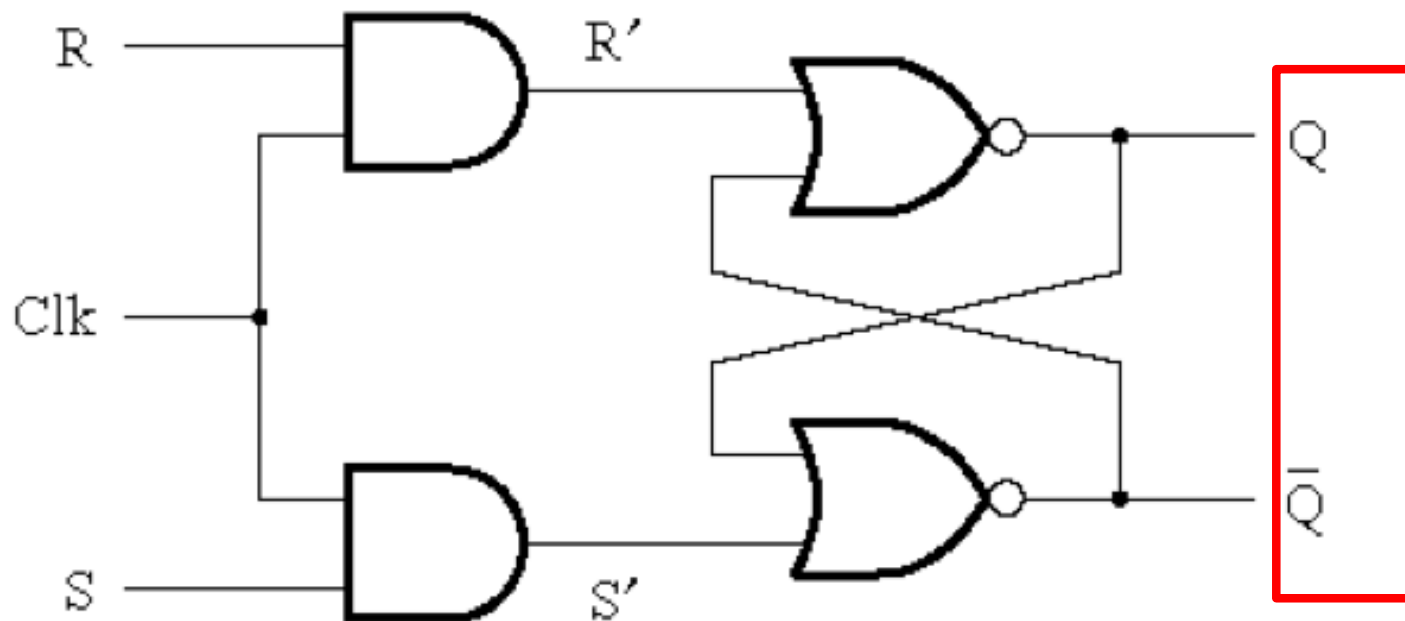
# Circuit Diagram for the Gated SR Latch



This is the “gate”  
of the gated latch

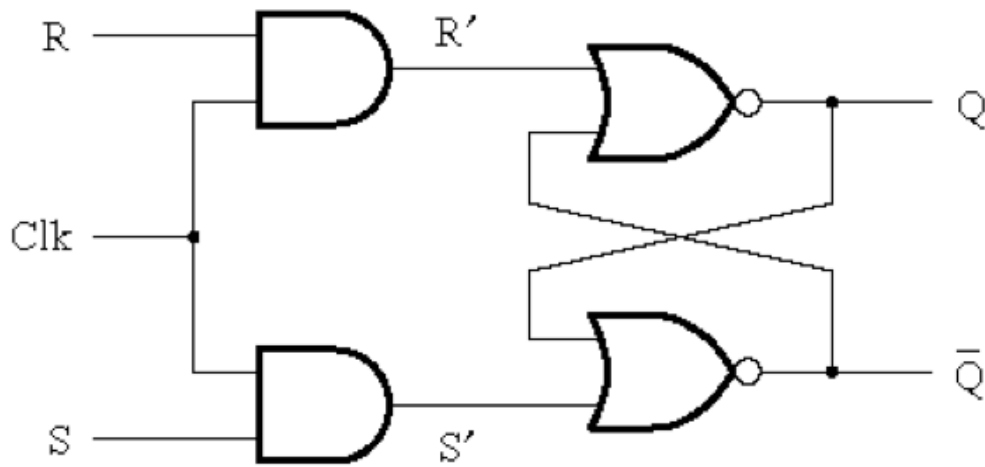


# Circuit Diagram for the Gated SR Latch



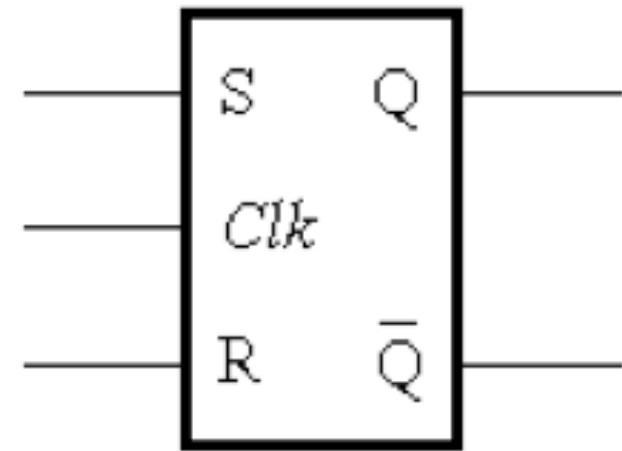
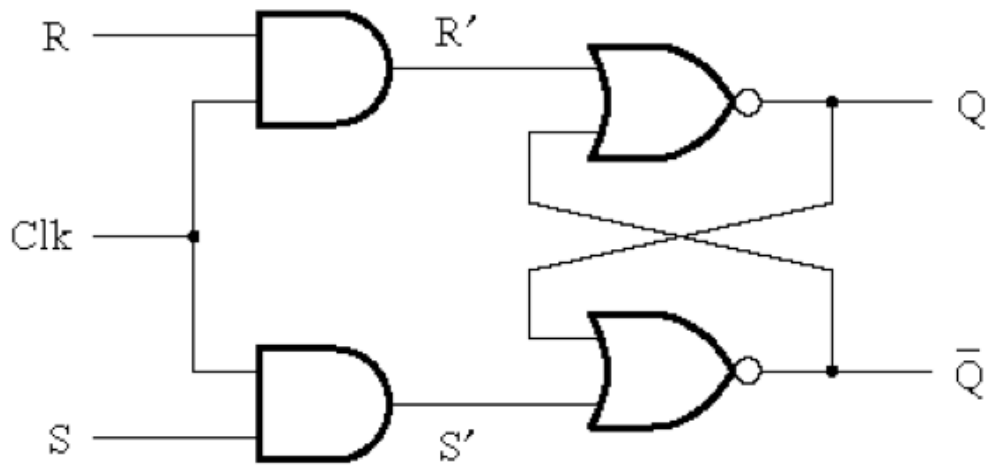
Notice that these are complements of each other

# Circuit Diagram and Characteristic Table for the Gated SR Latch

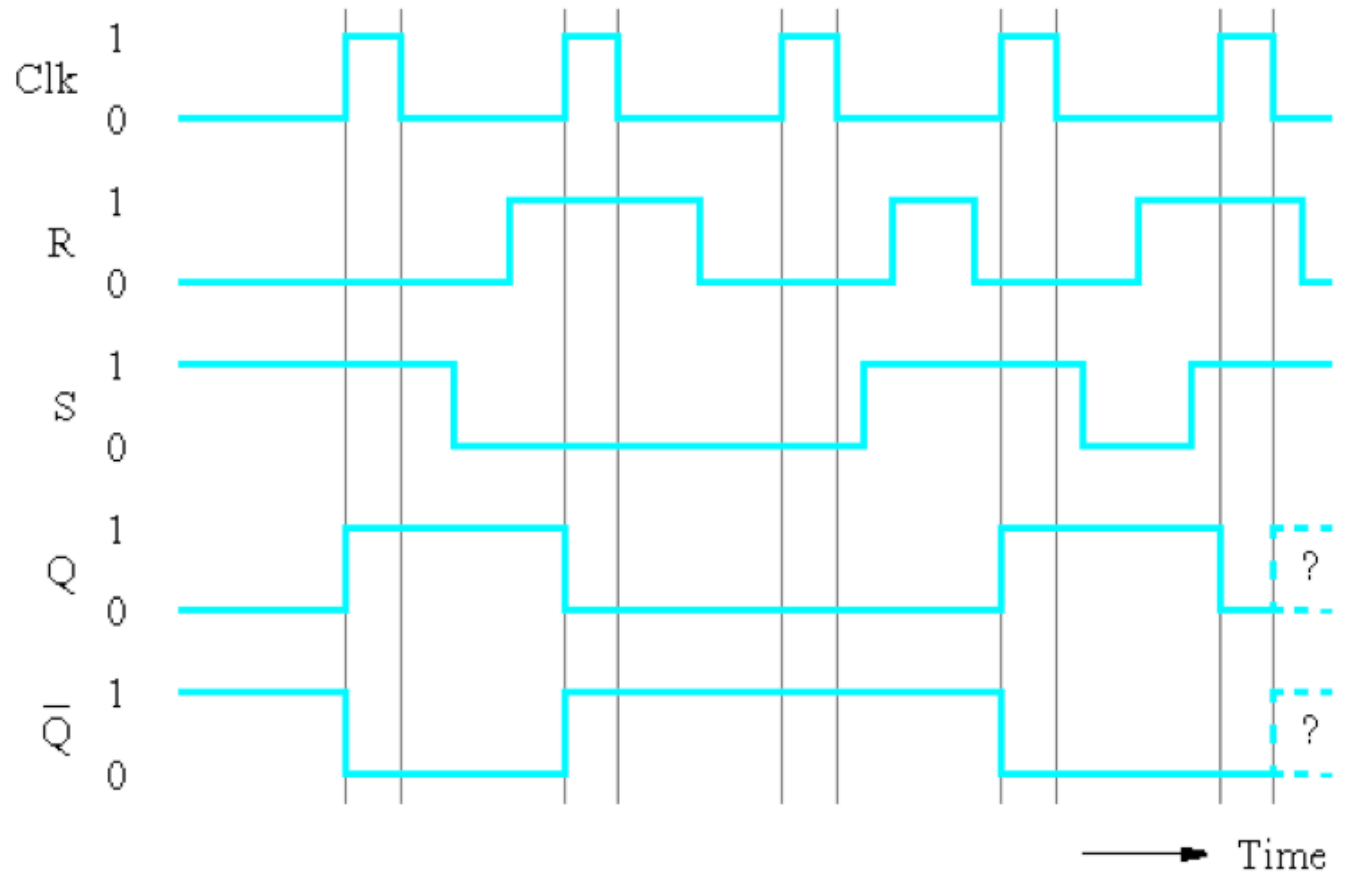
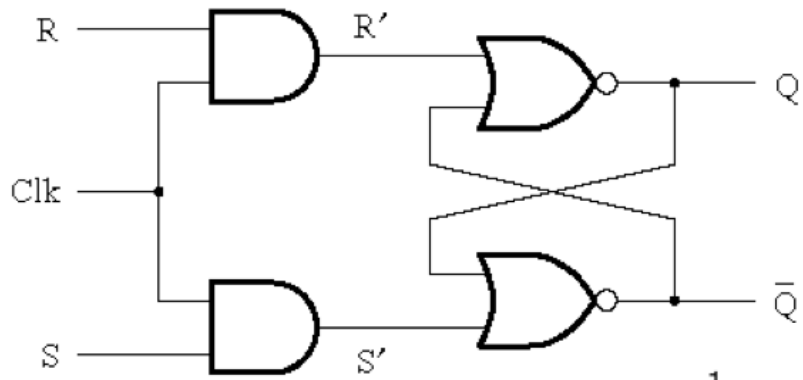


Clk	S	R	Q(t + 1)
0	x	x	Q(t) (no change)
1	0	0	Q(t) (no change)
1	0	1	0
1	1	0	1
1	1	1	x

# Circuit Diagram and Graphical Symbol for the Gated SR Latch

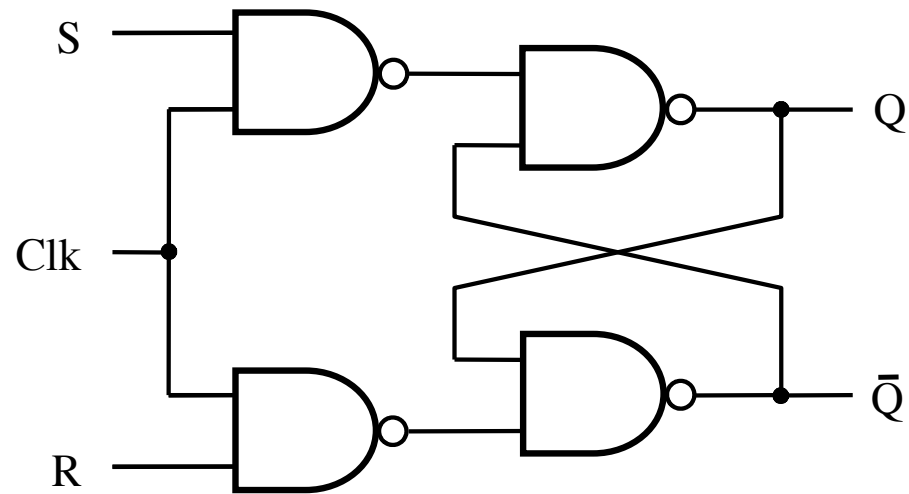


# Timing Diagram for the Gated SR Latch

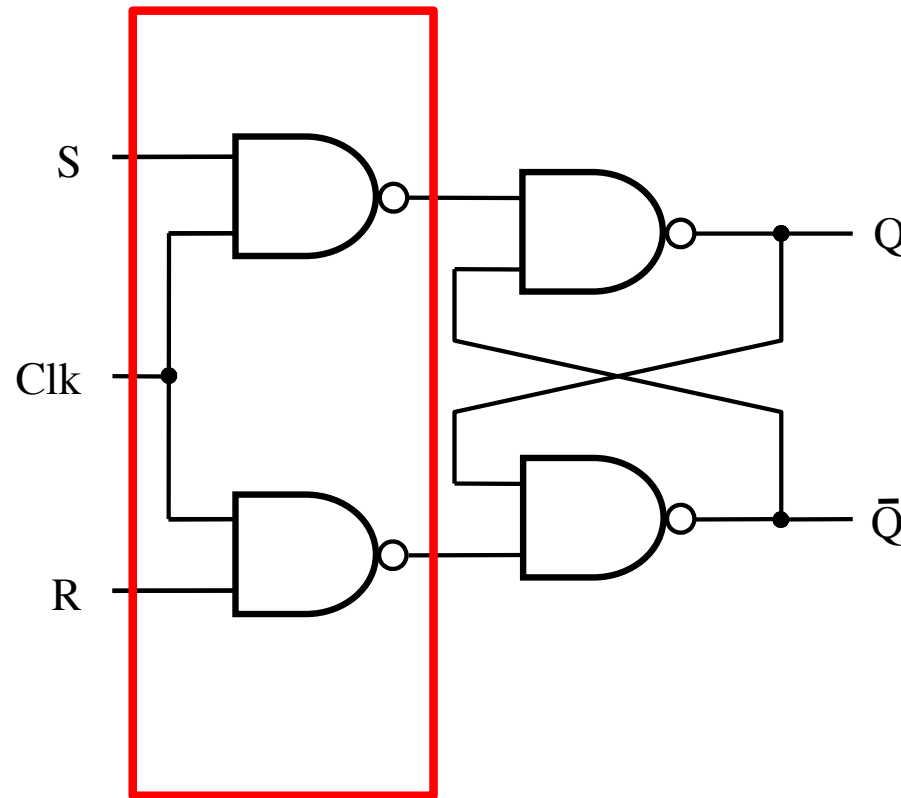


[ Figure 5.5c from the textbook ]

# Gated SR latch with NAND gates

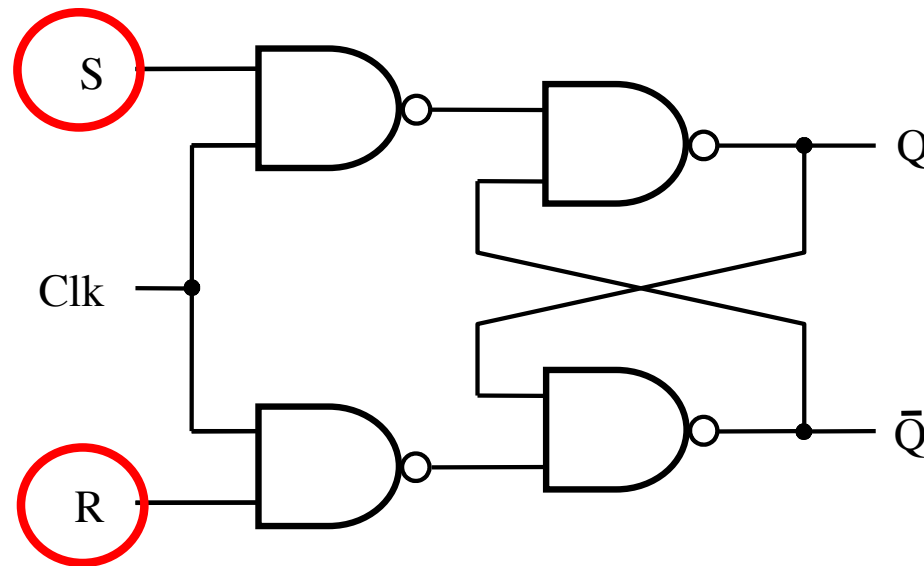


# Gated SR latch with NAND gates



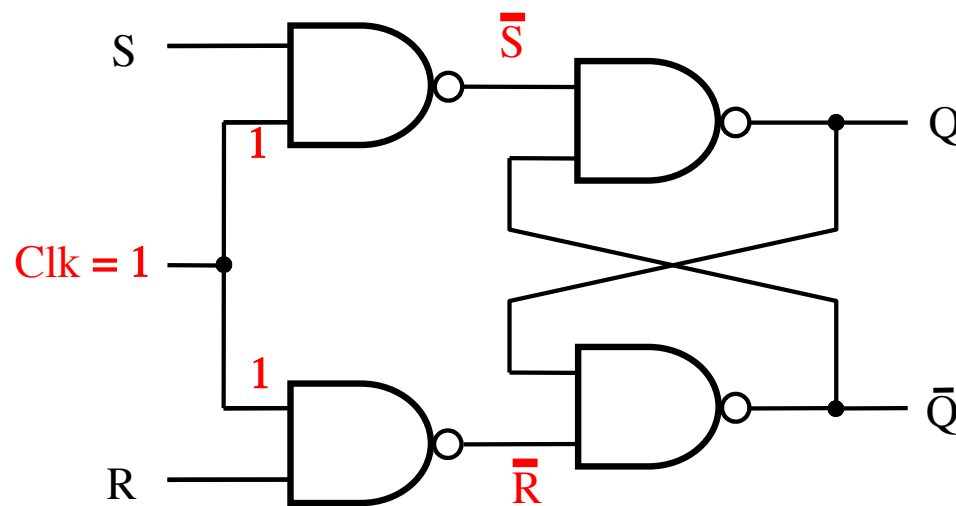
In this case the “gate” is constructed using NAND gates! Not AND gates.

# Gated SR latch with NAND gates



Also, notice that the positions of S and R are now swapped.

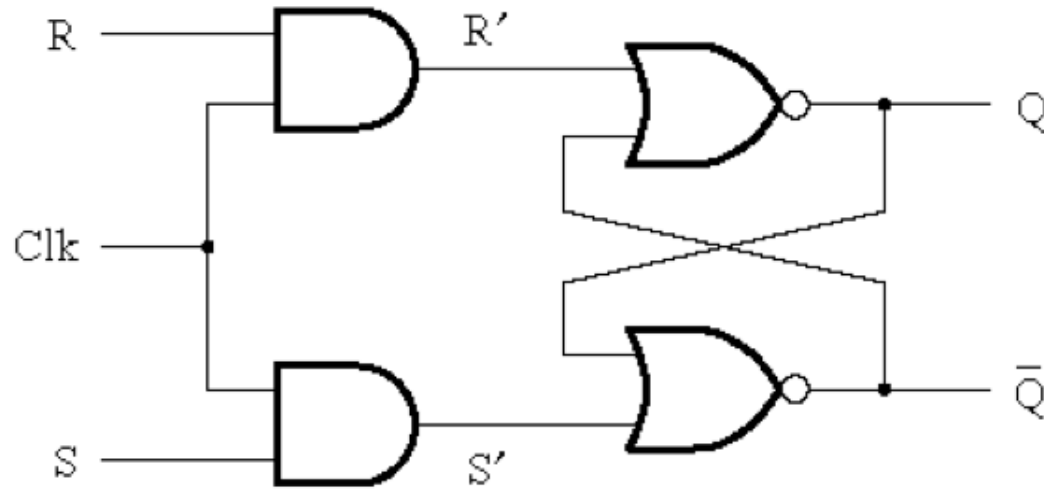
# Gated SR latch with NAND gates



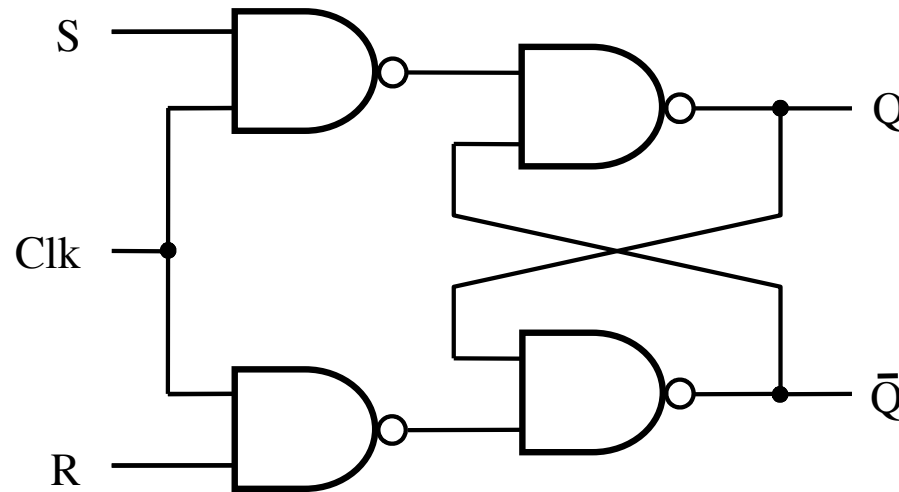
Finally, notice that when  $\text{Clk}=1$  this turns into the basic latch with NAND gates, i.e., the  $\bar{S}\bar{R}$  Latch.



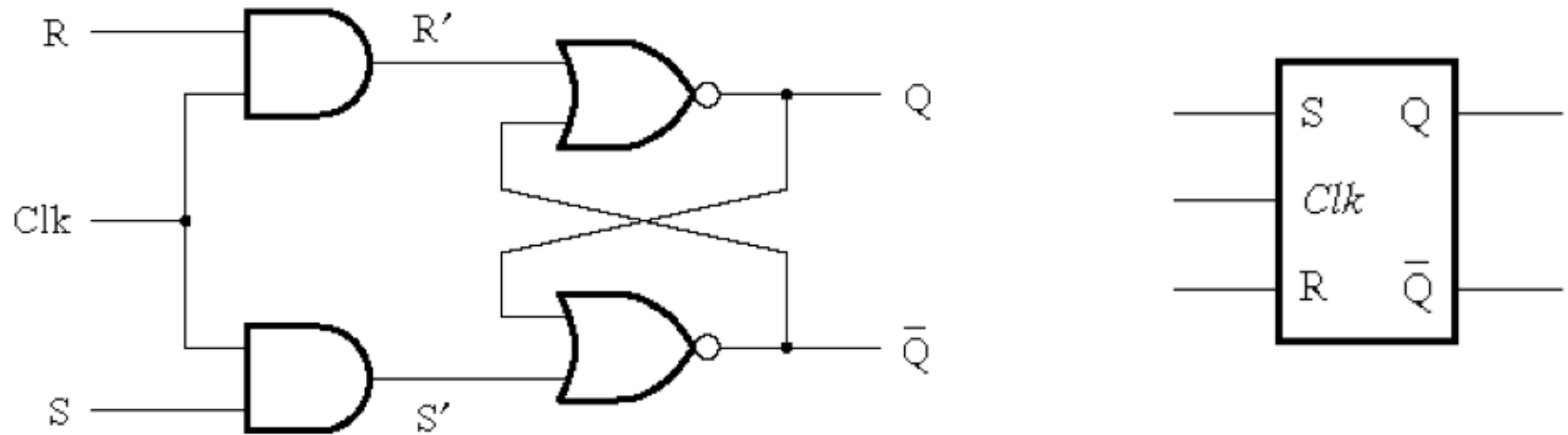
# Gated SR latch with NOR gates



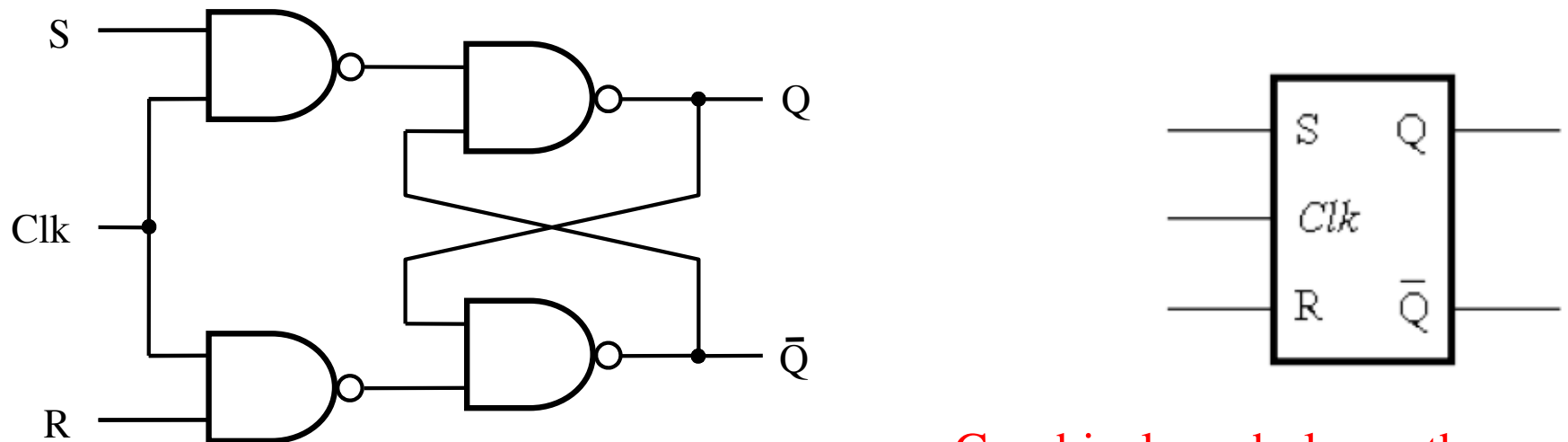
# Gated SR latch with NAND gates



# Gated SR latch with NOR gates

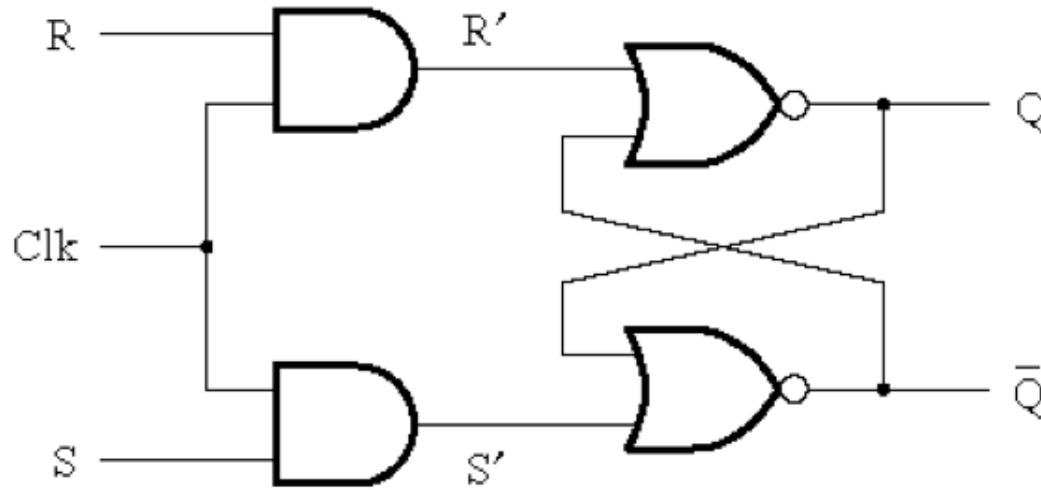


# Gated SR latch with NAND gates



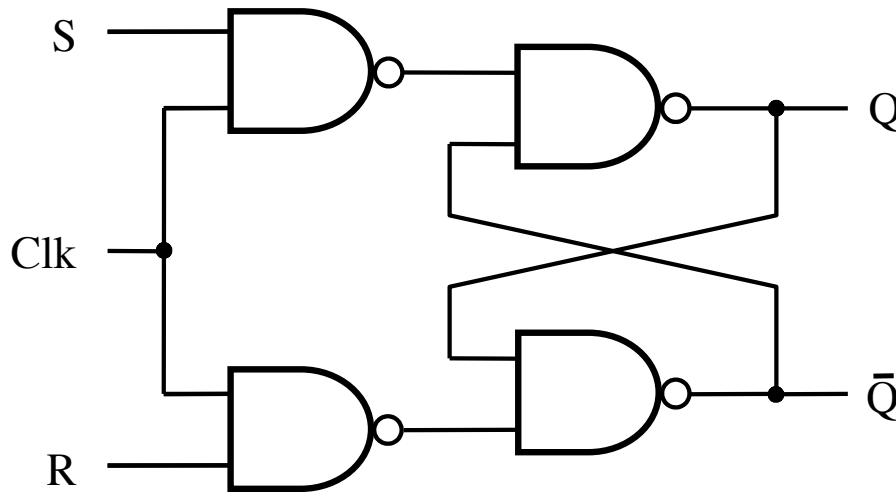
Graphical symbols are the same

# Gated SR latch with NOR gates



Clk	S	R	$Q(t+1)$
0	x	x	$Q(t)$ (no change)
1	0	0	$Q(t)$ (no change)
1	0	1	0
1	1	0	1
1	1	1	x (undesirable)

# Gated SR latch with NAND gates



Clk	S	R	$Q(t+1)$
0	x	x	$Q(t)$ (no change)
1	0	0	$Q(t)$ (no change)
1	0	1	0
1	1	0	1
1	1	1	x (undesirable)

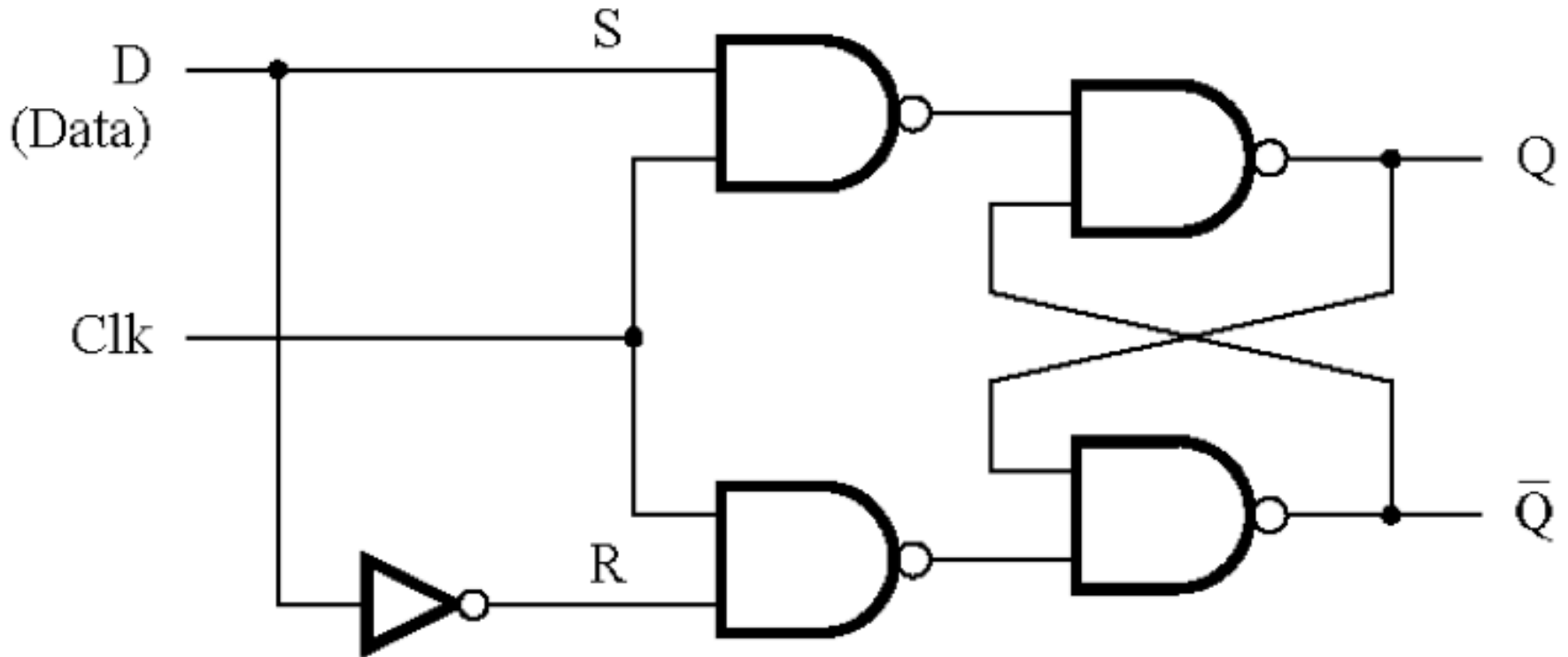
Characteristic tables are the same

# **Gated D Latch**

# Motivation

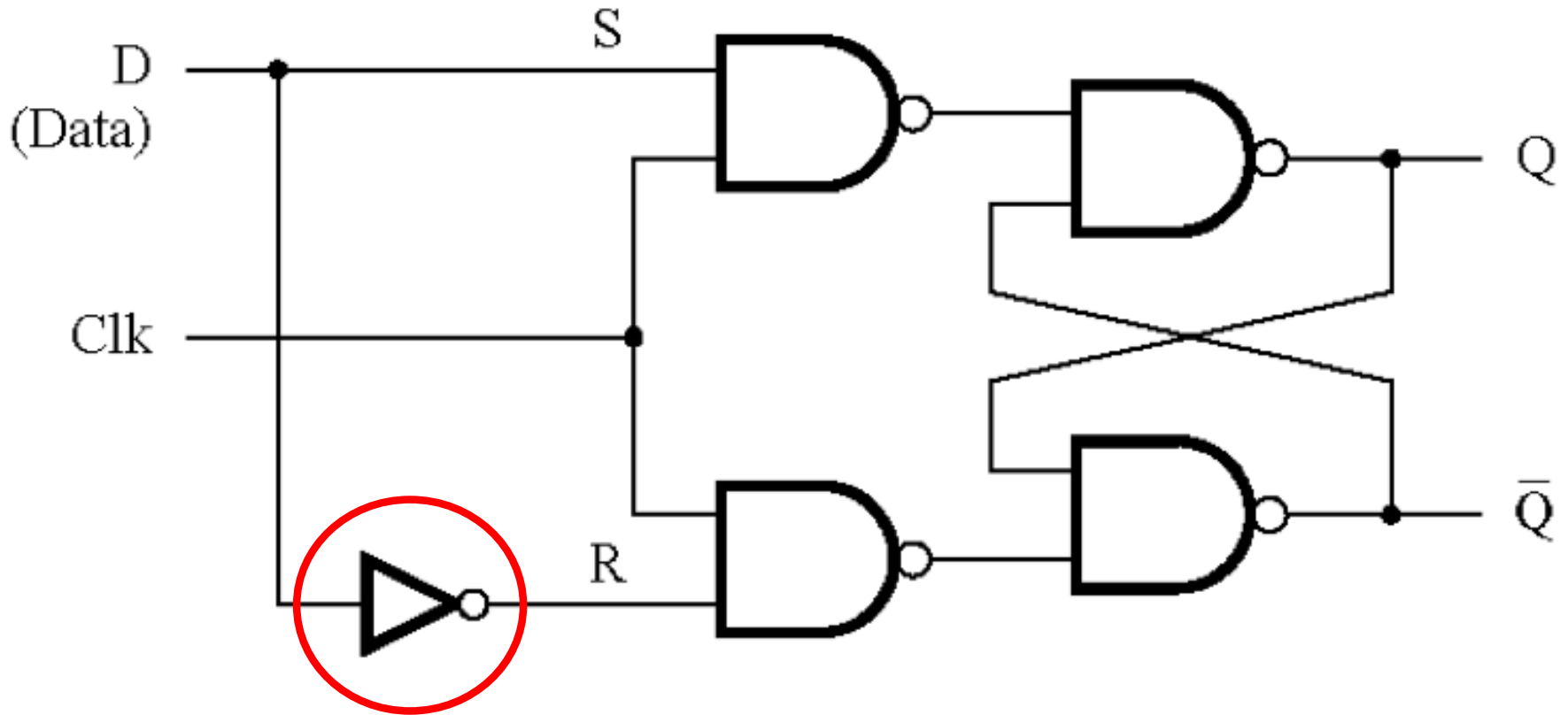
- **Dealing with two inputs (S and R) could be messy. For example, we may have to reset the latch before some operations in order to store a specific value but the reset may not be necessary depending on the current state of the latch.**
- **Why not just have one input and call it D.**
- **The D latch can be constructed using a simple modification of the SR latch.**

# Circuit Diagram for the Gated D Latch



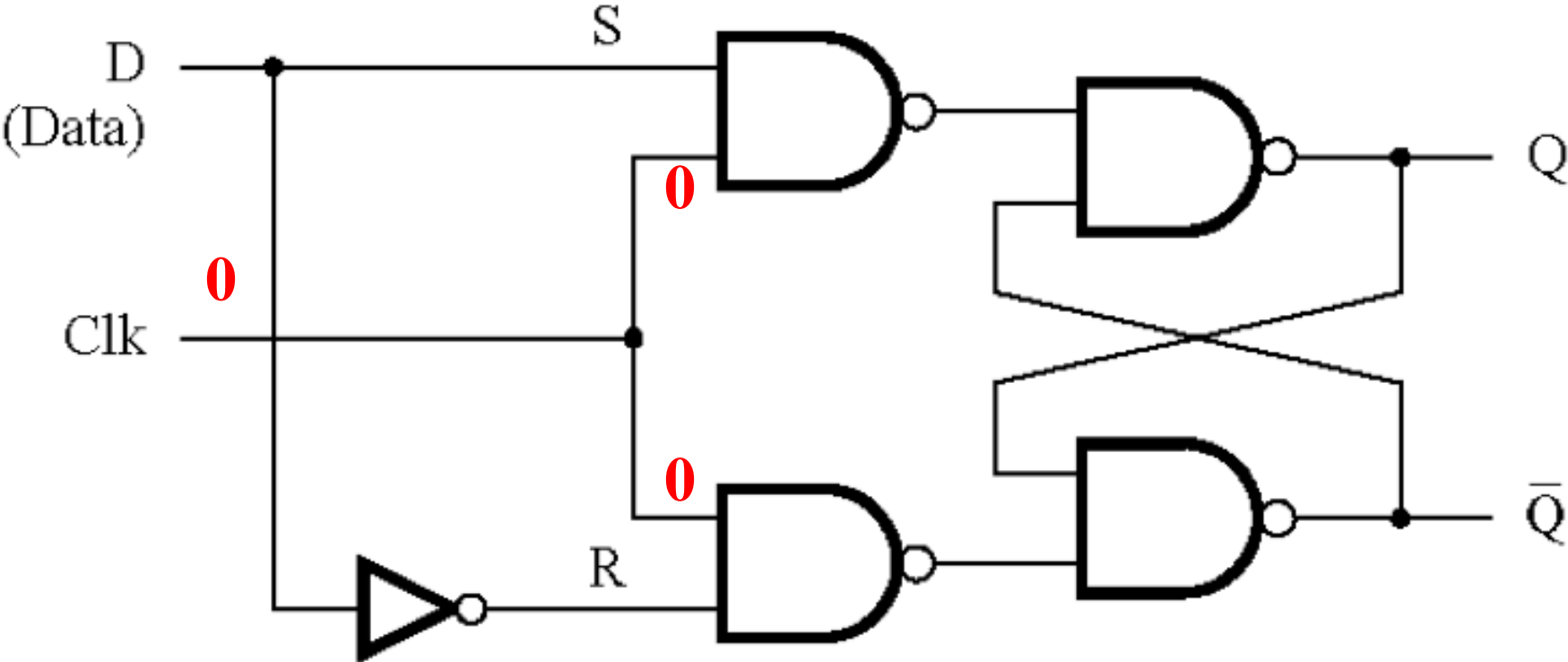
[ Figure 5.7a from the textbook ]

# Circuit Diagram for the Gated D Latch



This is the only  
new thing here.

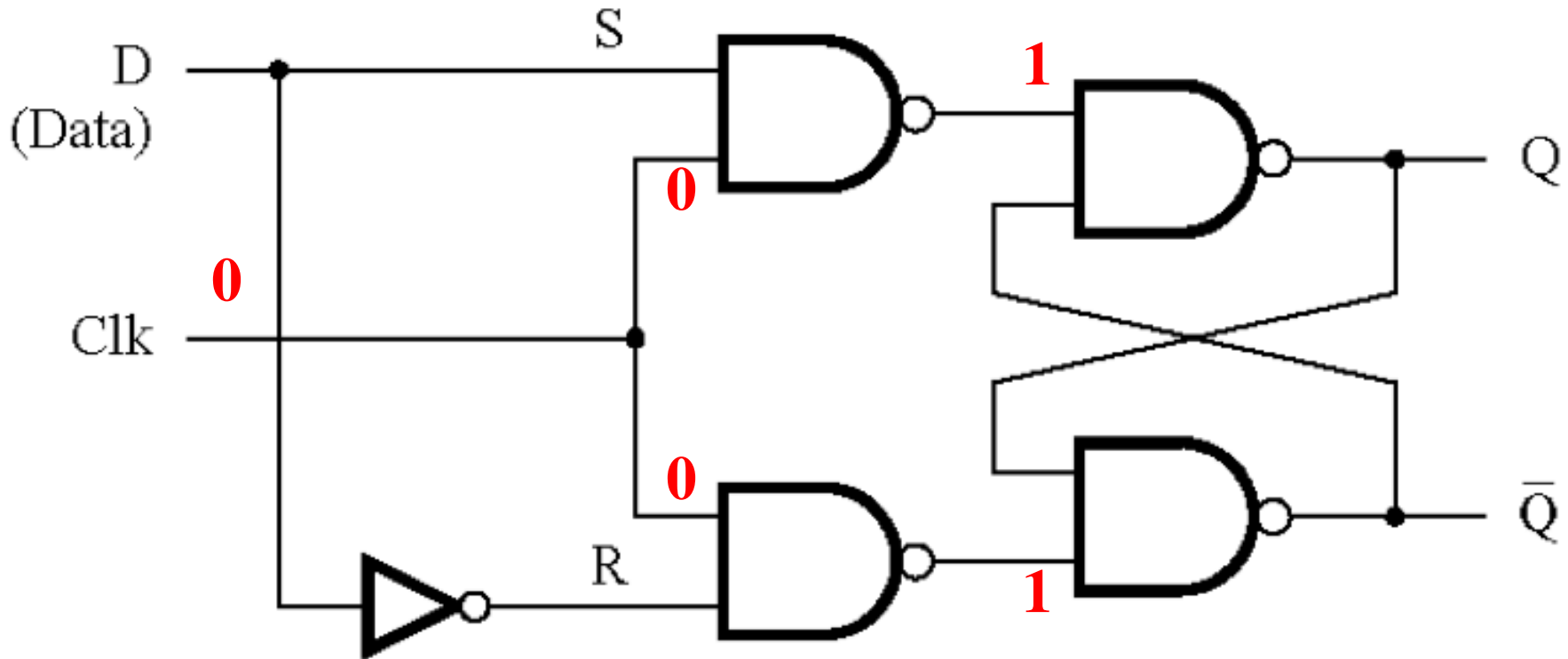
# Circuit Diagram for the Gated D Latch



[ Figure 5.7a from the textbook ]



# Circuit Diagram for the Gated D Latch

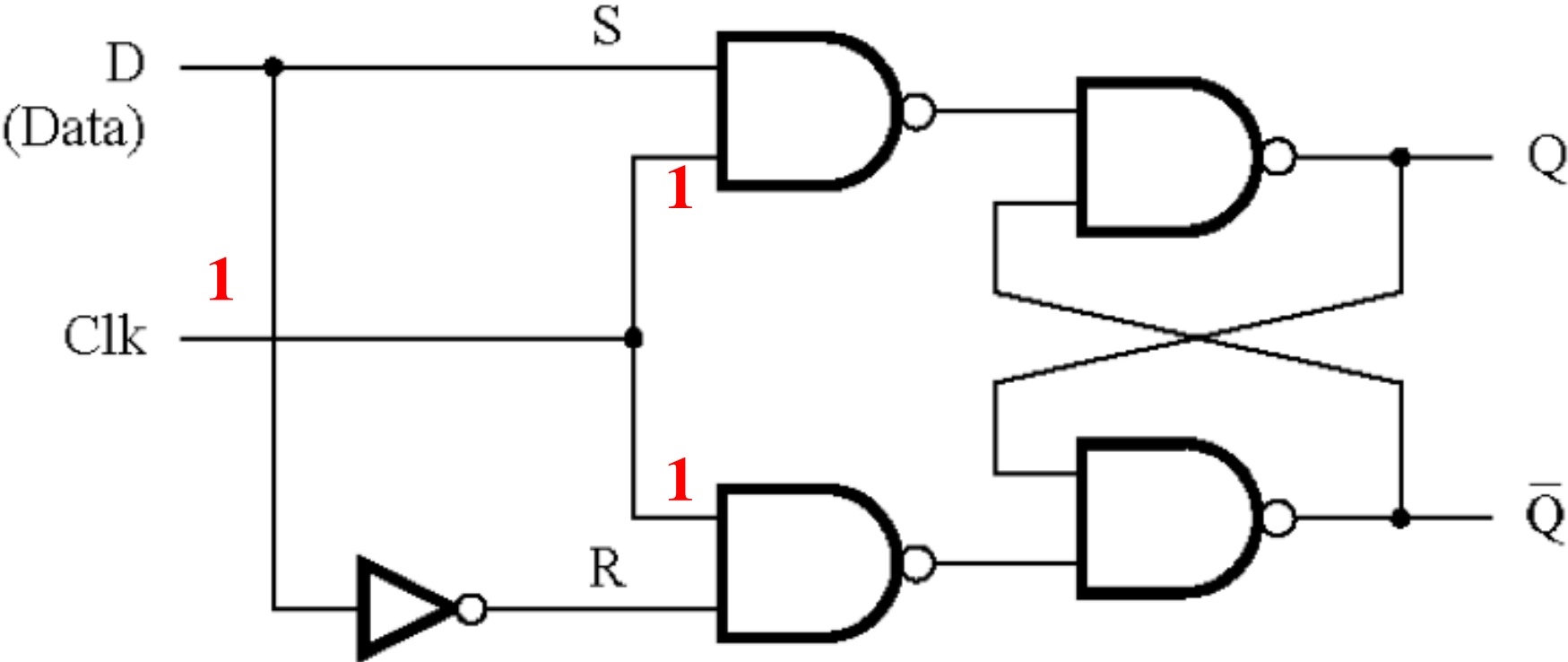


$\bar{S}$	$\bar{R}$	$Q_a$	$Q_b$
0	0	1	1
0	1	1	0
1	0	0	1
1	1	0/1	1/0

(no change)

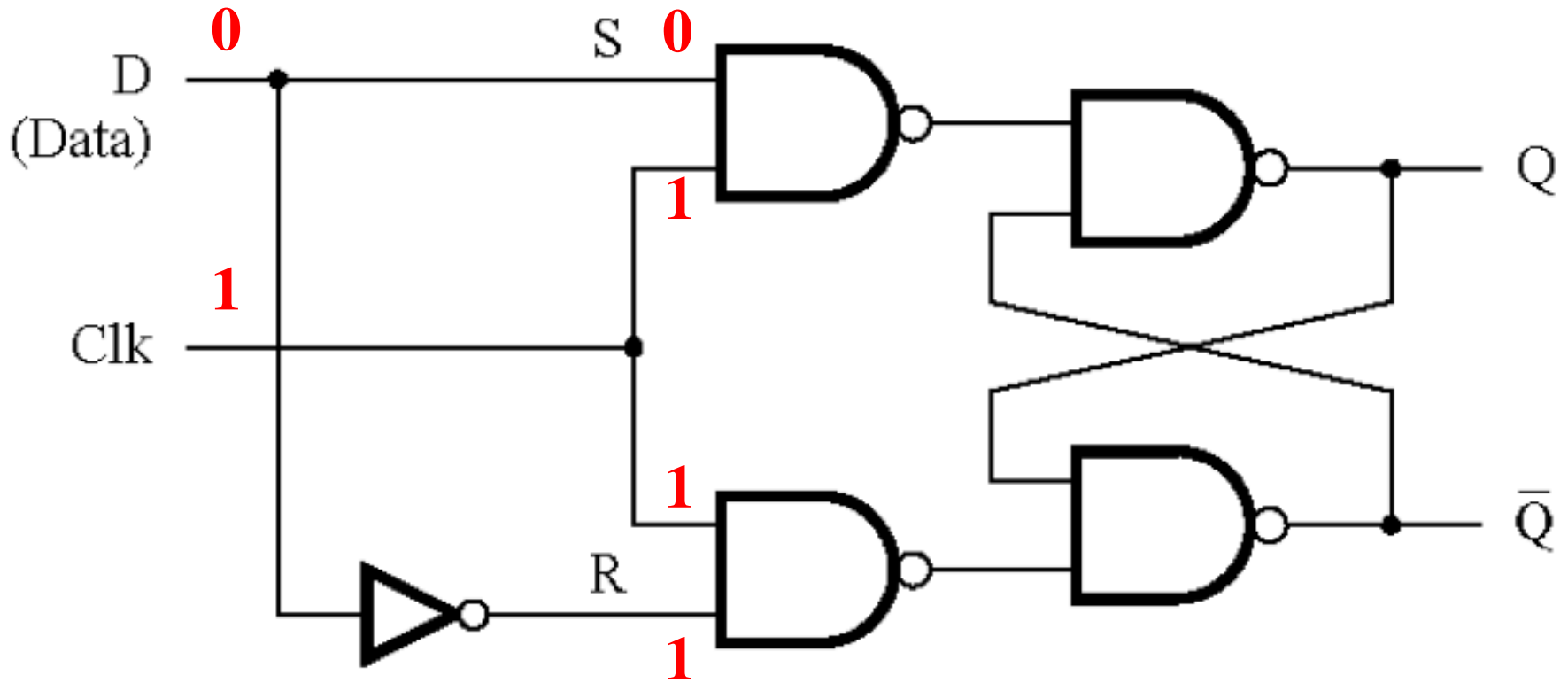
[ Figure 5.7a from the textbook ]

# Circuit Diagram for the Gated D Latch



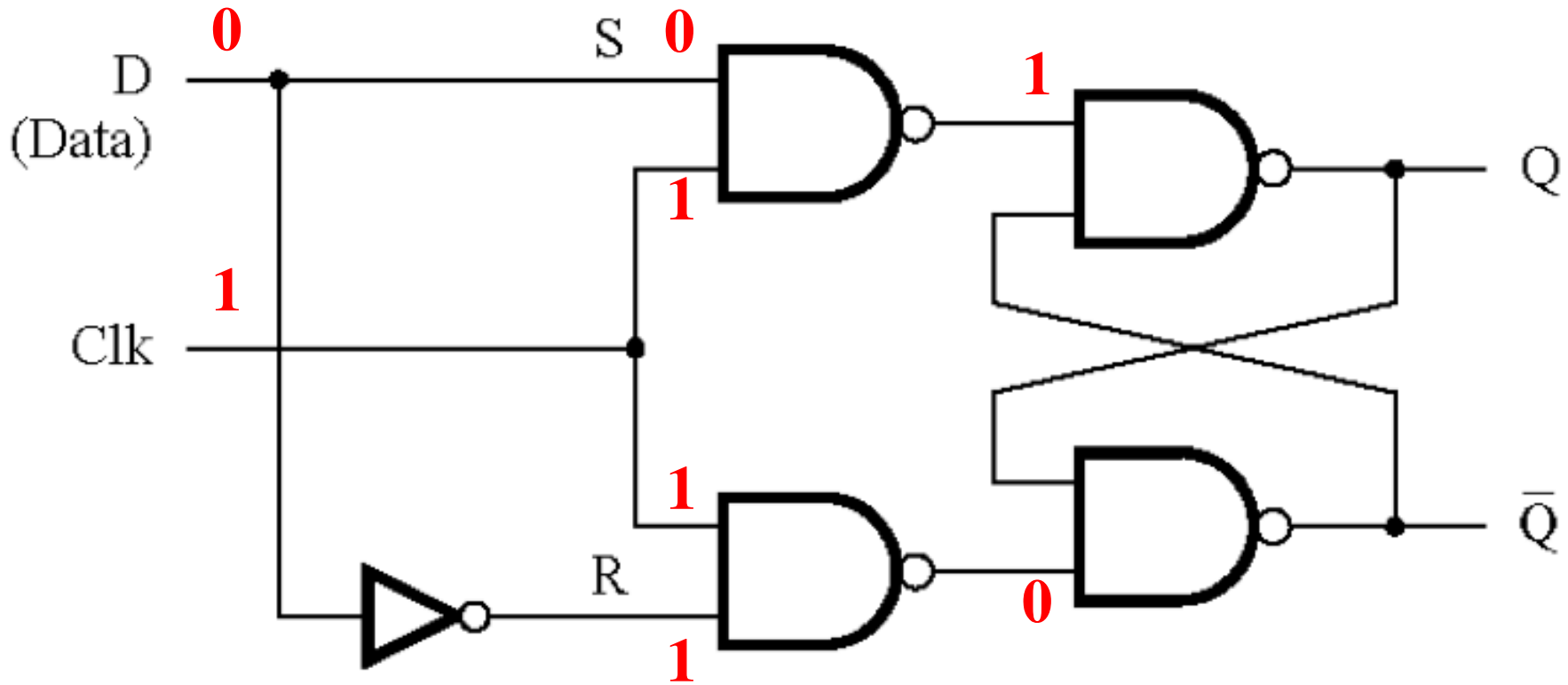
[ Figure 5.7a from the textbook ]

# Circuit Diagram for the Gated D Latch



[ Figure 5.7a from the textbook ]

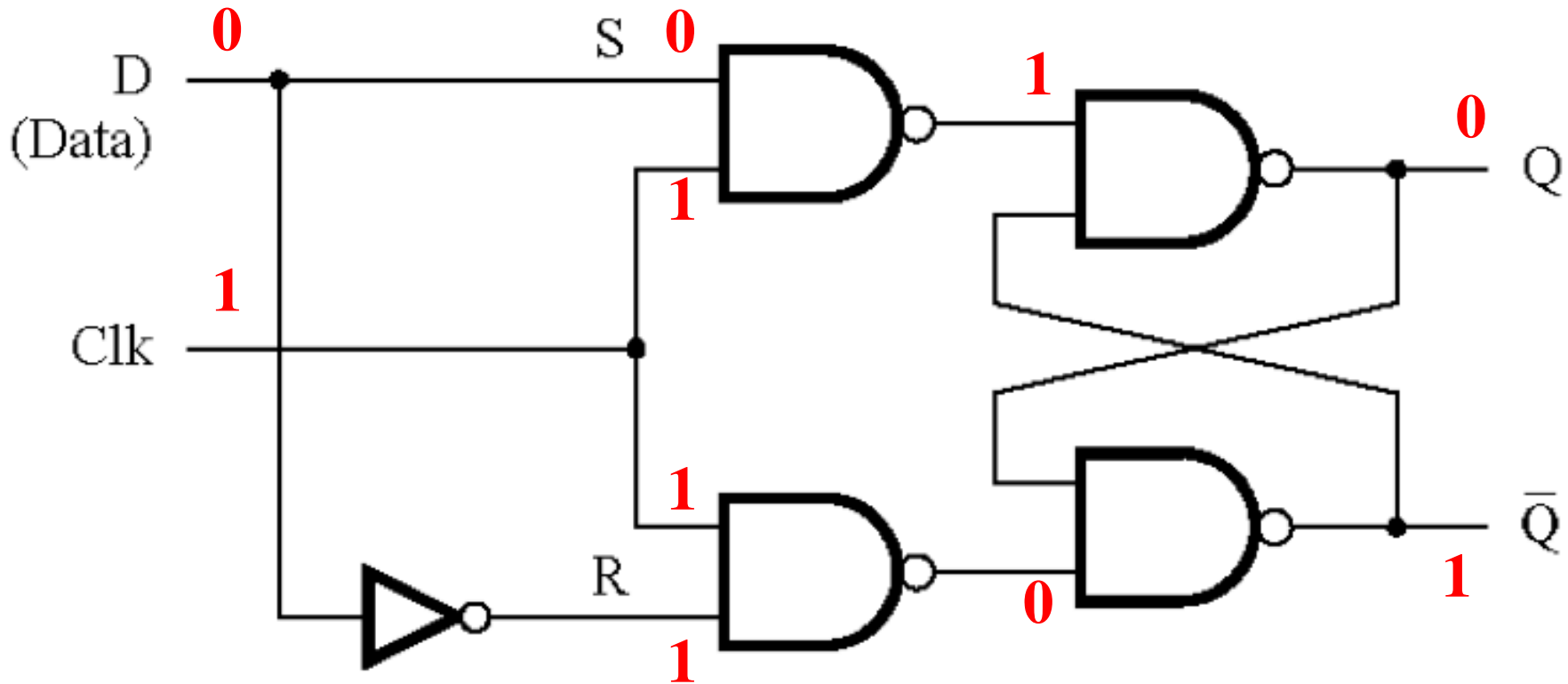
# Circuit Diagram for the Gated D Latch



$\bar{S}$	$\bar{R}$	$Q_a$	$Q_b$
0	0	1	1
0	1	1	0
1	0	0	1
1	1	0/1	1/0 (no change)

[ Figure 5.7a from the textbook ]

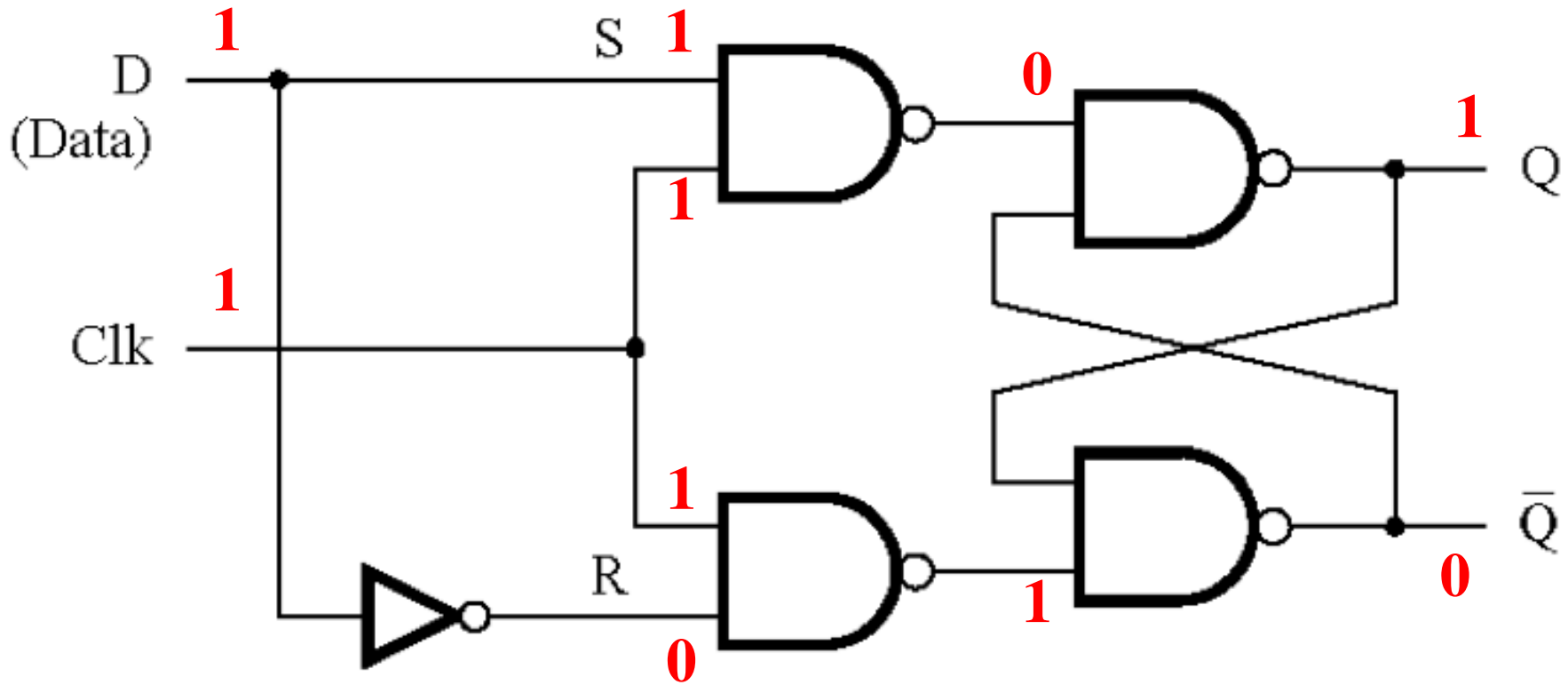
# Circuit Diagram for the Gated D Latch



$\bar{S}$	$\bar{R}$	$Q_a$	$Q_b$
0	0	1	1
0	1	1	0
1	0	0	1
1	1	0/1	1/0 (no change)

[ Figure 5.7a from the textbook ]

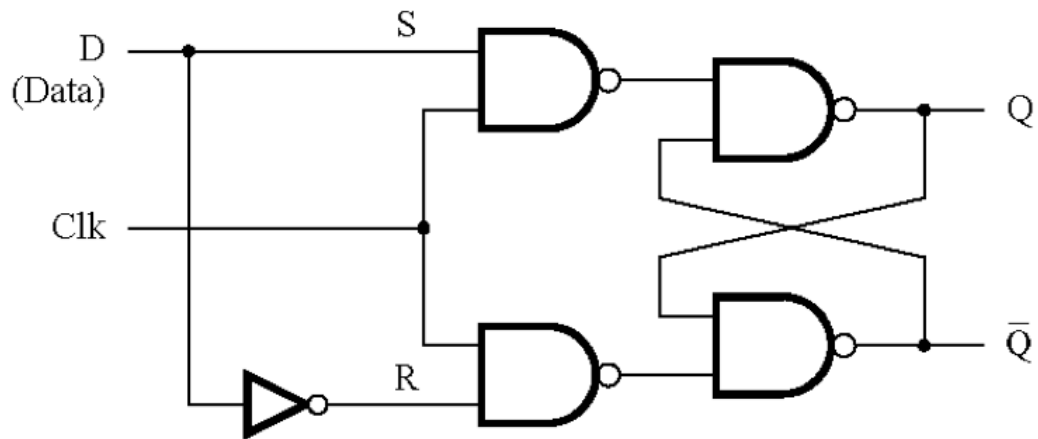
# Circuit Diagram for the Gated D Latch



$\bar{S}$	$\bar{R}$	$Q_a$	$Q_b$
0	0	1	1
0	1	1	0
1	0	0	1
1	1	0/1	1/0 (no change)

[ Figure 5.7a from the textbook ]

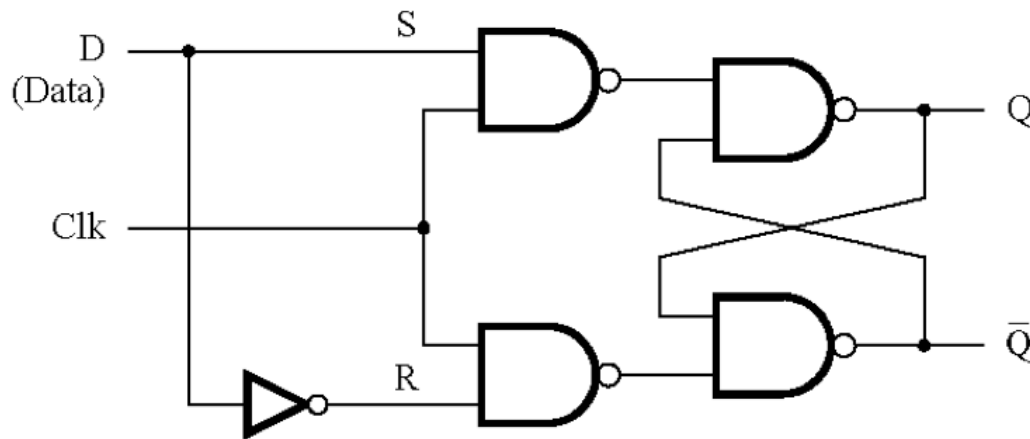
# Circuit Diagram and Characteristic Table for the Gated D Latch



Clk	D	$Q(t+1)$
0	x	$Q(t)$
1	0	0
1	1	1

Note that it is now impossible to have  $S=R=1$ .

# Circuit Diagram and Characteristic Table for the Gated D Latch

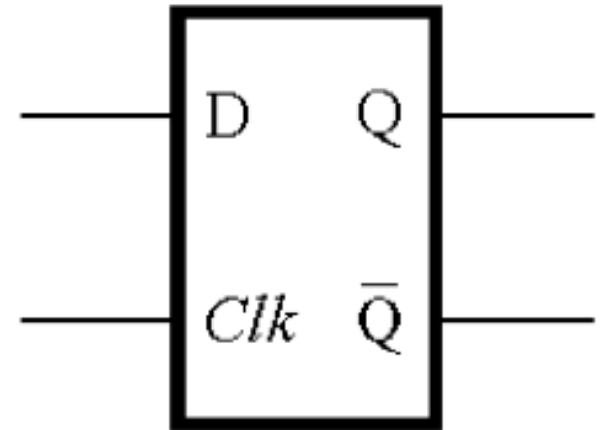
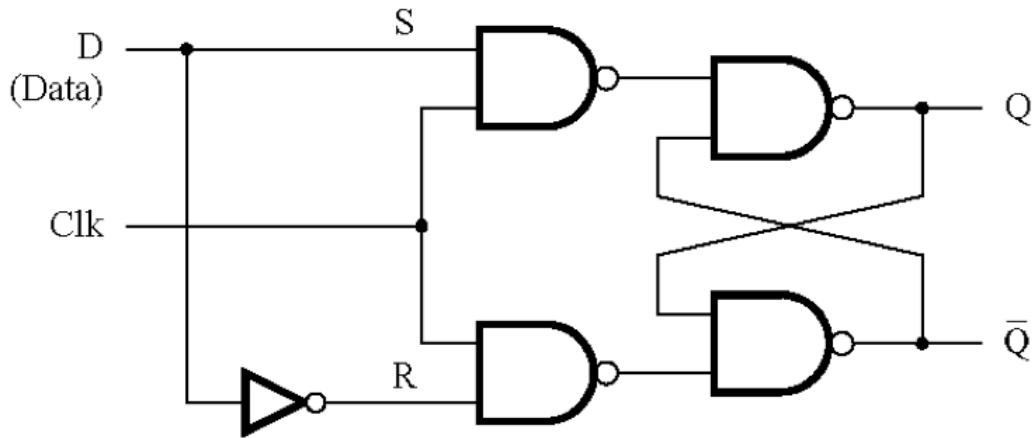


Clk	D	$Q(t+1)$
0	x	$Q(t)$
1	0	0
1	1	1

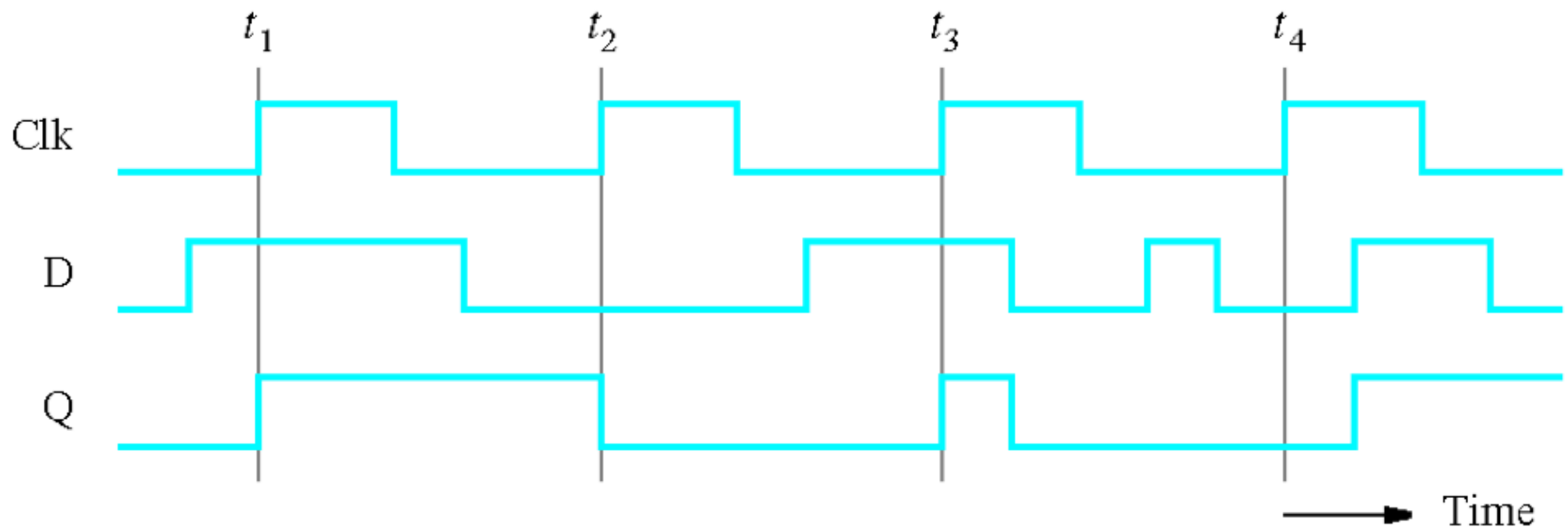
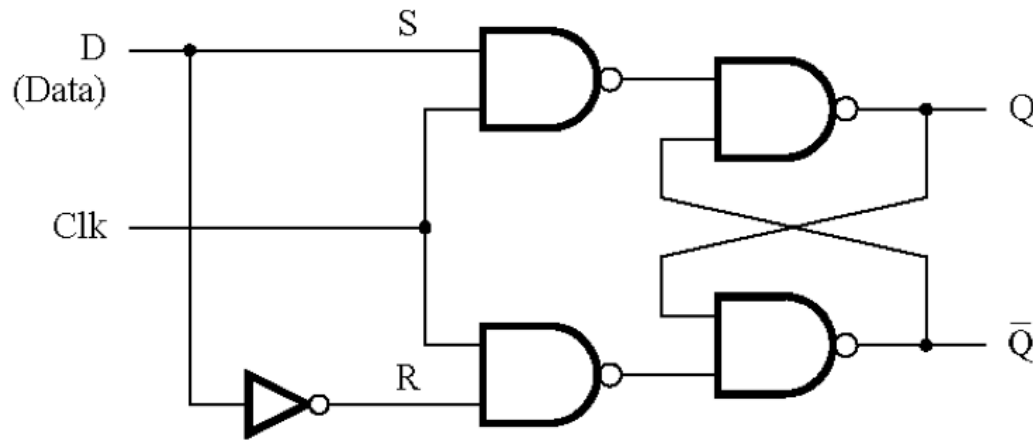
When Clk=1 the output follows the D input.  
When Clk=0 the output cannot be changed.



# Circuit Diagram and Graphical Symbol for the Gated D Latch

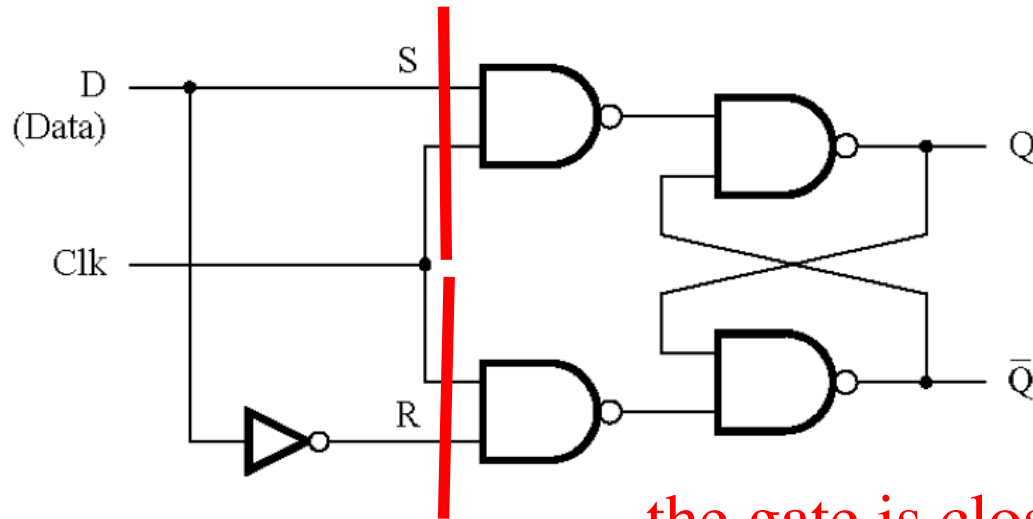


# Timing Diagram for the Gated D Latch



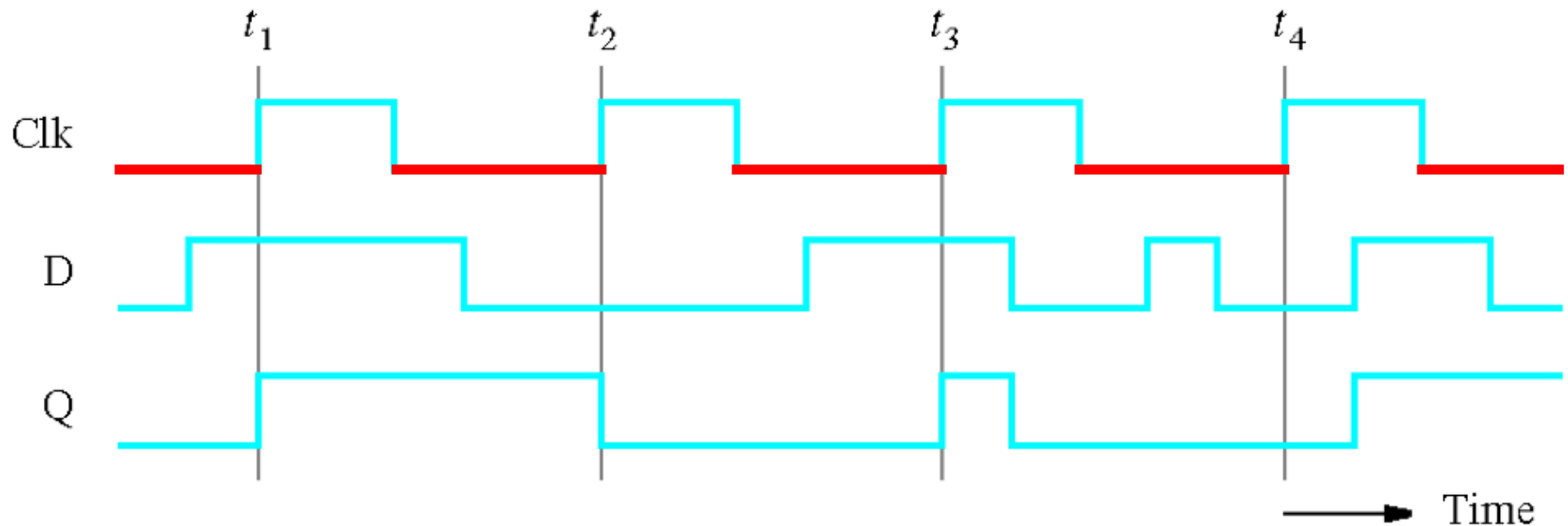
[ Figure 5.7d from the textbook ]

# Timing Diagram for the Gated D Latch



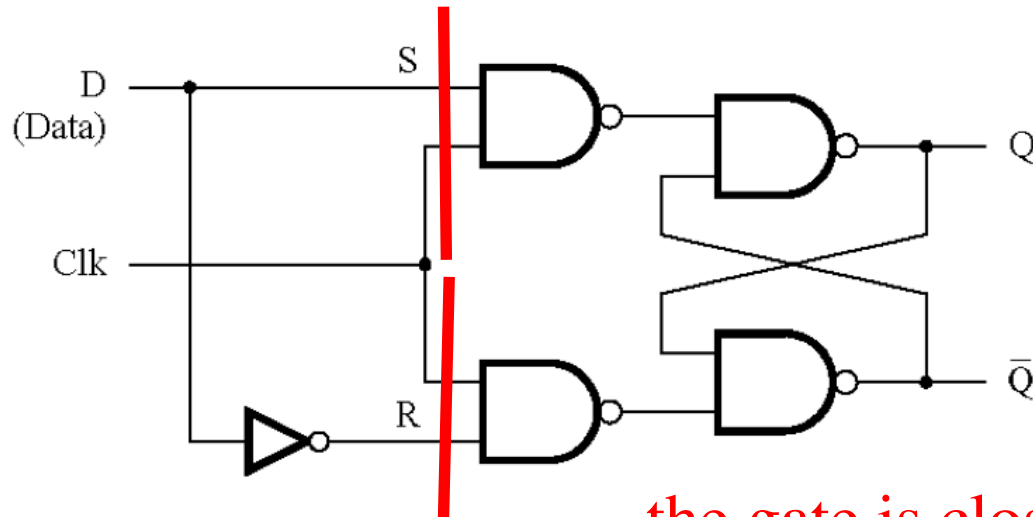
Clk=0

the gate is closed



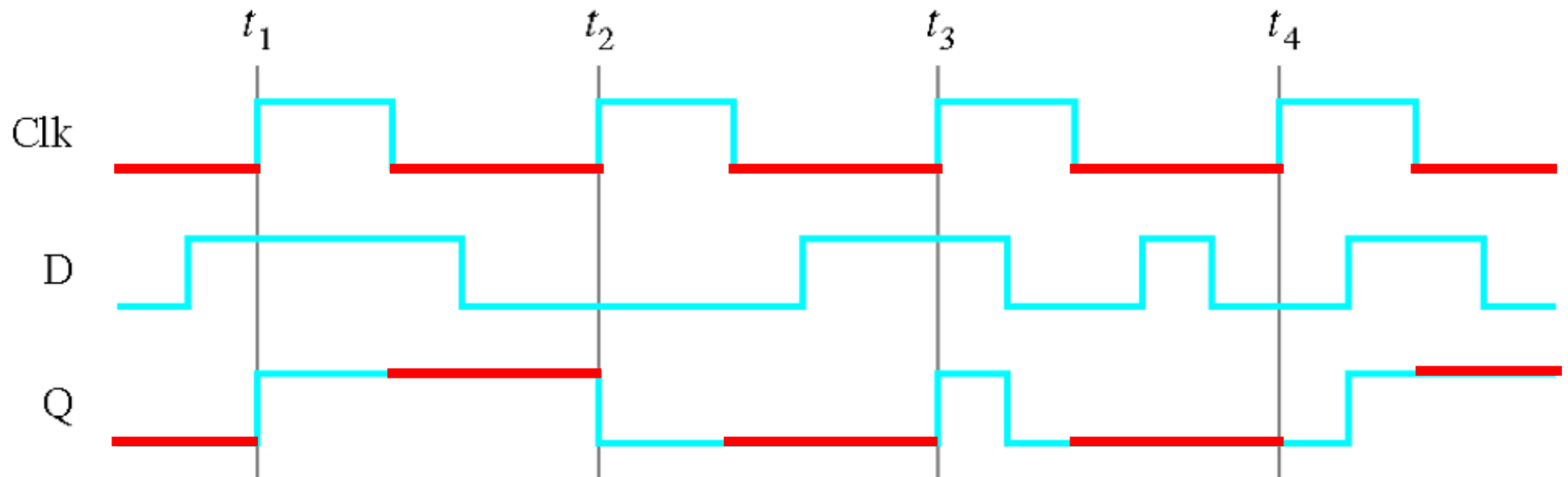
[ Figure 5.7d from the textbook ]

# Timing Diagram for the Gated D Latch



Clk=0

the gate is closed

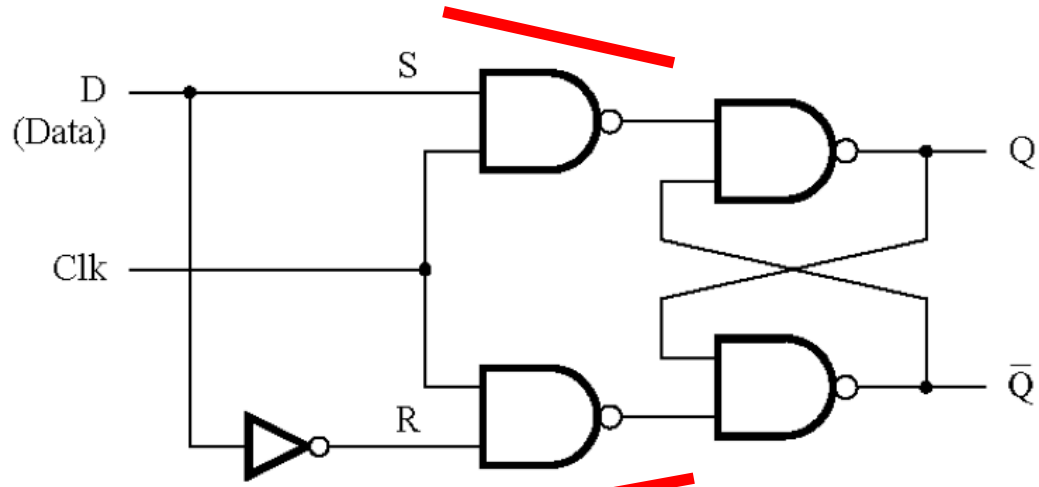


The output Q cannot \*change\* in these intervals.

Time

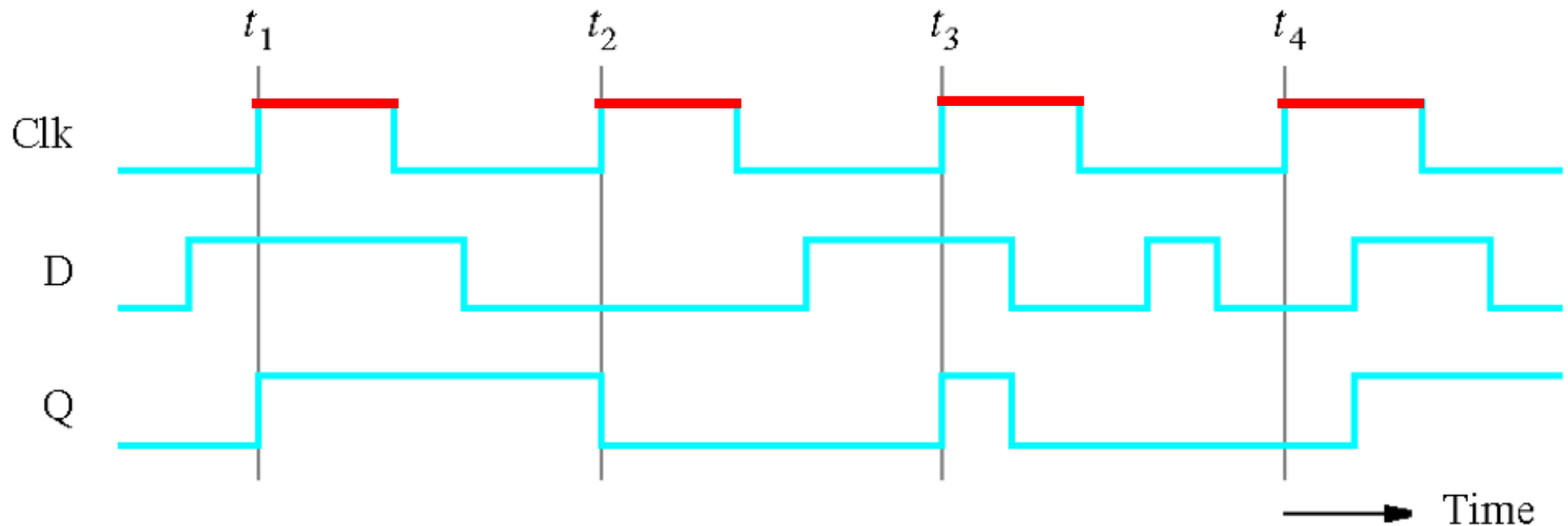
[ Figure 5.7d from the textbook ]

# Timing Diagram for the Gated D Latch



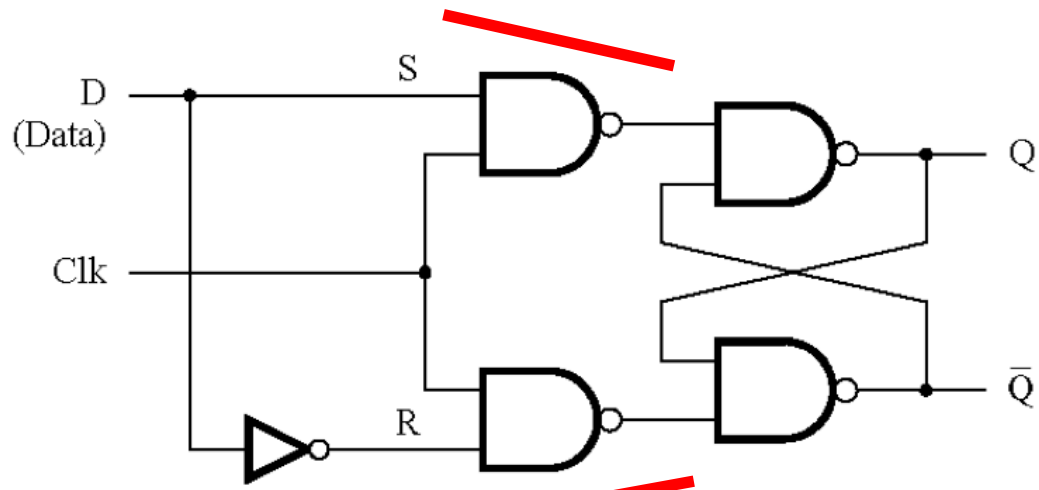
Clk=1

the gate is open



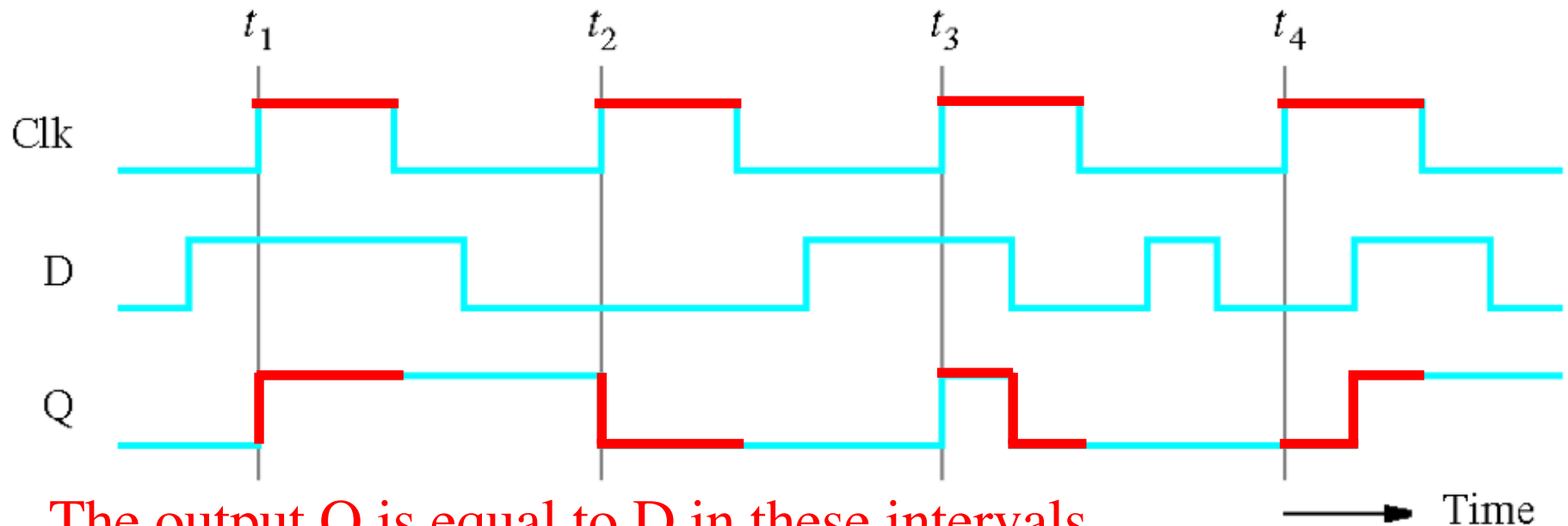
[ Figure 5.7d from the textbook ]

# Timing Diagram for the Gated D Latch



Clk=1

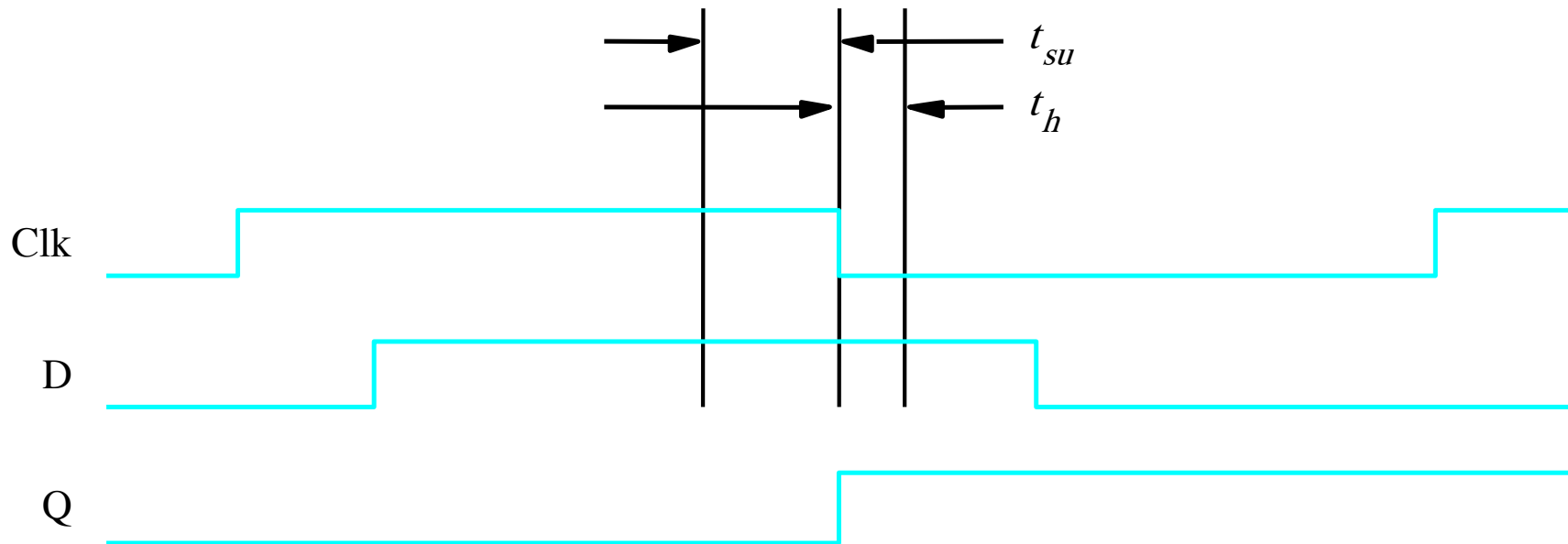
the gate is open



The output Q is equal to D in these intervals.

[ Figure 5.7d from the textbook ]

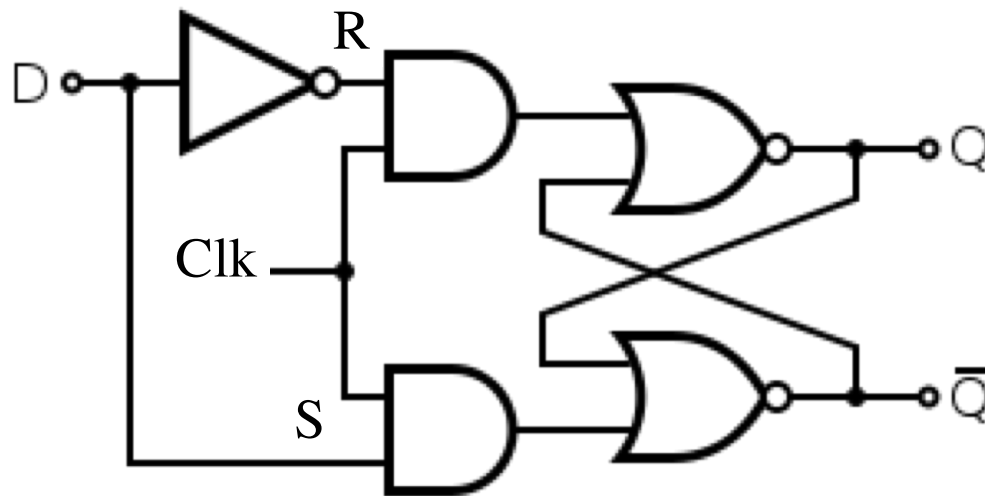
# Setup and hold times



Setup time ( $t_{su}$ ) – the minimum time that the D signal must be stable prior to the the negative edge of the Clock signal.

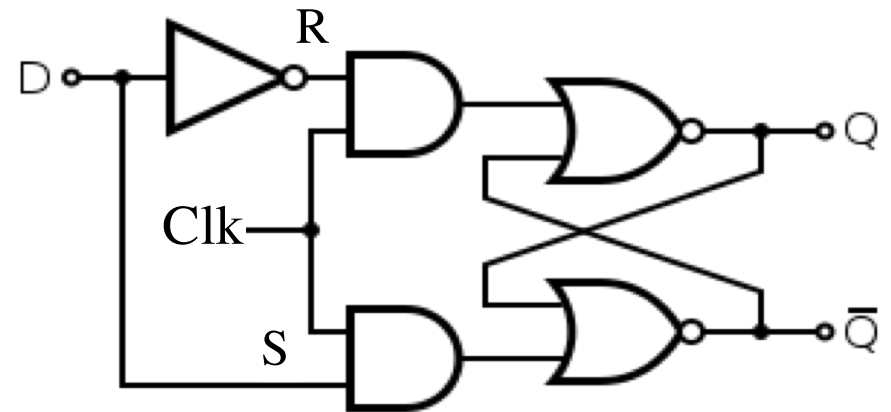
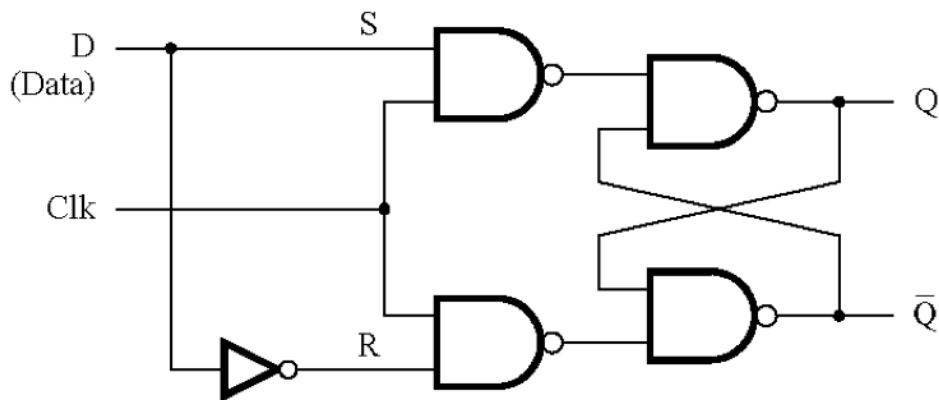
Hold time ( $t_h$ ) – the minimum time that the D signal must remain stable after the the negative edge of the Clock signal.

# Circuit Diagram for the Gated D Latch (with the latch implemented using NORs)



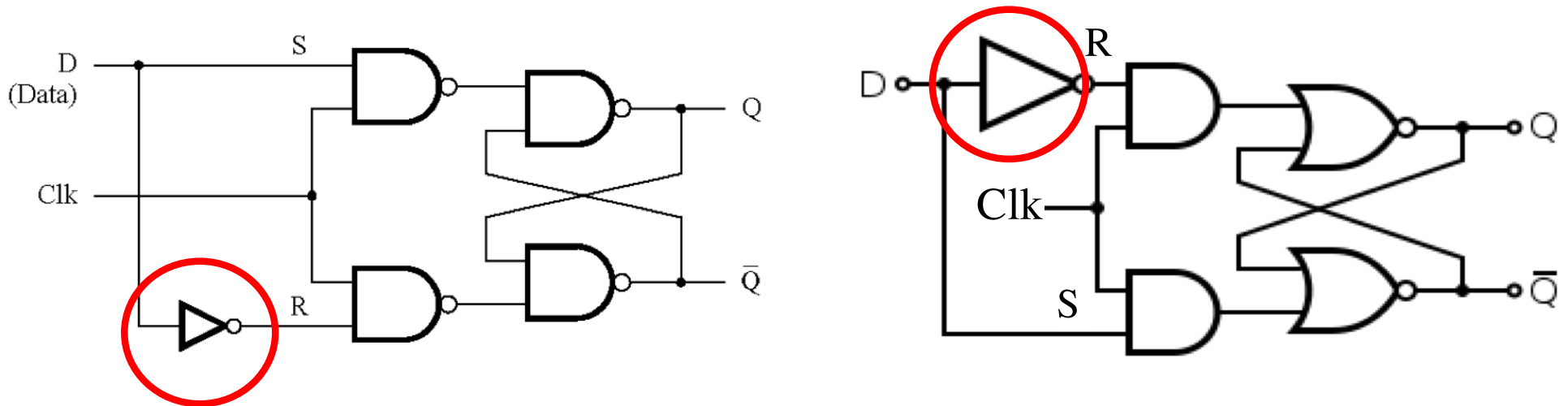


# Circuit Diagram for the Gated D Latch (with the latch implemented using NORs)



[ Figure 5.7a from the textbook ]

# Circuit Diagram for the Gated D Latch (with the latch implemented using NORs)

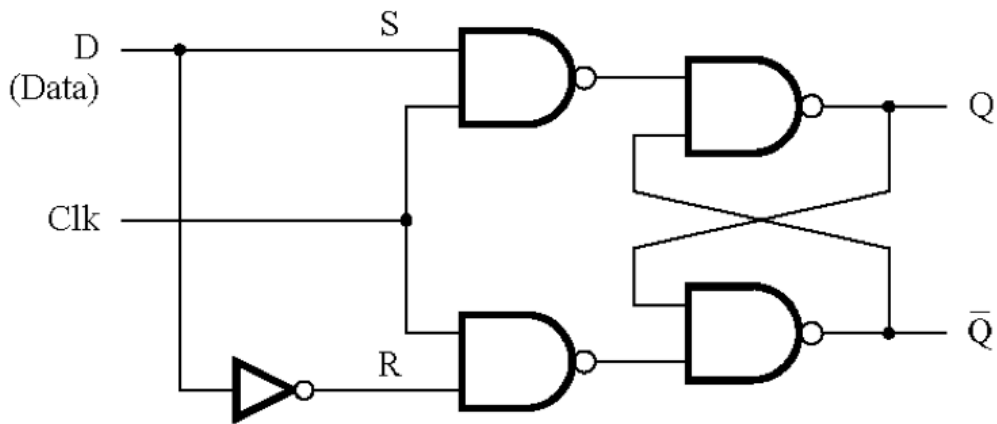


The NOT gate is now in a different place.  
Also, S and R are swapped.

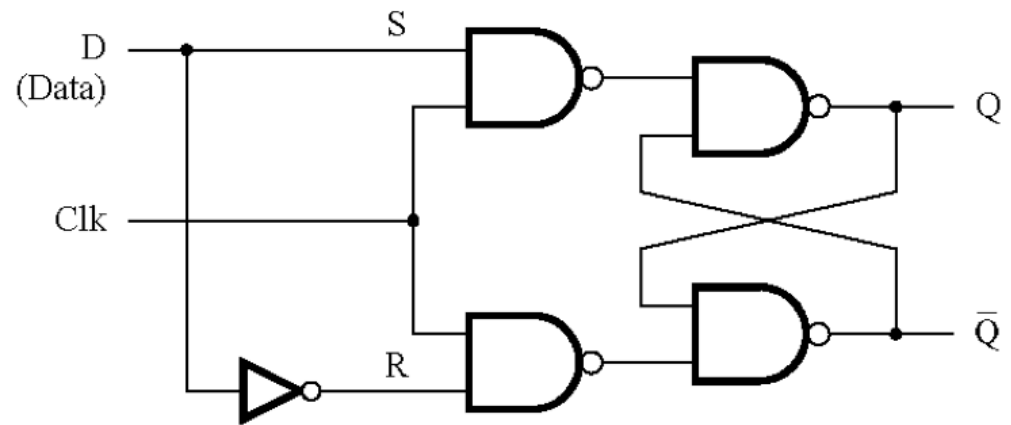
# Master-Slave D Flip-Flop

# Constructing a Master-Slave D Flip-Flop From Two D Latches

Master



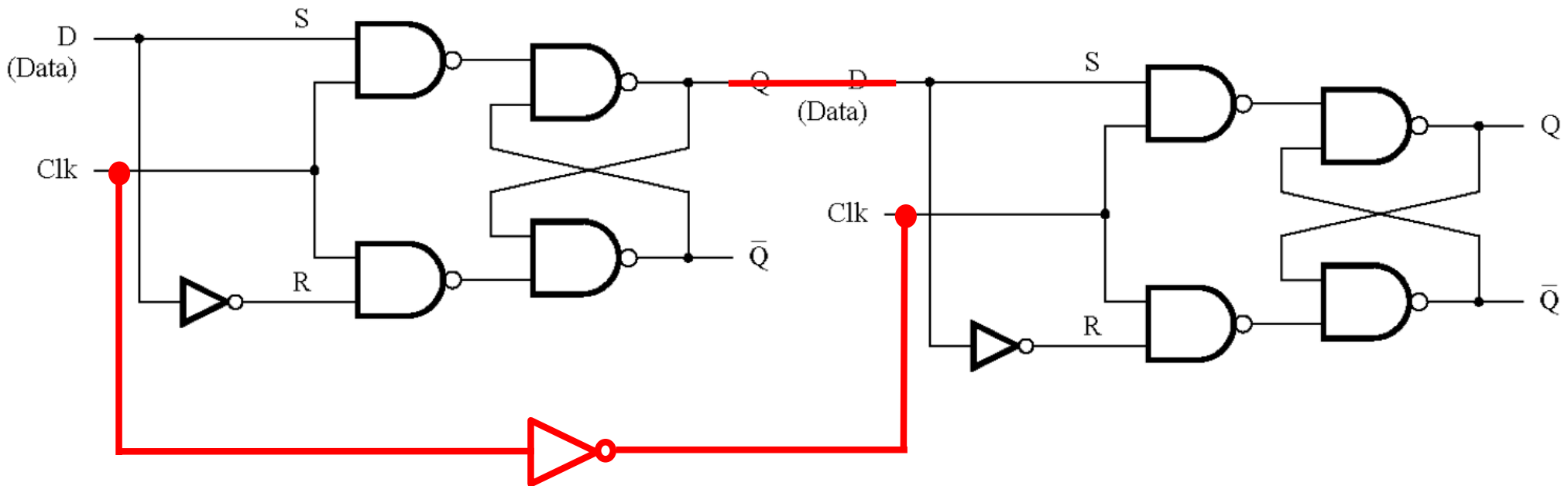
Slave



# Constructing a Master-Slave D Flip-Flop From Two D Latches

Master

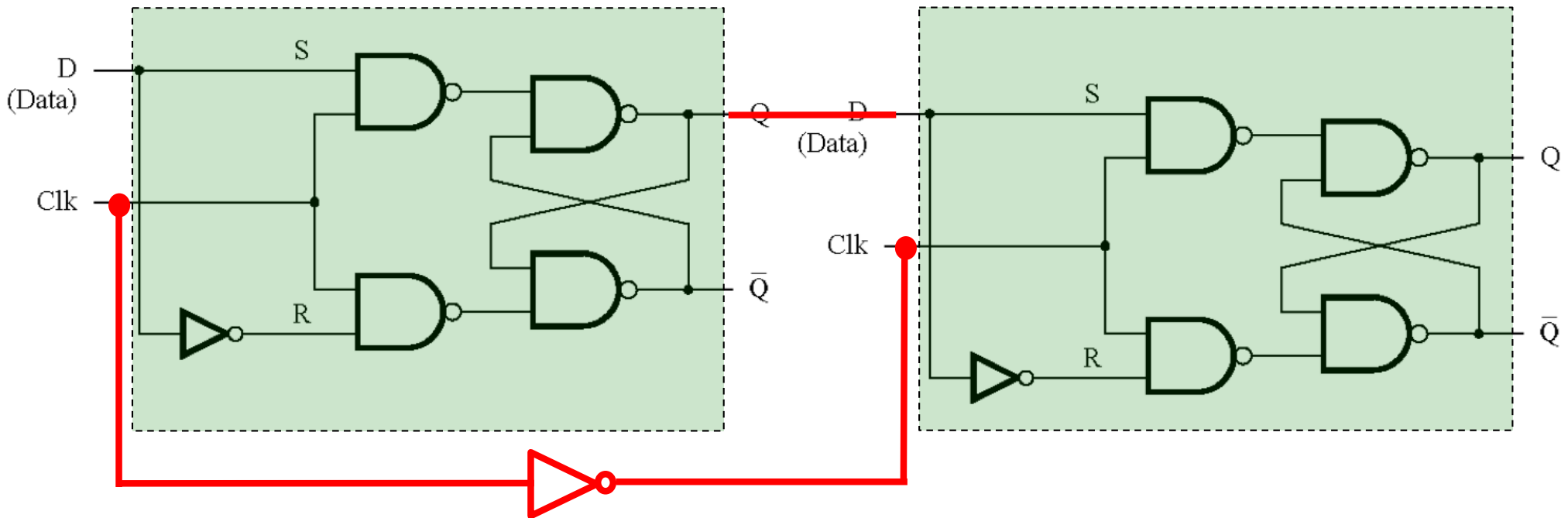
Slave



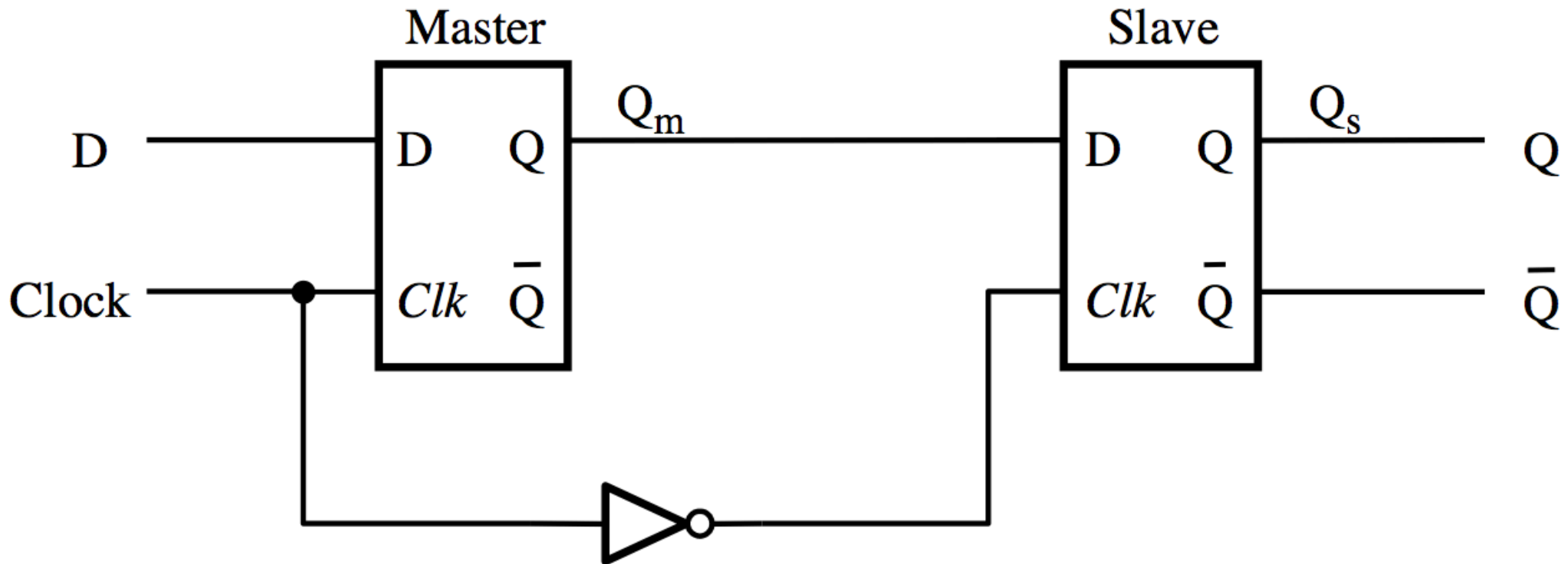
# Constructing a Master-Slave D Flip-Flop From Two D Latches

Master

Slave

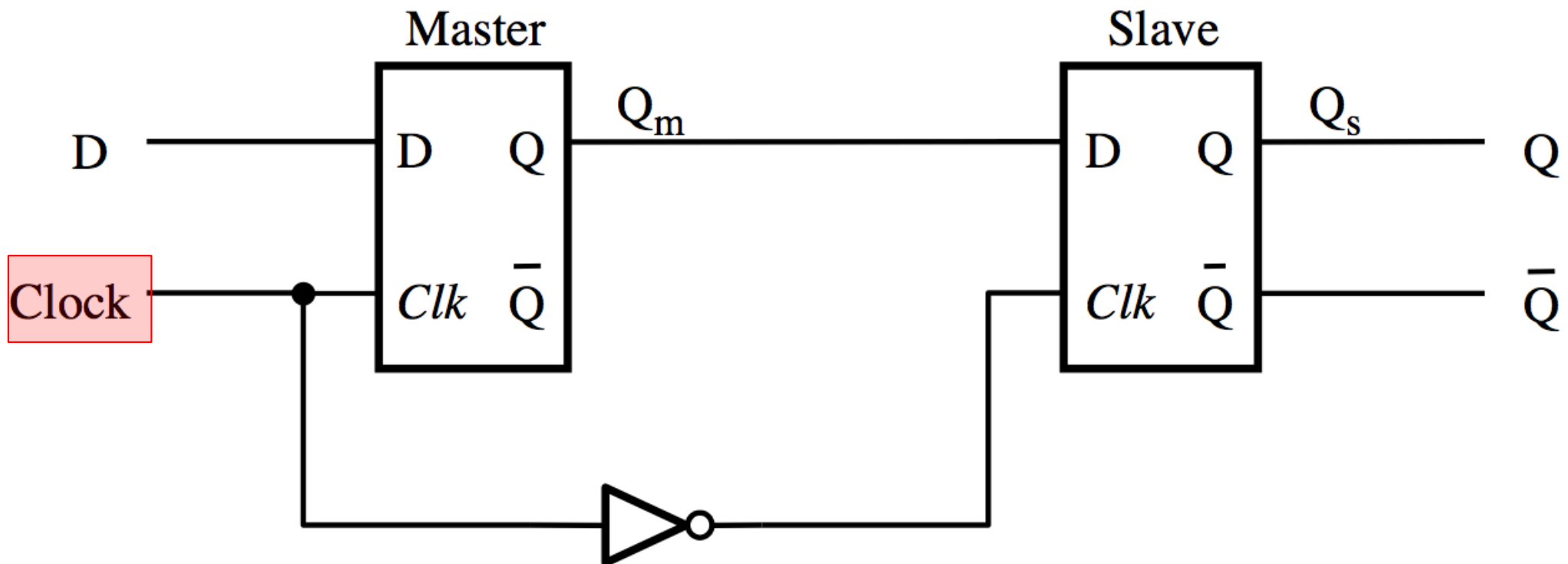


# Constructing a Master-Slave D Flip-Flop From Two D Latches



[ Figure 5.9a from the textbook ]

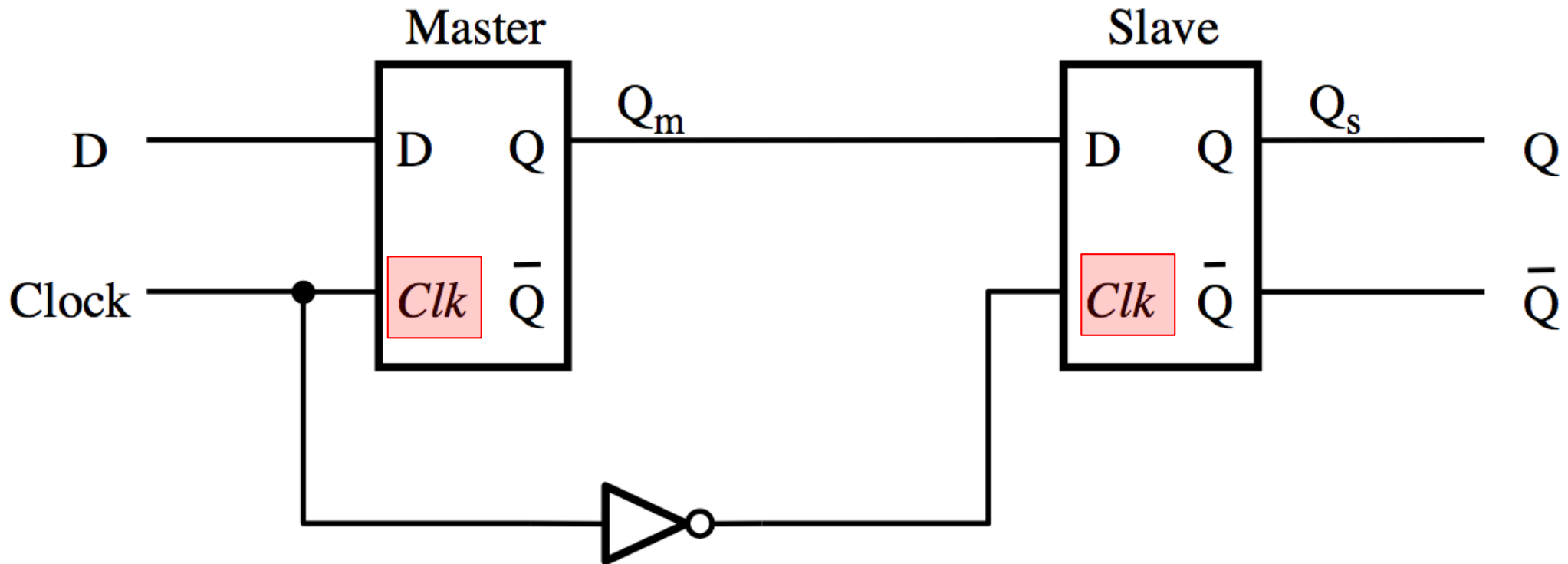
# Clock is used for the D Flip-Flop



[ Figure 5.9a from the textbook ]



# Clock is used for the D Flip-Flop, but Clk is used for each D Latch

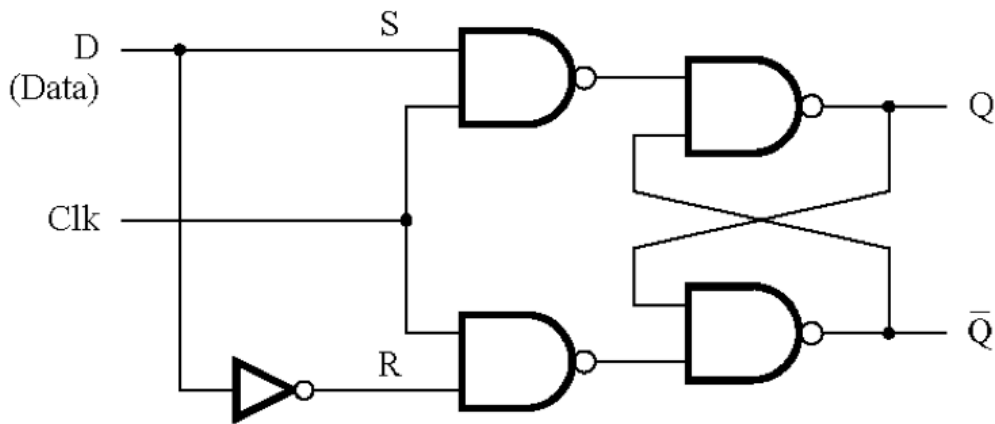


[ Figure 5.9a from the textbook ]

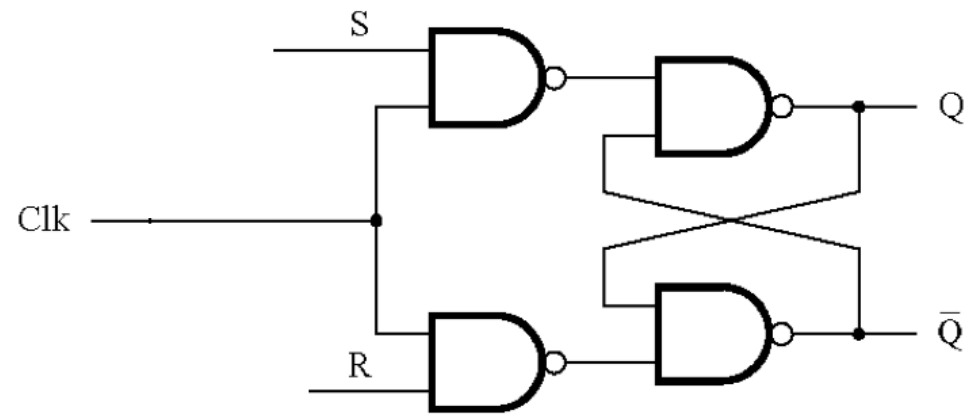
# Constructing a Master-Slave D Flip-Flop From one D Latch and one Gated SR Latch

(This version uses one less NOT gate)

Master



Slave

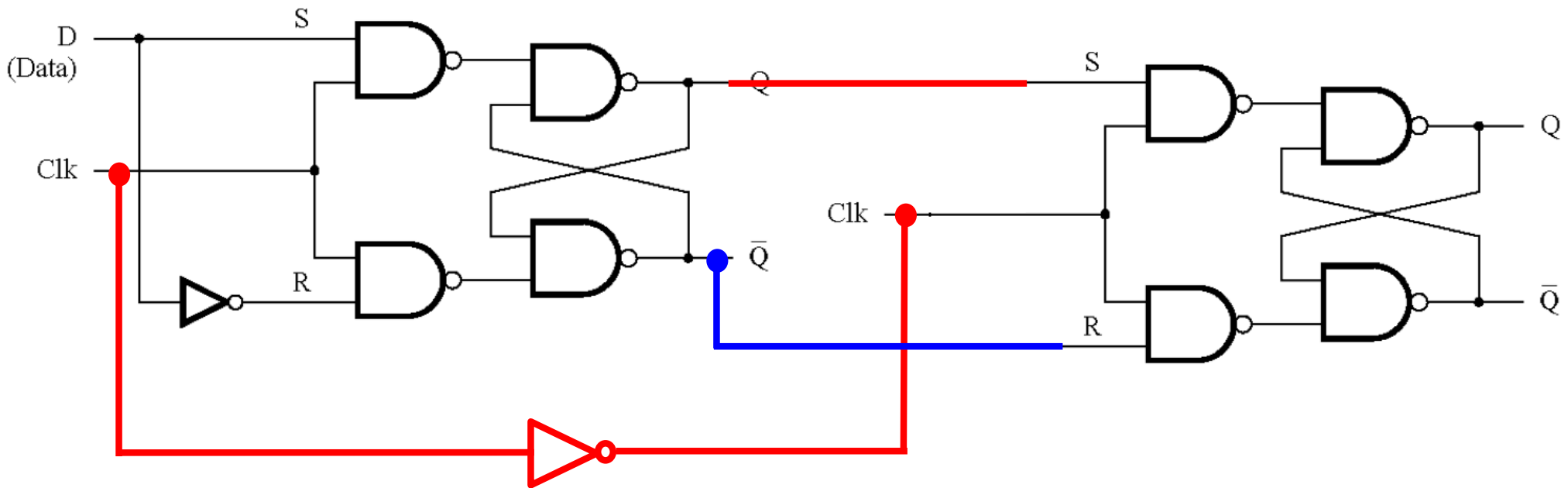


# Constructing a Master-Slave D Flip-Flop From one D Latch and one Gated SR Latch

(This version uses one less NOT gate)

Master

Slave

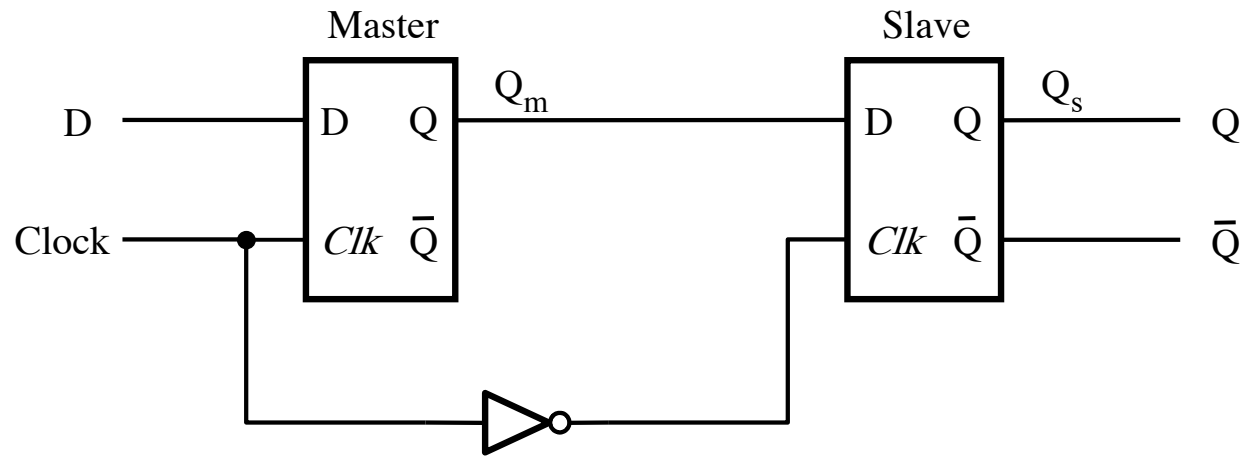


# Edge-Triggered D Flip-Flops

# Motivation

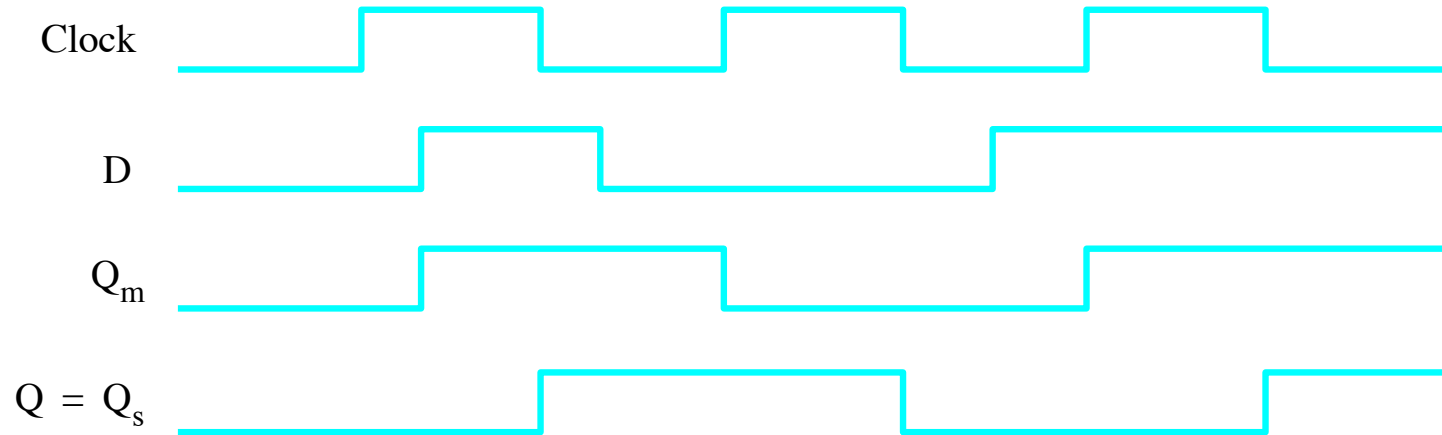
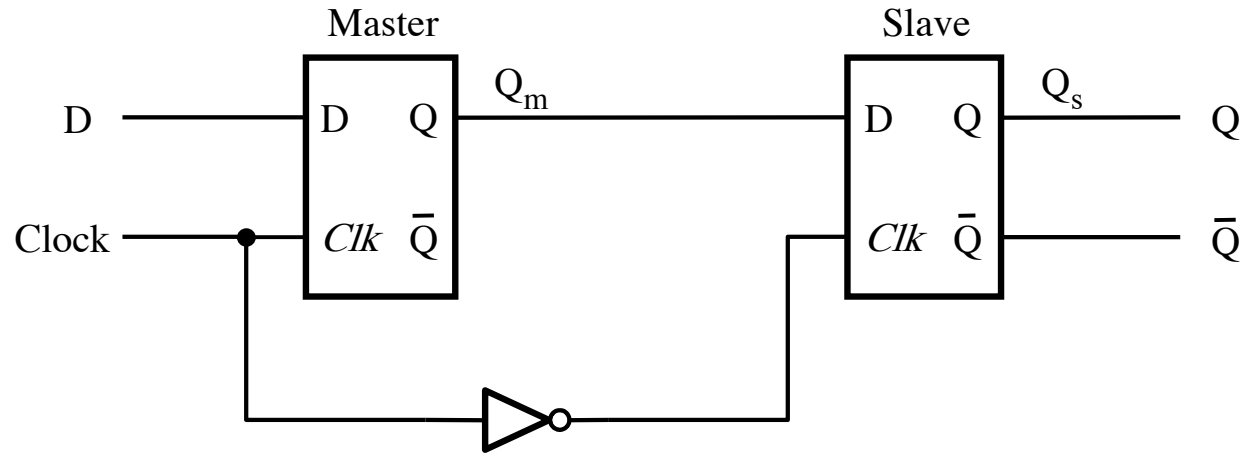
**In some cases we need to use a memory storage device that can change its state no more than once during each clock cycle.**

# Master-Slave D Flip-Flop



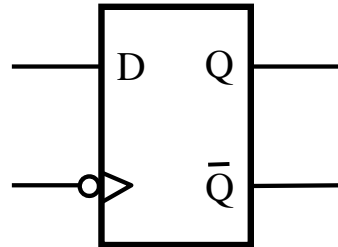
(a) Circuit

# Timing Diagram for the Master-Slave D Flip-Flop



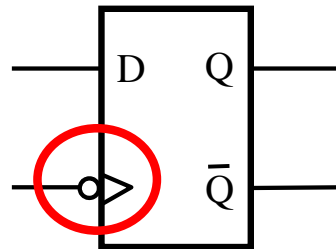
[ Figure 5.9a,b from the textbook ]

# Graphical Symbol for the Master-Slave D Flip-Flop





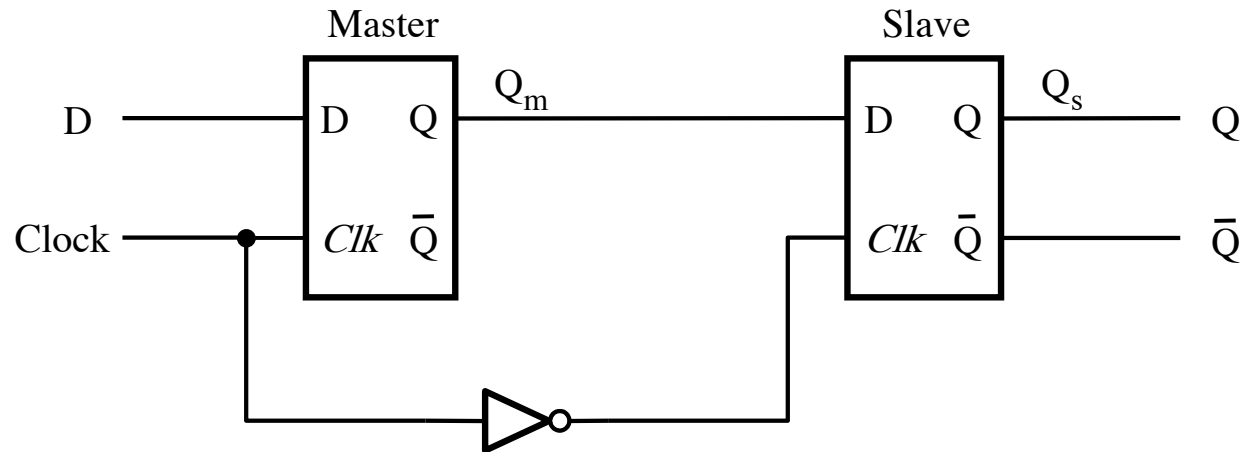
# Graphical Symbol for the Master-Slave D Flip-Flop



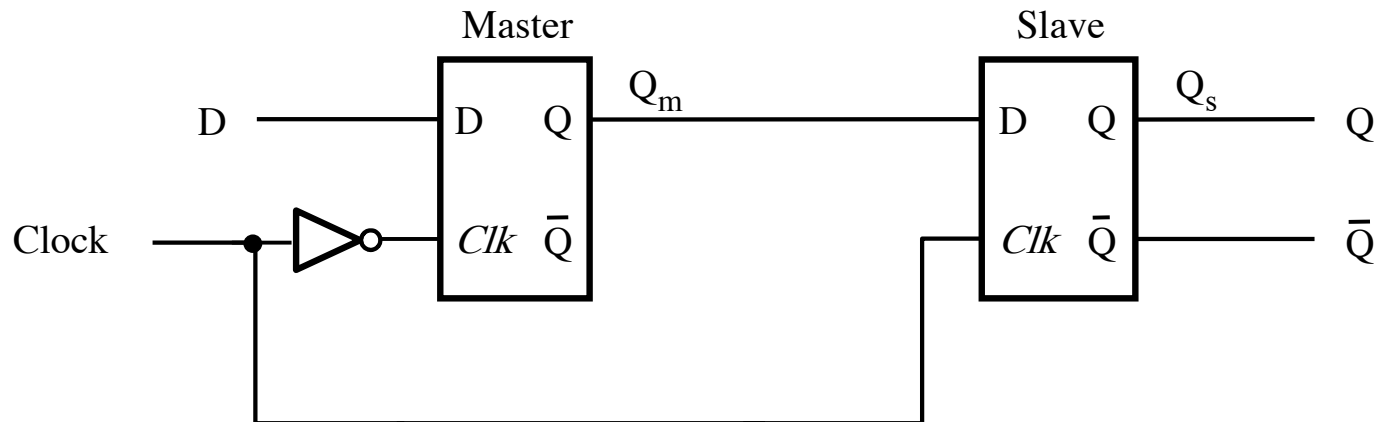
The  $>$  means that this is edge-triggered

The small circle means that it is the negative edge

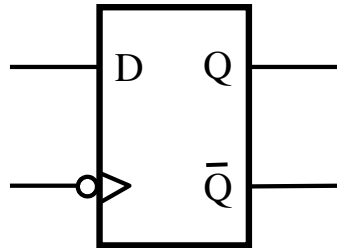
# Negative-Edge-Triggered Master-Slave D Flip-Flop



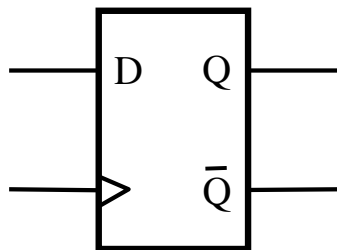
# Positive-Edge-Triggered Master-Slave D Flip-Flop



# Negative-Edge-Triggered Master-Slave D Flip-Flop

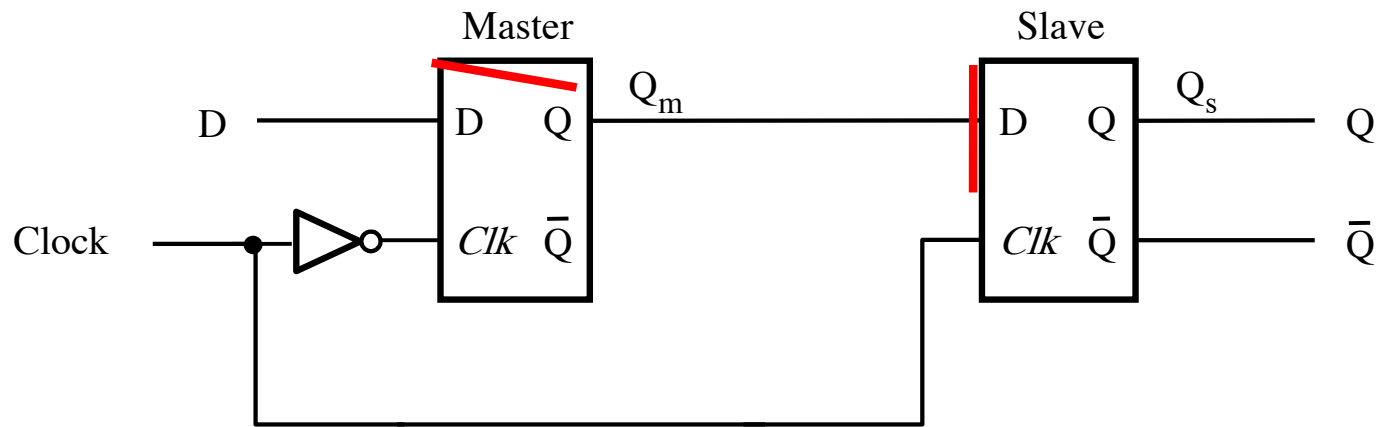


# Positive-Edge-Triggered Master-Slave D Flip-Flop

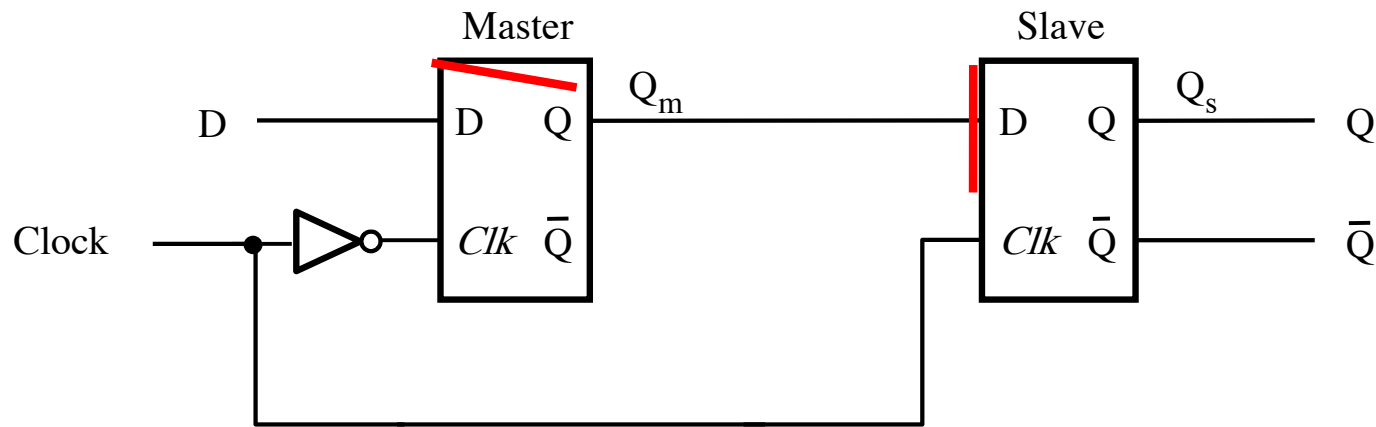


# **D Flip-Flop: A Double Door Analogy**

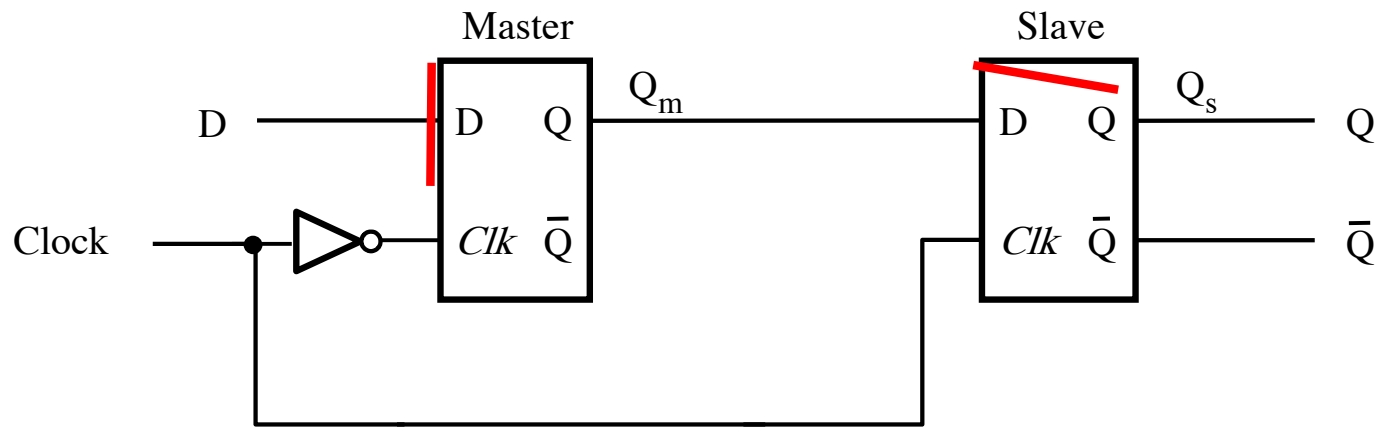
# Positive-Edge-Triggered Master-Slave D Flip-Flop



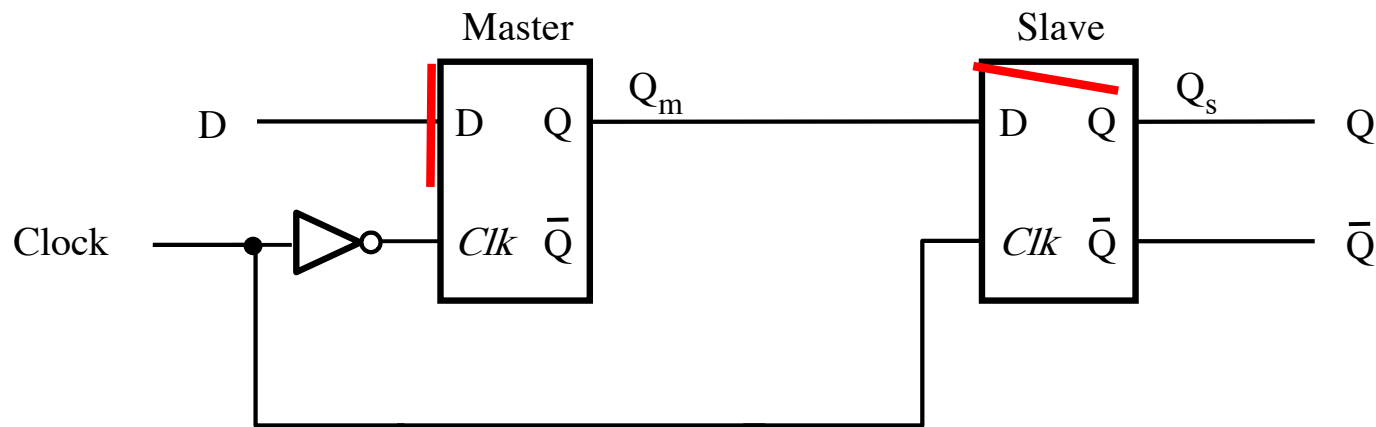
# Positive-Edge-Triggered Master-Slave D Flip-Flop



# Positive-Edge-Triggered Master-Slave D Flip-Flop

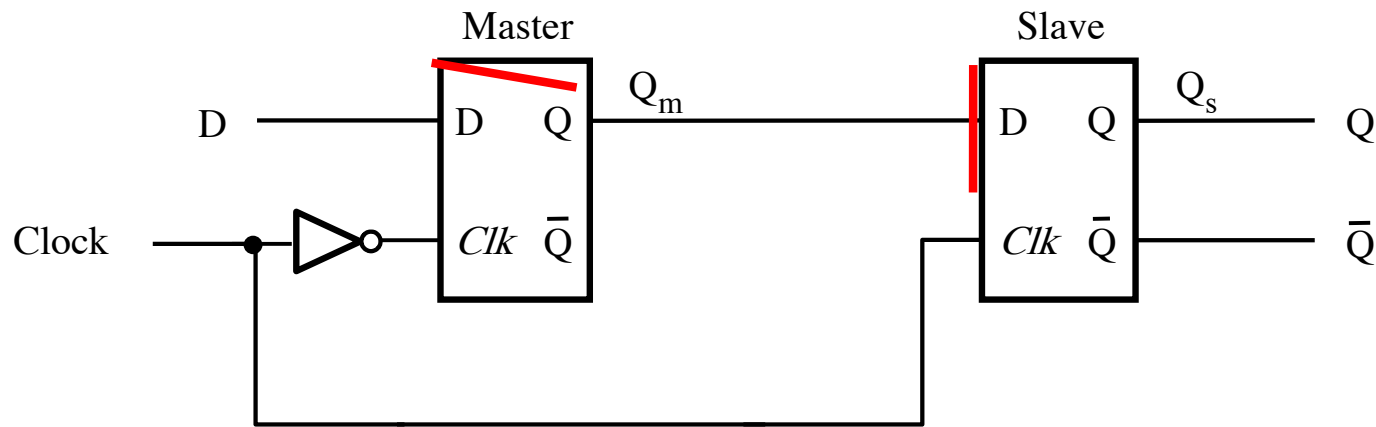


# Positive-Edge-Triggered Master-Slave D Flip-Flop

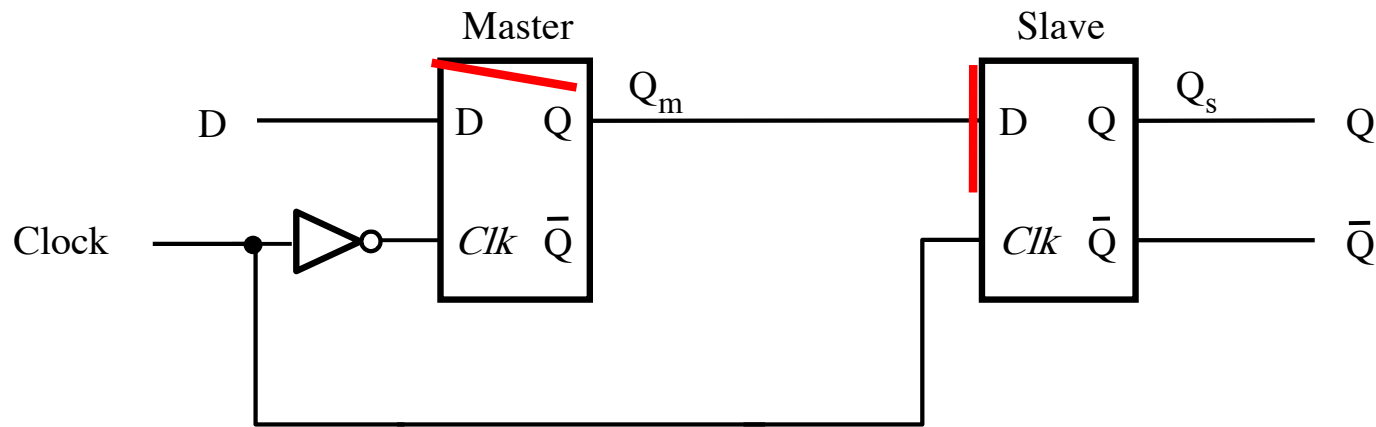




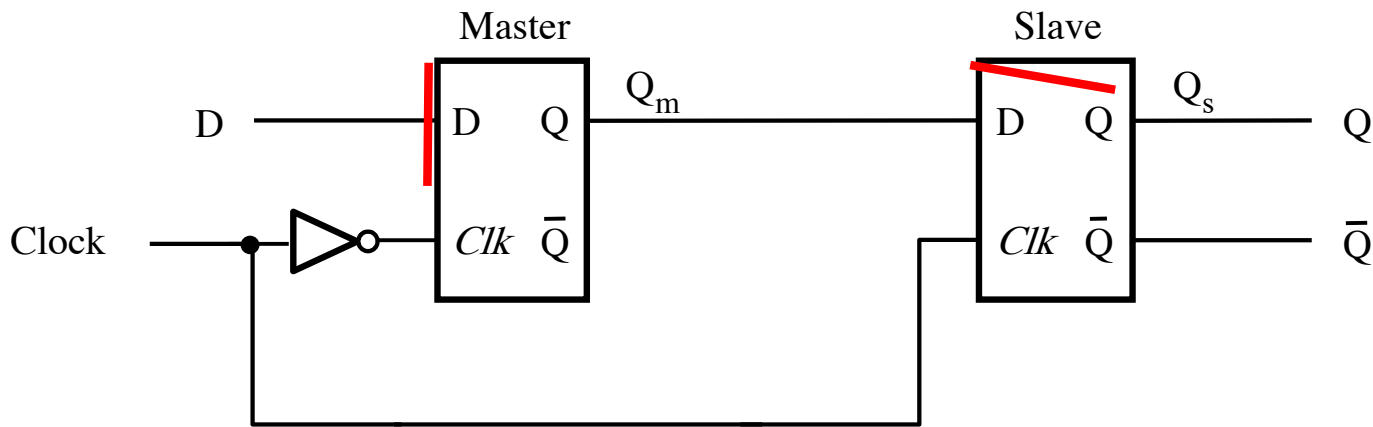
# Positive-Edge-Triggered Master-Slave D Flip-Flop



# Positive-Edge-Triggered Master-Slave D Flip-Flop

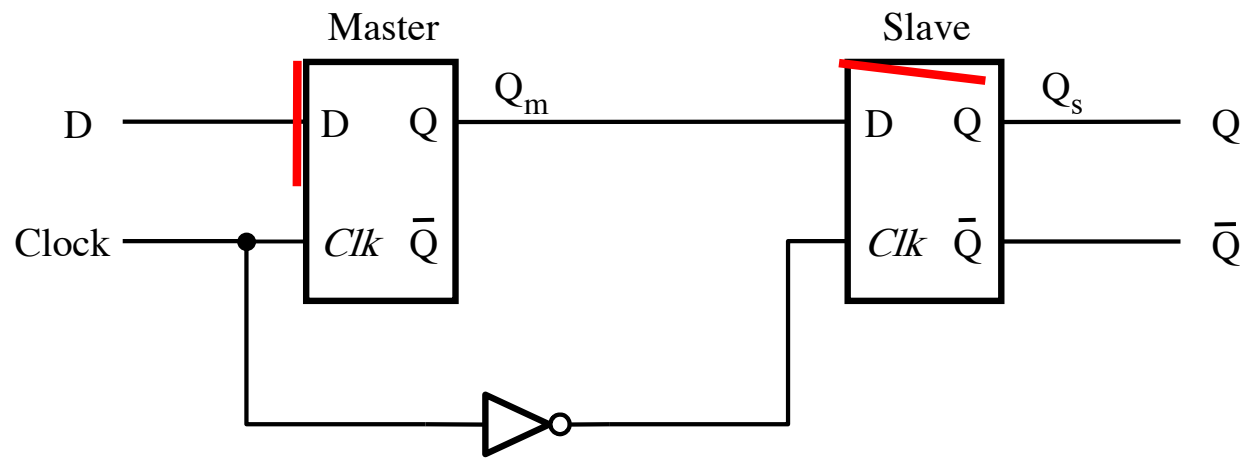


# Positive-Edge-Triggered Master-Slave D Flip-Flop

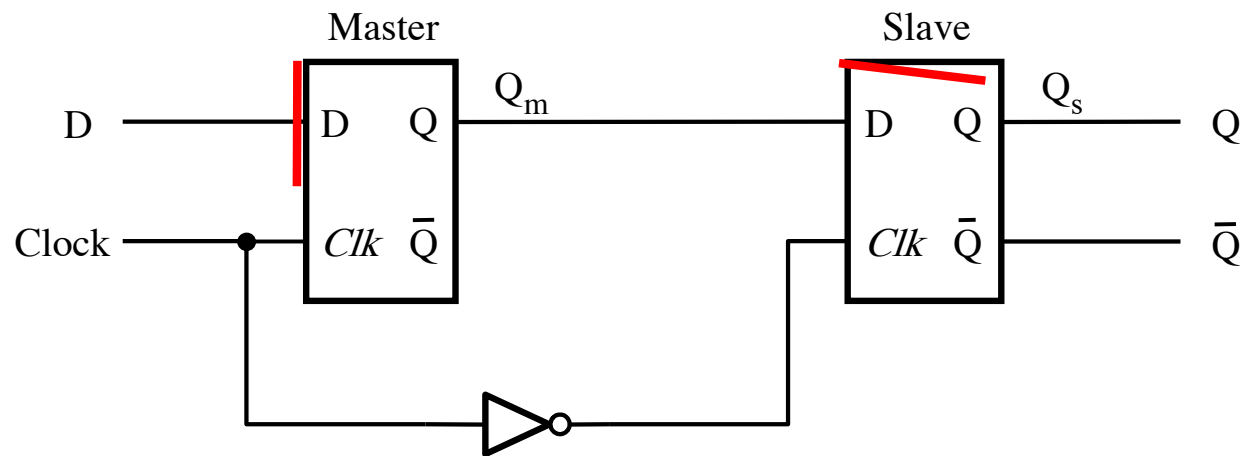




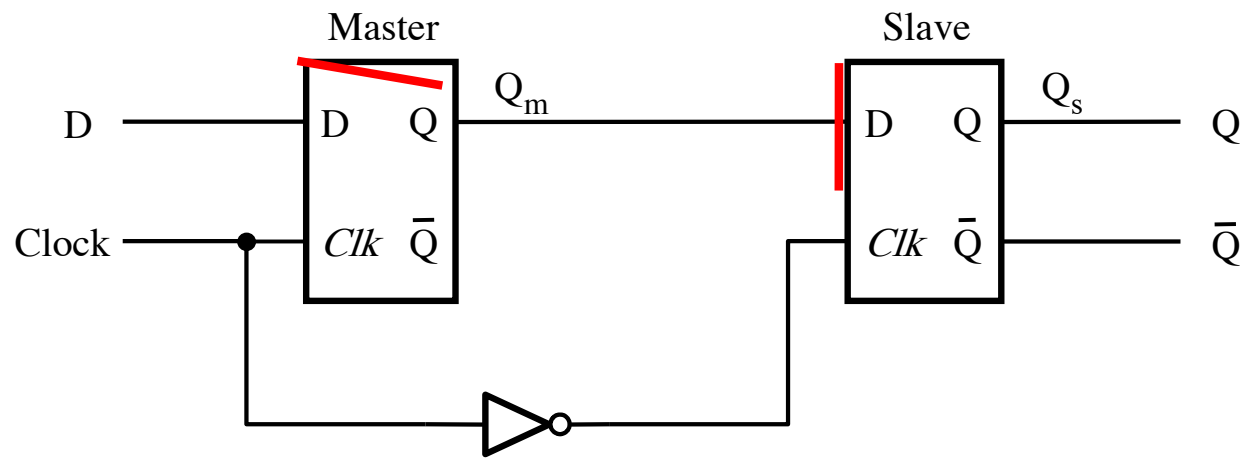
# Negative-Edge-Triggered Master-Slave D Flip-Flop



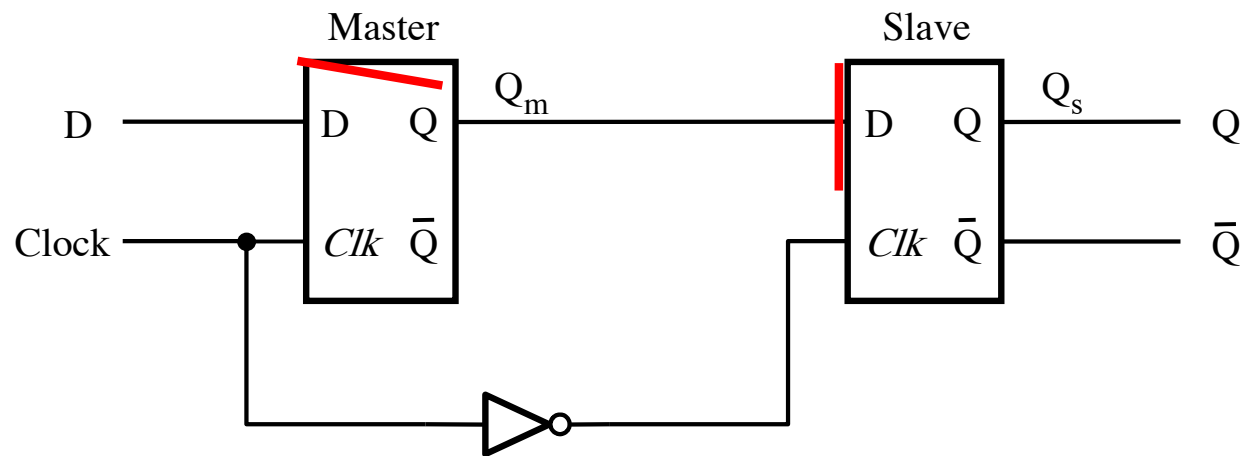
# Negative-Edge-Triggered Master-Slave D Flip-Flop



# Negative-Edge-Triggered Master-Slave D Flip-Flop

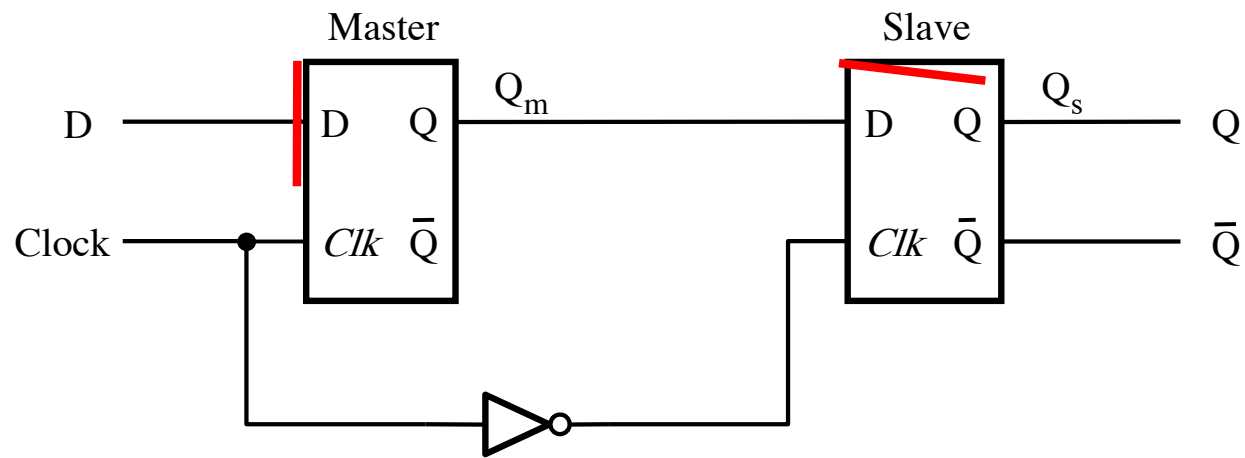


# Negative-Edge-Triggered Master-Slave D Flip-Flop

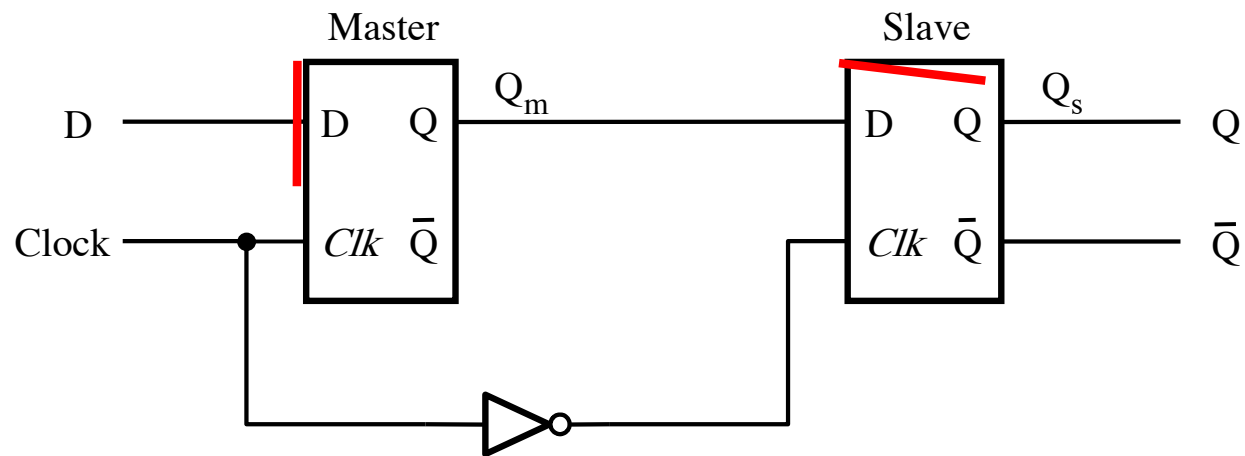




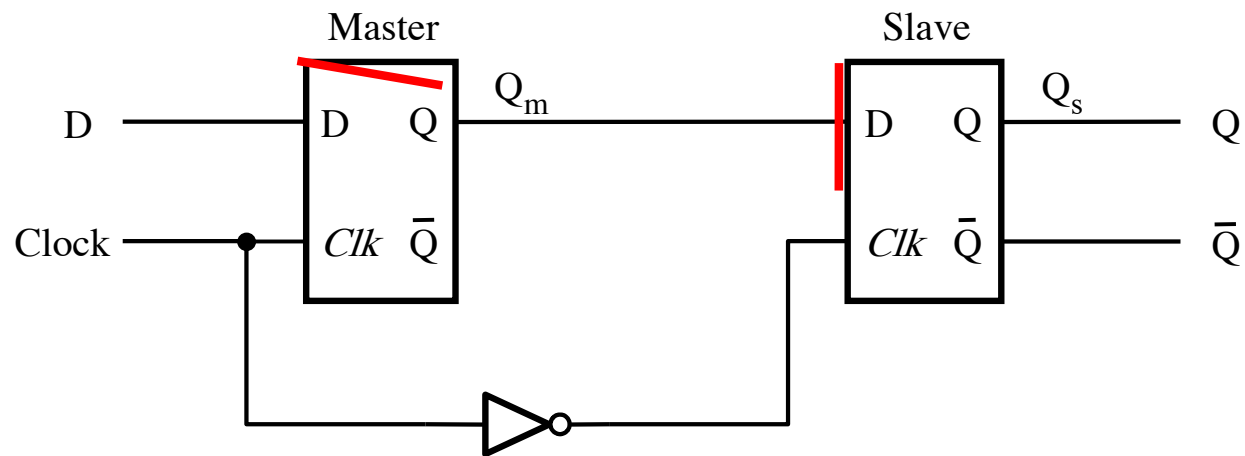
# Negative-Edge-Triggered Master-Slave D Flip-Flop



# Negative-Edge-Triggered Master-Slave D Flip-Flop

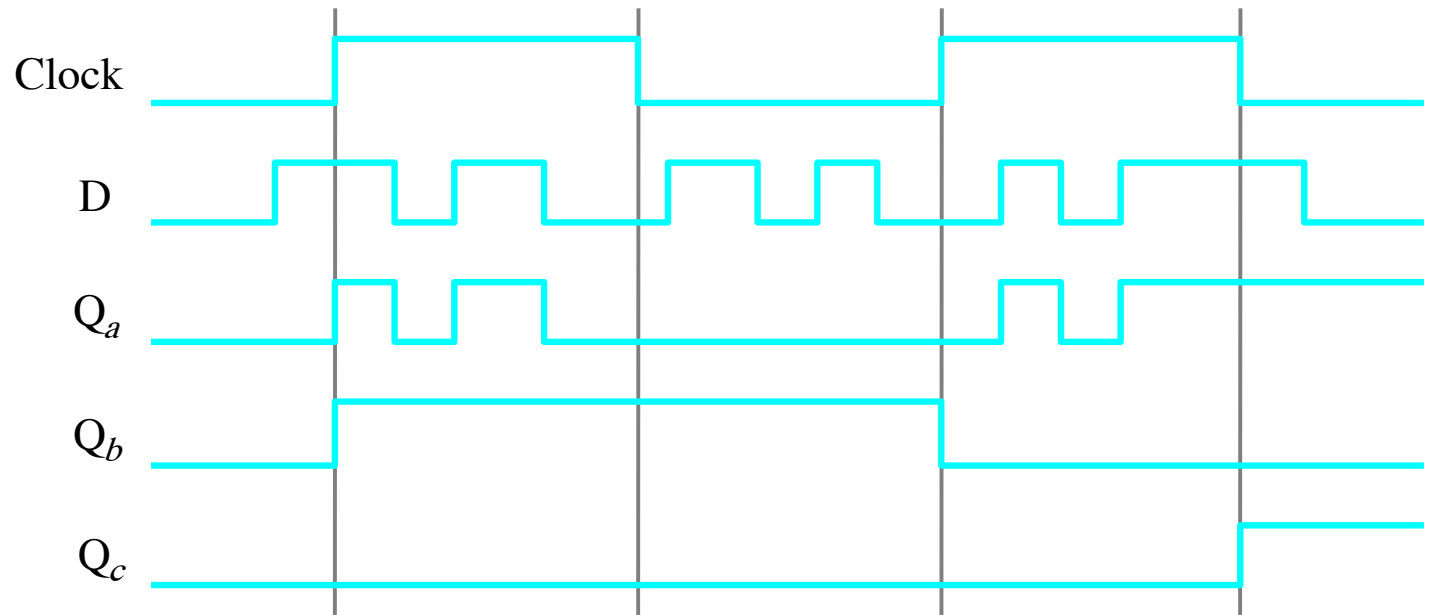
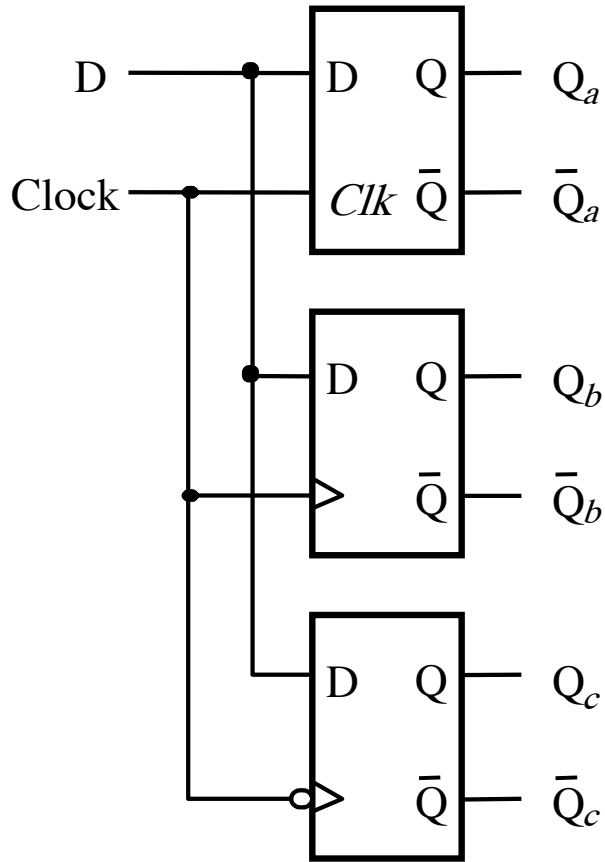


# Negative-Edge-Triggered Master-Slave D Flip-Flop

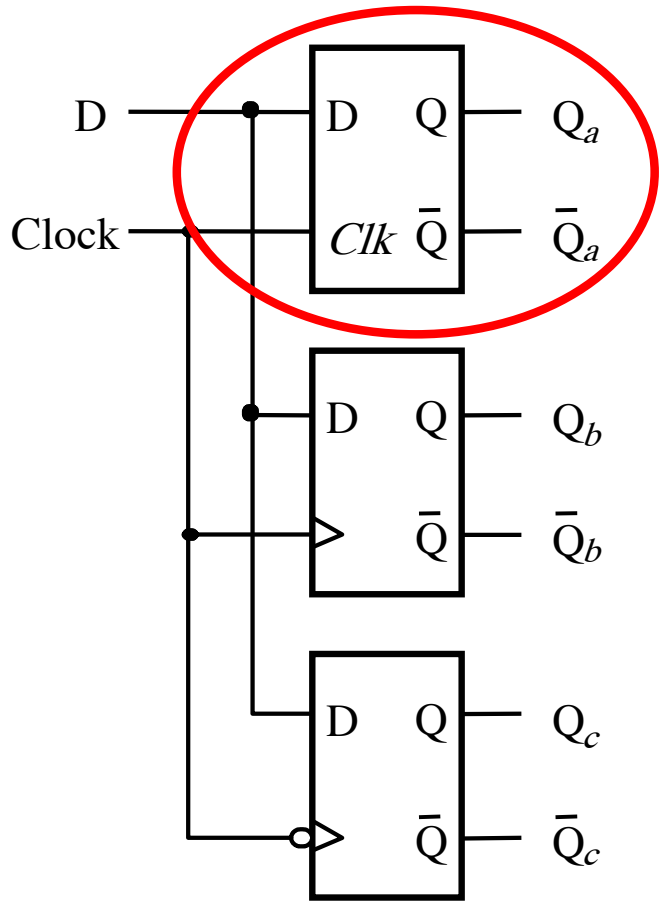


# **Level-Sensitive v.s. Edge-Triggered**

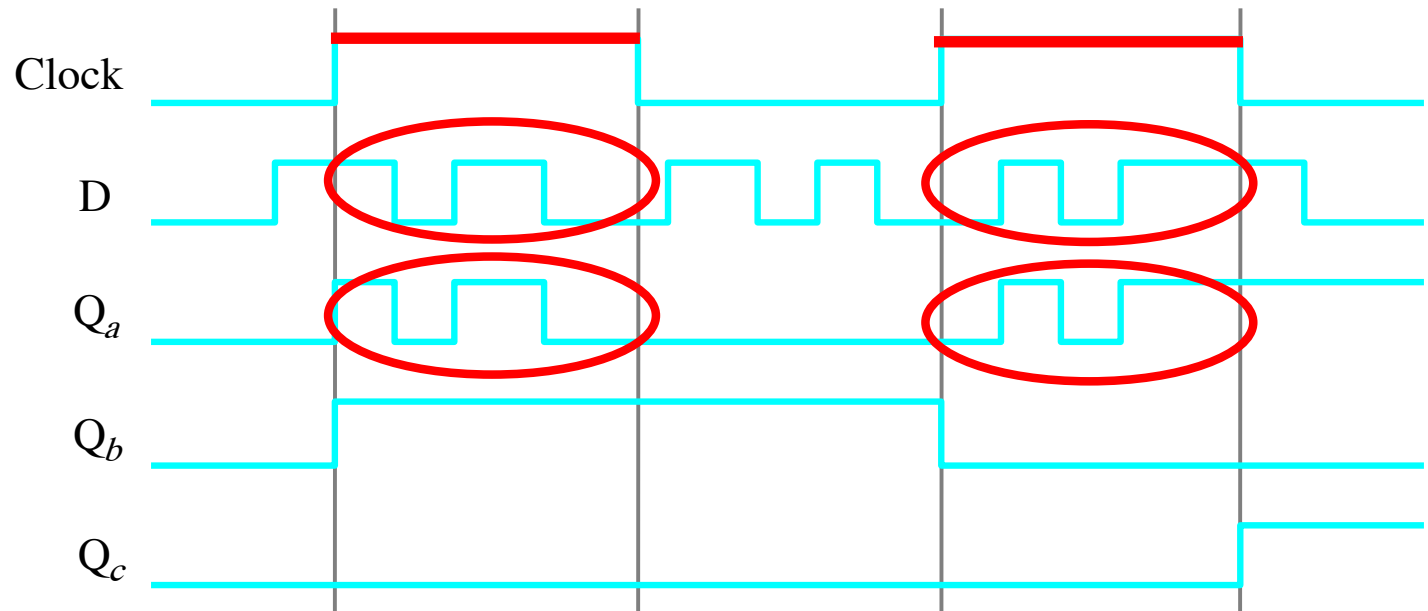
# Comparison of level-sensitive and edge-triggered D storage elements



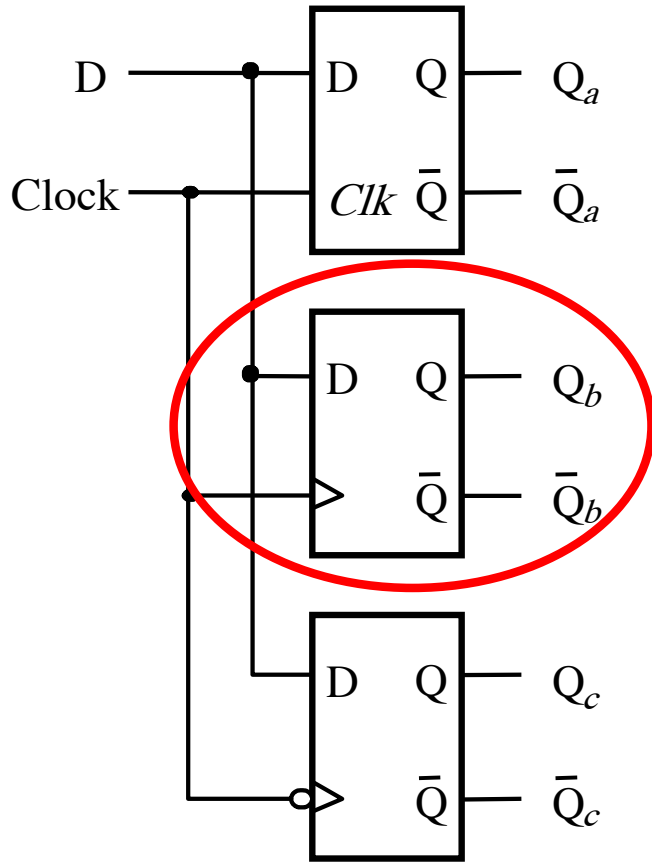
# Comparison of level-sensitive and edge-triggered D storage elements



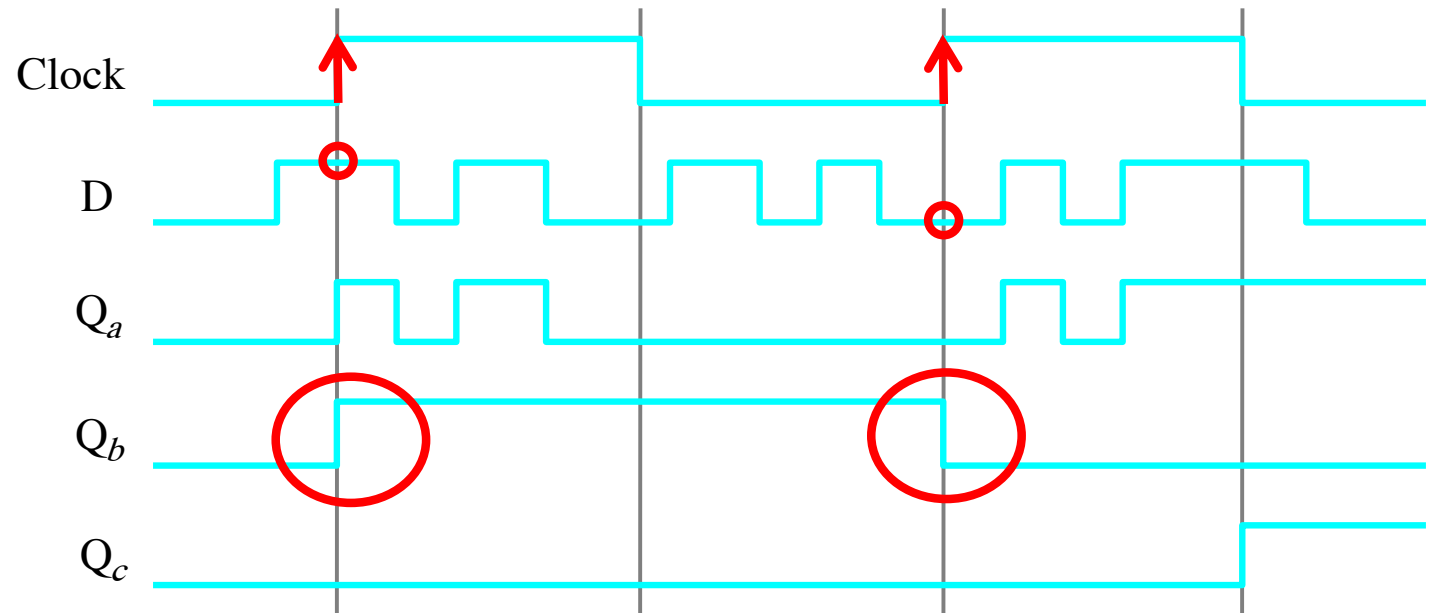
The D Latch is Level-Sensitive  
(the output mirrors the D input when Clk=1)



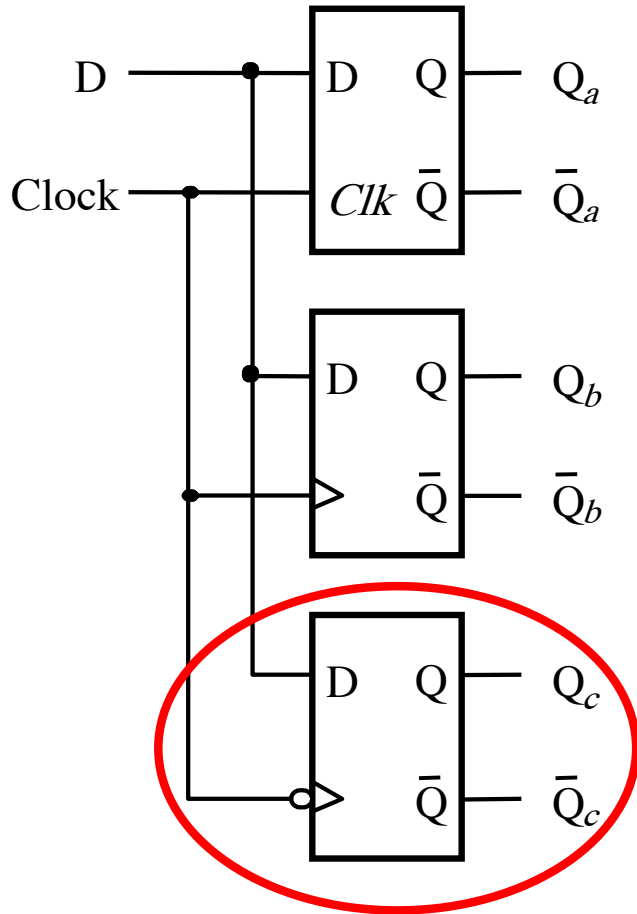
# Comparison of level-sensitive and edge-triggered D storage elements



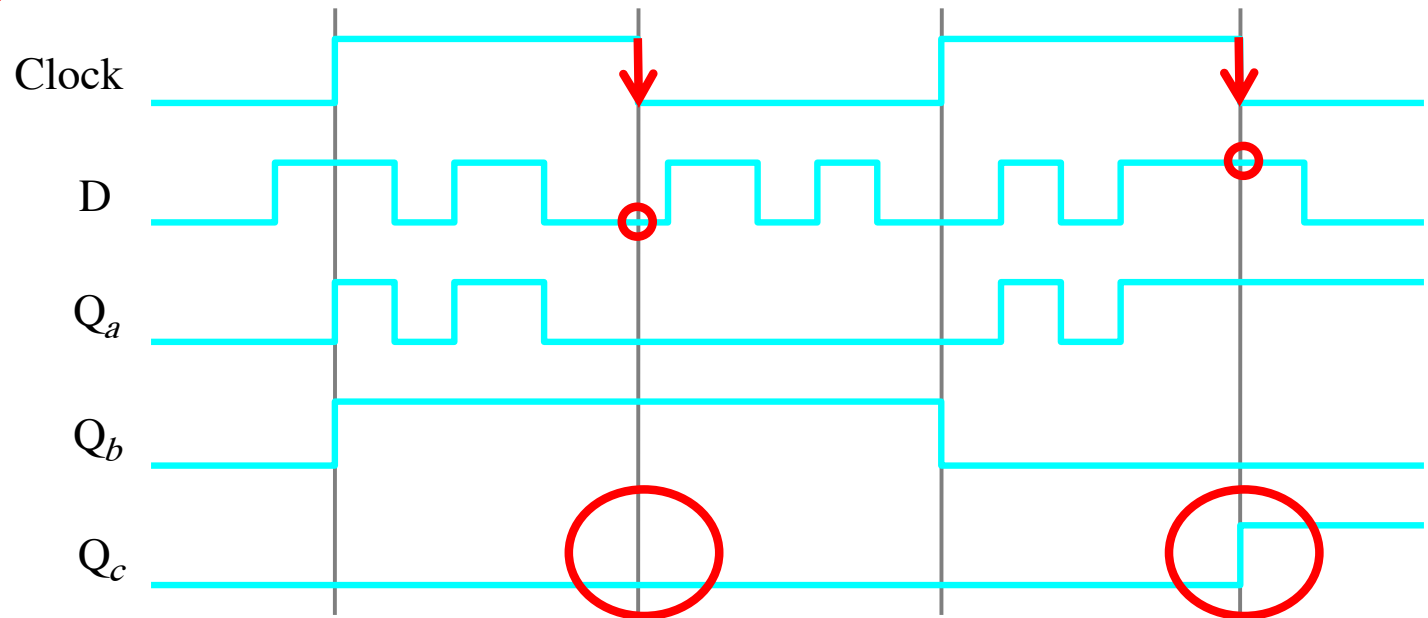
Positive-edge-triggered D Flip-Flop  
(the output is equal to the value of D right at the positive edge of the clock signal)



# Comparison of level-sensitive and edge-triggered D storage elements



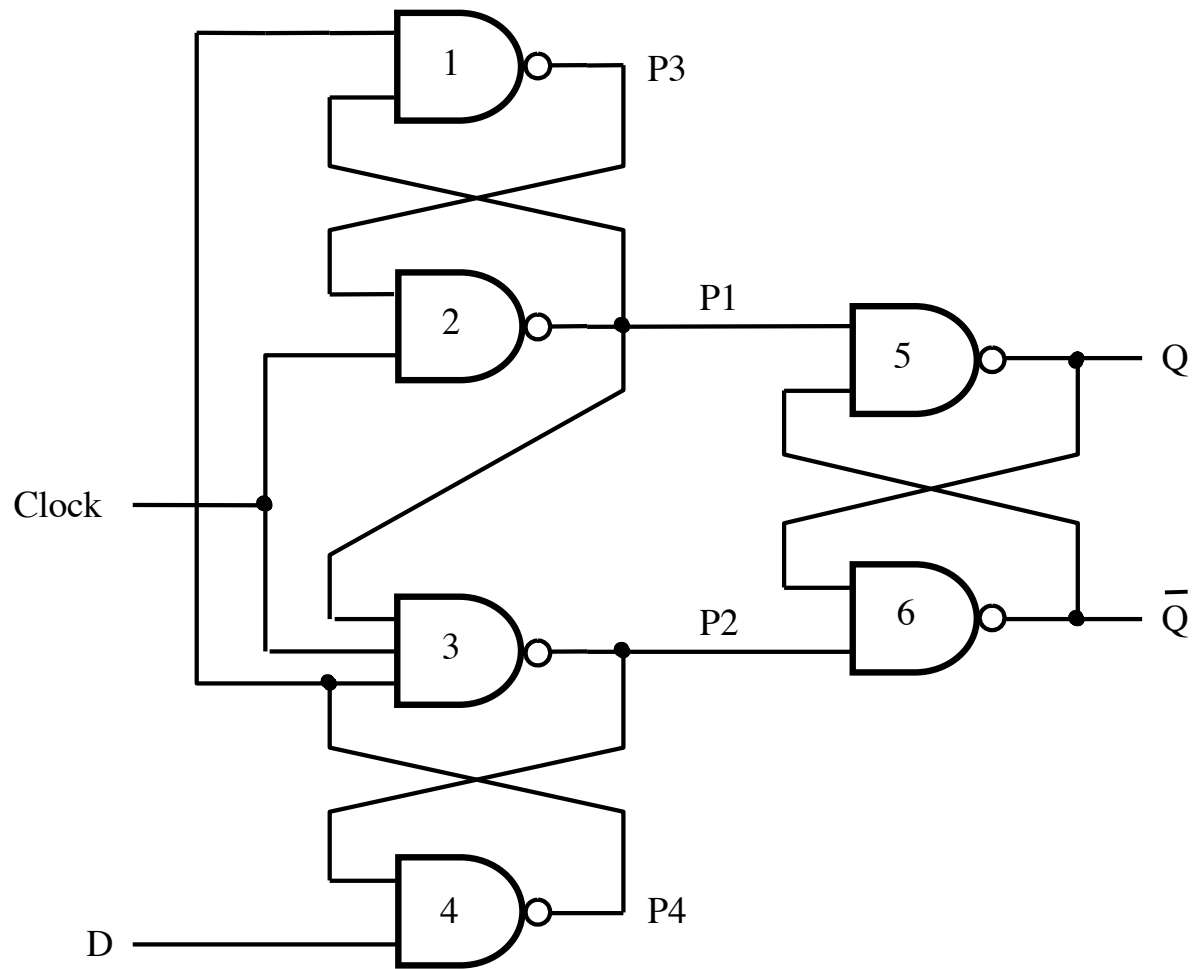
Negative-edge-triggered D Flip-Flop  
(the output is equal to the value of D right at the negative edge of the clock signal)



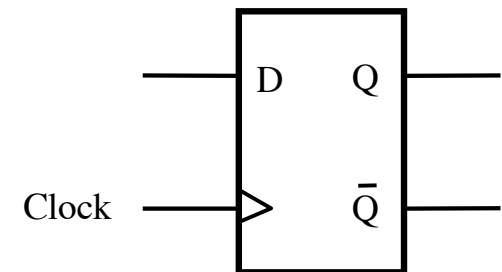


# **An alternative D Flip-Flop Design**

# A positive-edge-triggered D flip-flop



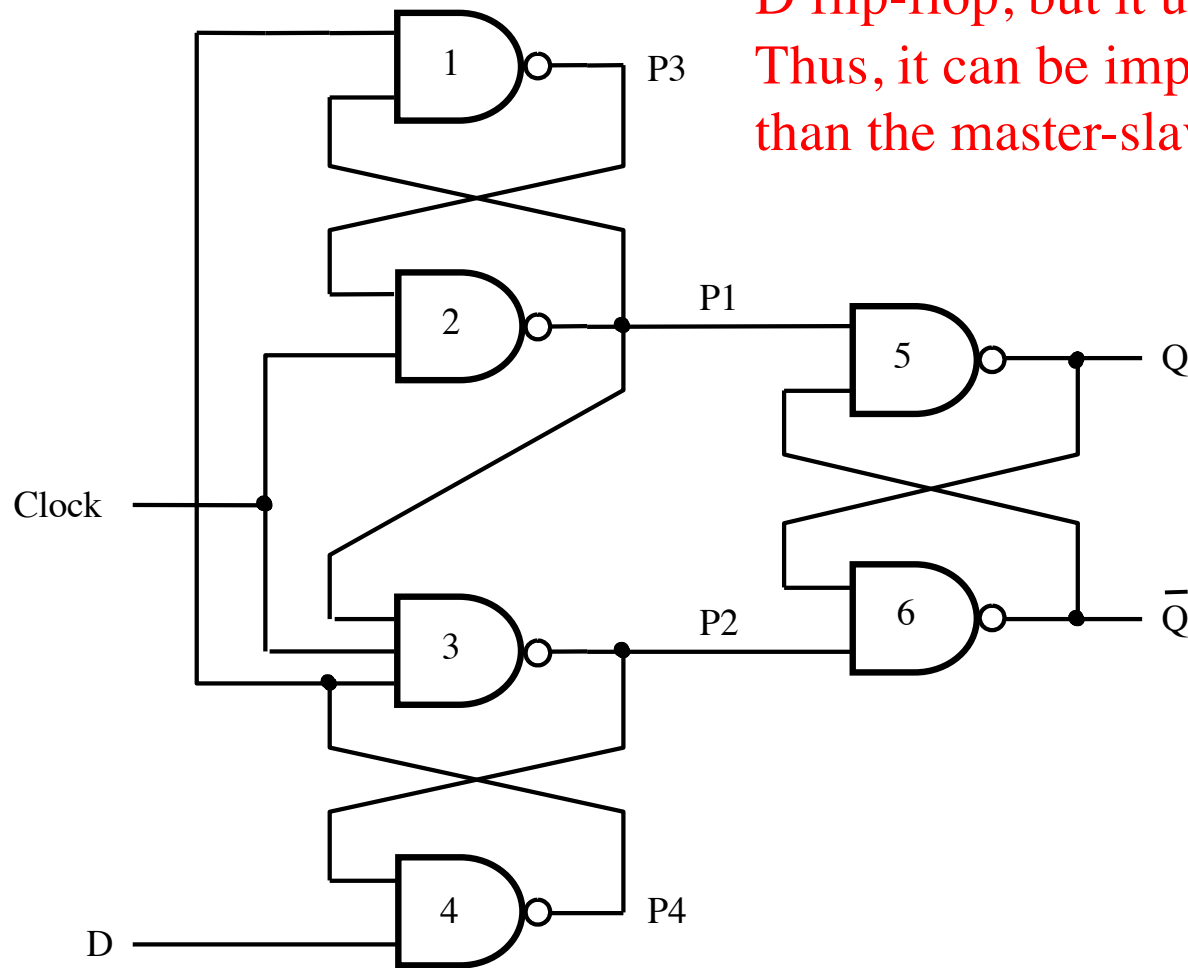
(a) Circuit



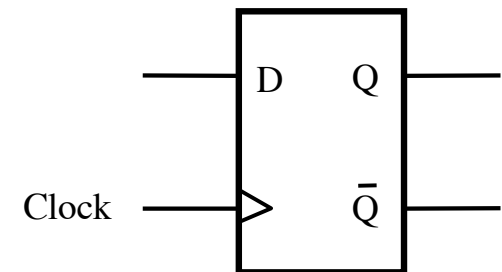
(b) Graphical symbol

# A positive-edge-triggered D flip-flop

This circuit behaves like a positive-edge-triggered D flip-flop, but it uses only 6 NAND gates. Thus, it can be implemented with fewer transistors than the master-slave D flip-flop.



(a) Circuit

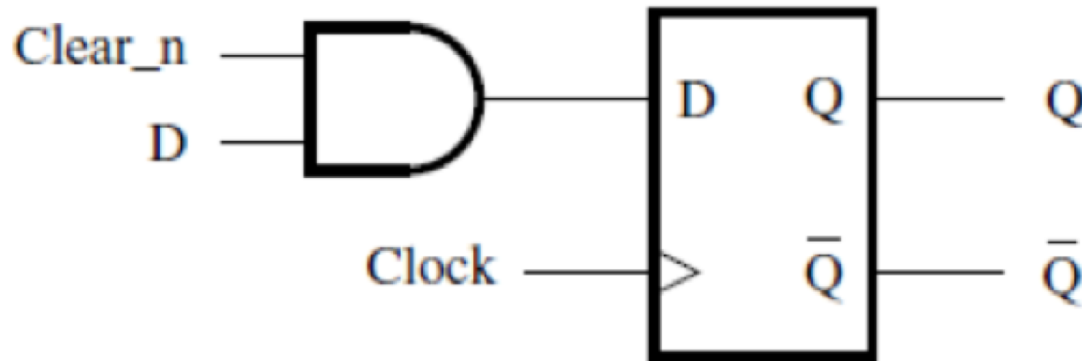


(b) Graphical symbol

# **Positive-edge-triggered D flip-flop with Clear and Preset**

# Positive-edge-triggered D flip-flop with Clear\_n and Preset\_n

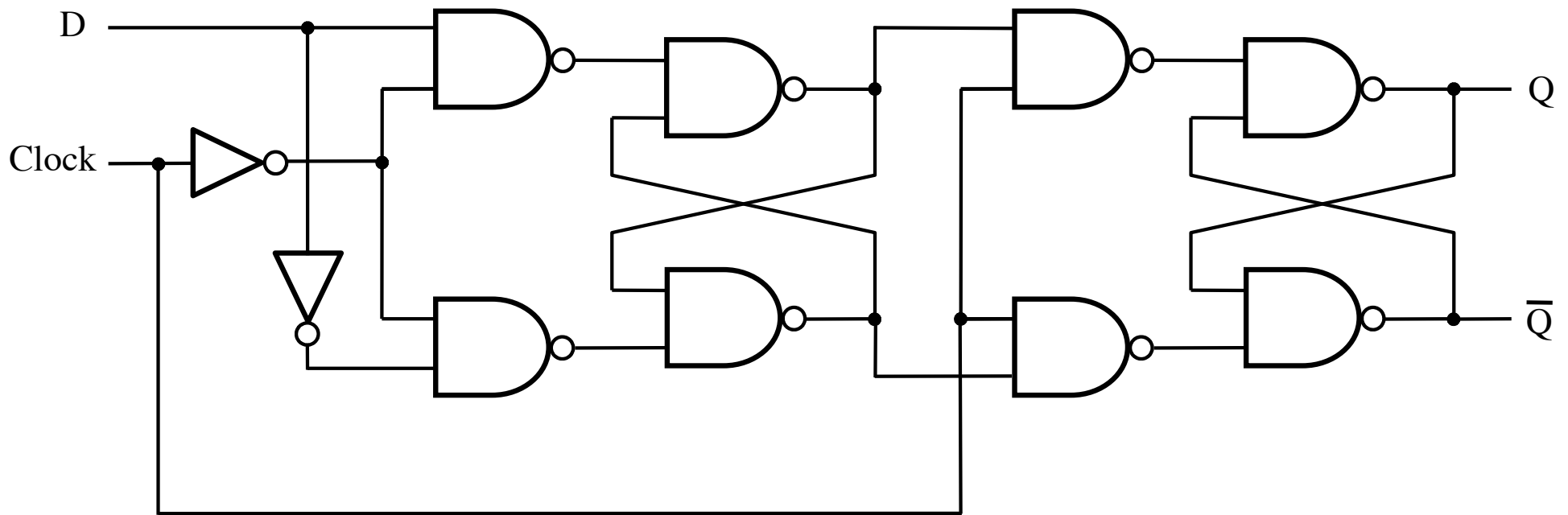
# Positive-edge-triggered D flip-flop with **Synchronous Clear**



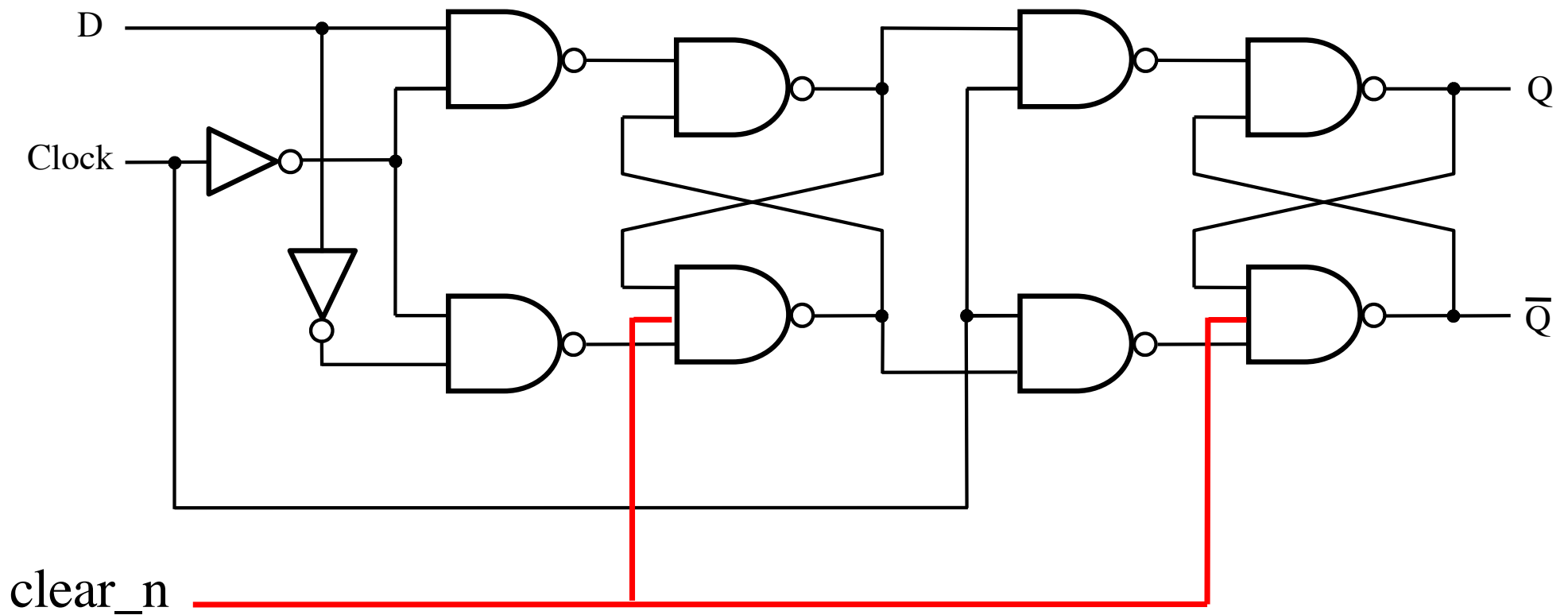
(c) Adding a synchronous clear

The output  $Q$  can be cleared only on the positive clock edge.

# The Complete Wiring Diagram for a Positive-Edge-Triggered D Flip-Flop

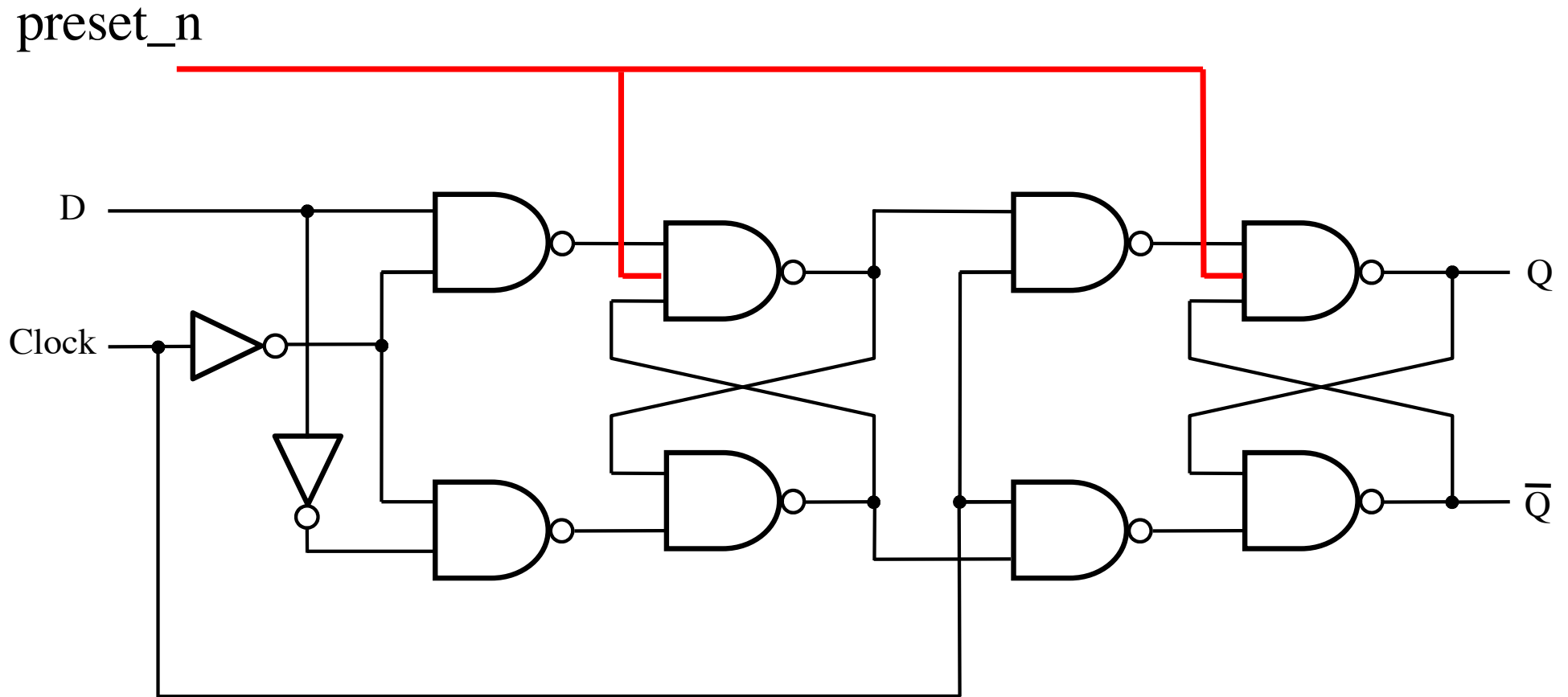


# Adding an Asynchronous Clear

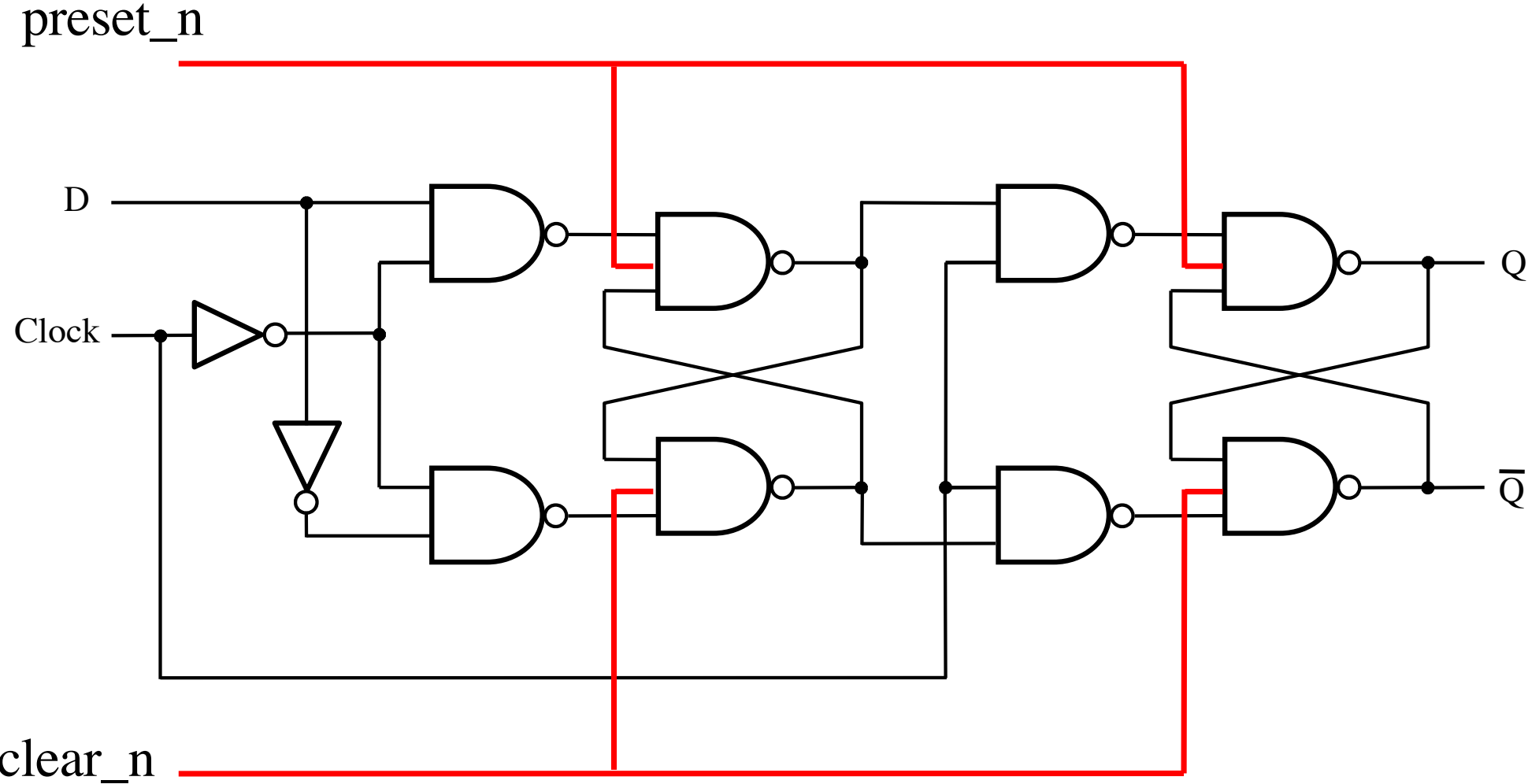




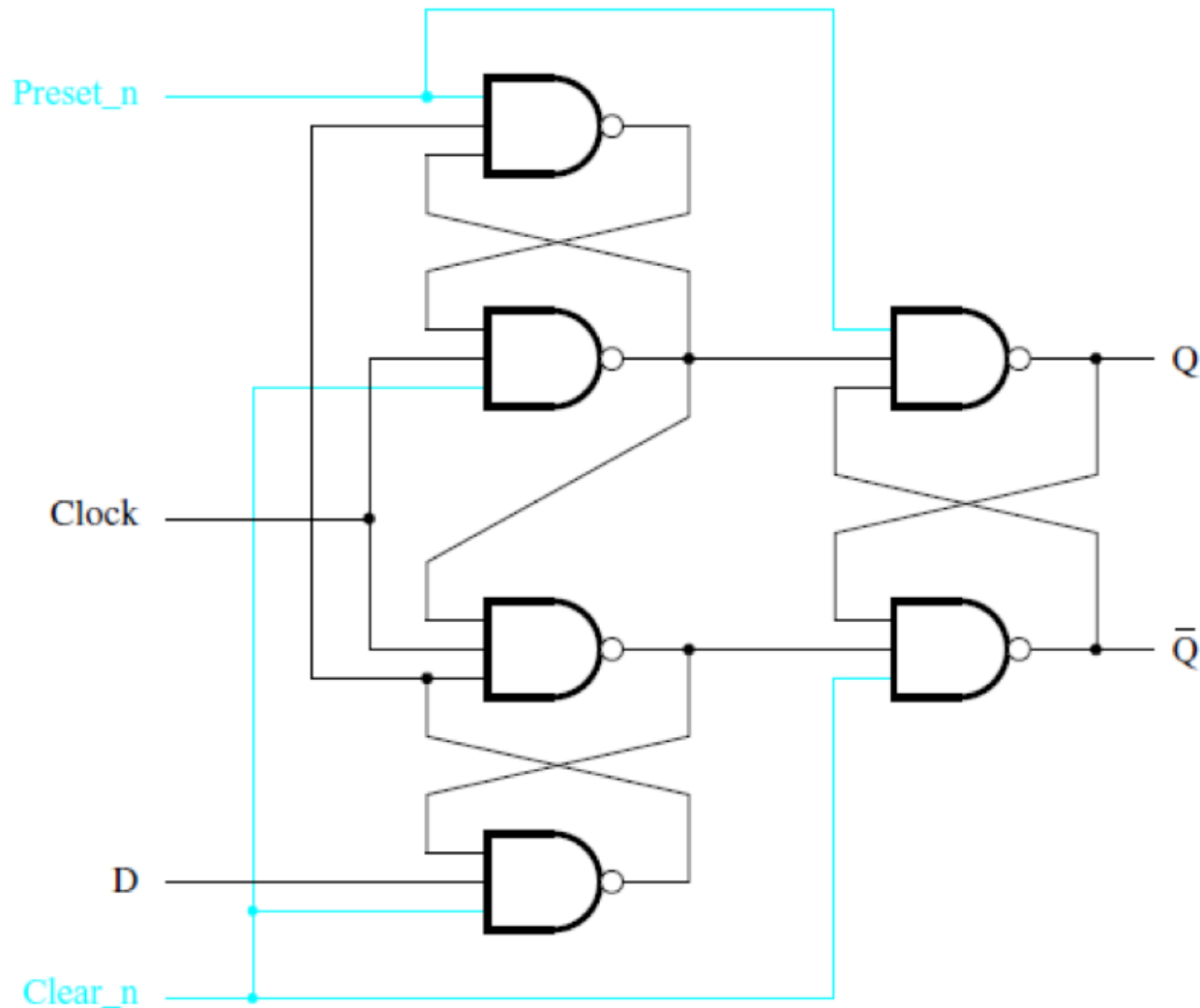
# Adding an Asynchronous Preset



# Positive-Edge-Triggered D Flip-Flop with **Asynchronous** Clear and Preset

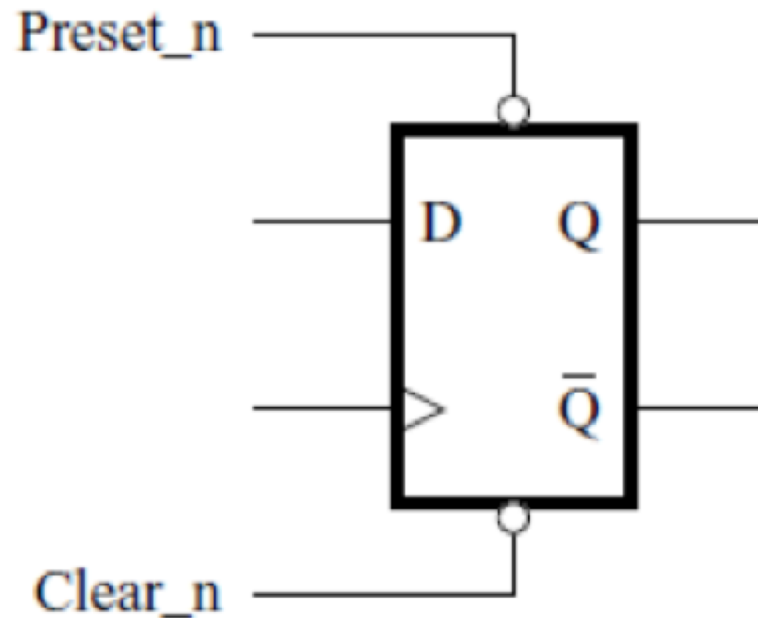


# Positive-edge-triggered D flip-flop with **asynchronous** Clear and Preset



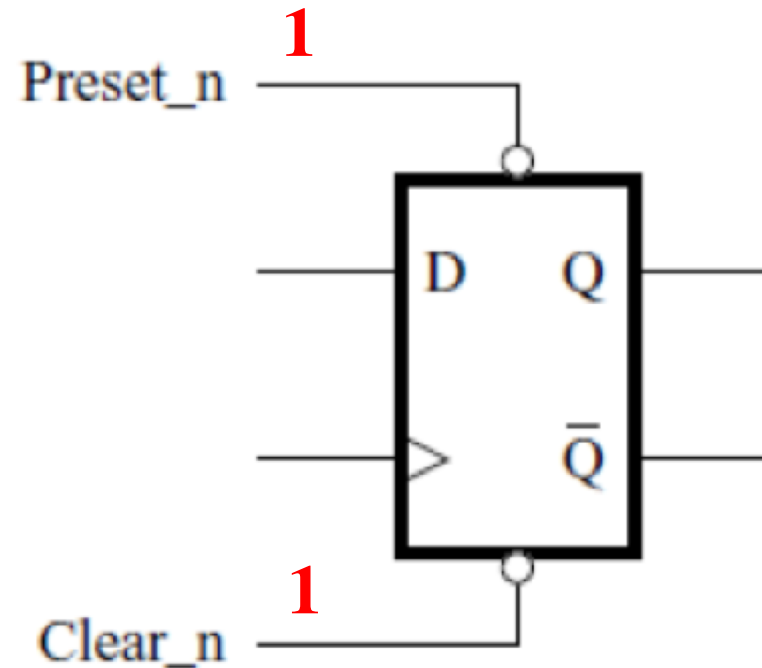
[ Figure 5.13a from the textbook ]

# Positive-edge-triggered D flip-flop with asynchronous Clear and Preset



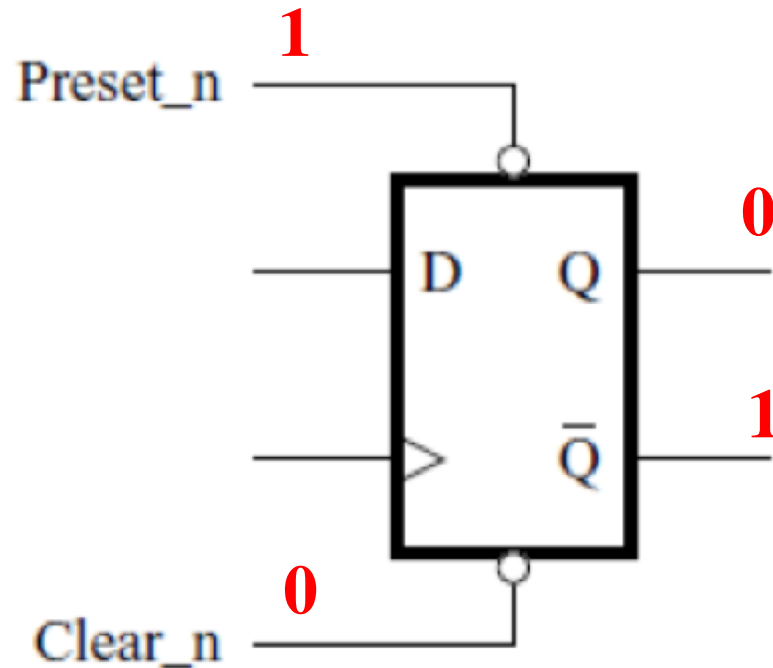
(b) Graphical symbol

**For normal operation both must be set to 1**



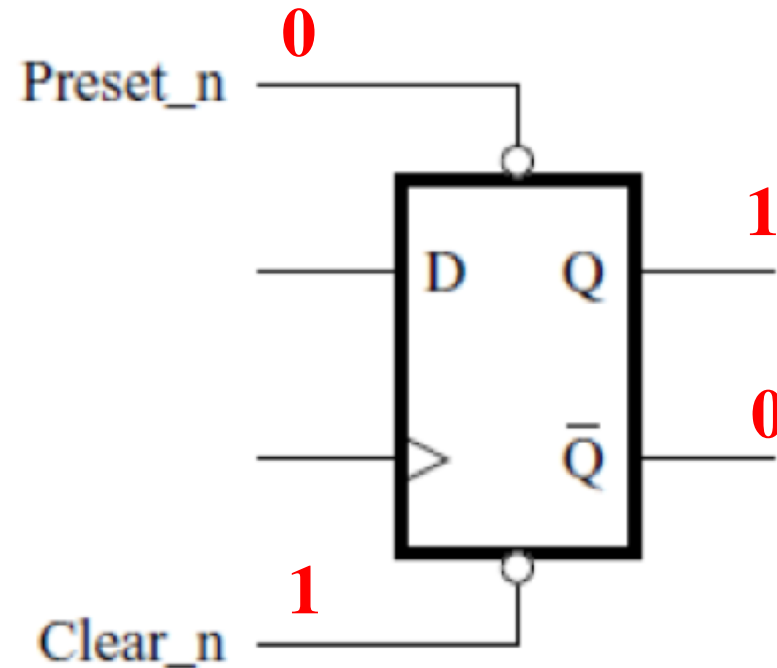
(b) Graphical symbol

**A zero on clear\_n drives the output Q to zero**



(b) Graphical symbol

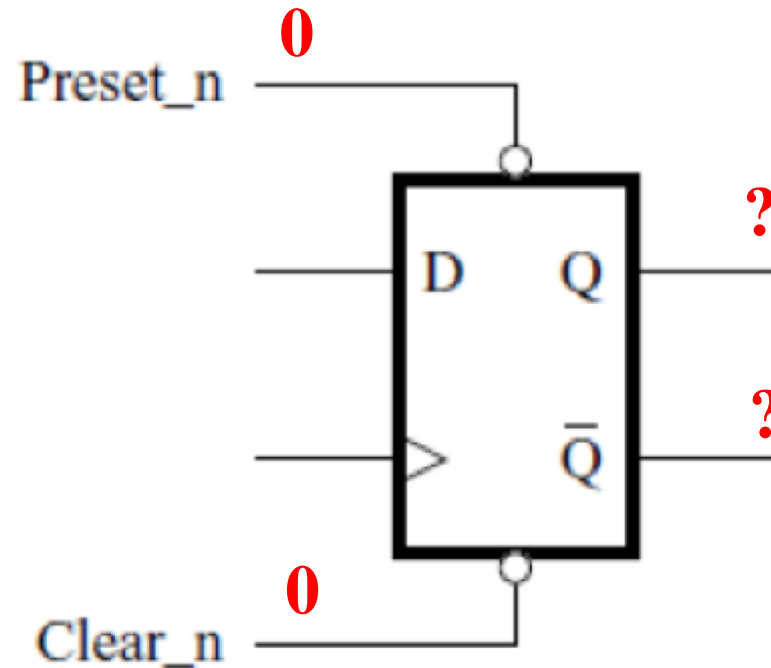
**A zero on preset\_n drives the output Q to one**



(b) Graphical symbol

# The output is indeterminate if both are zero

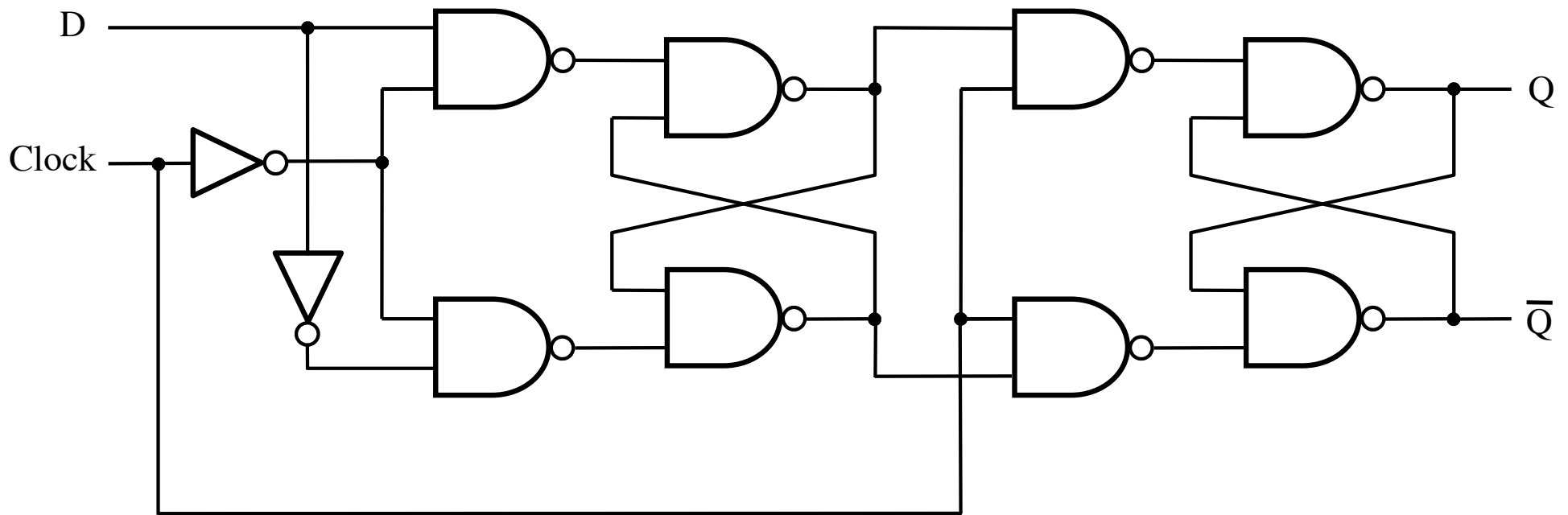
don't ever  
use this one



(b) Graphical symbol

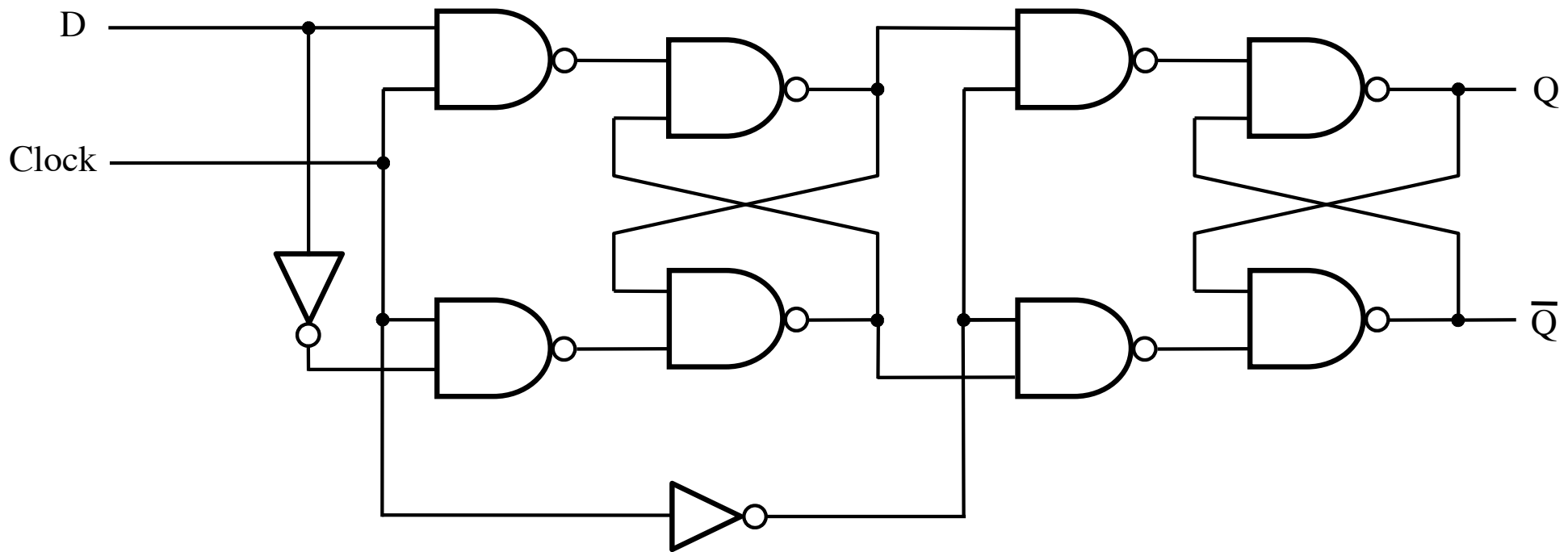


# The Complete Wiring Diagram for a Positive-Edge-Triggered D Flip-Flop

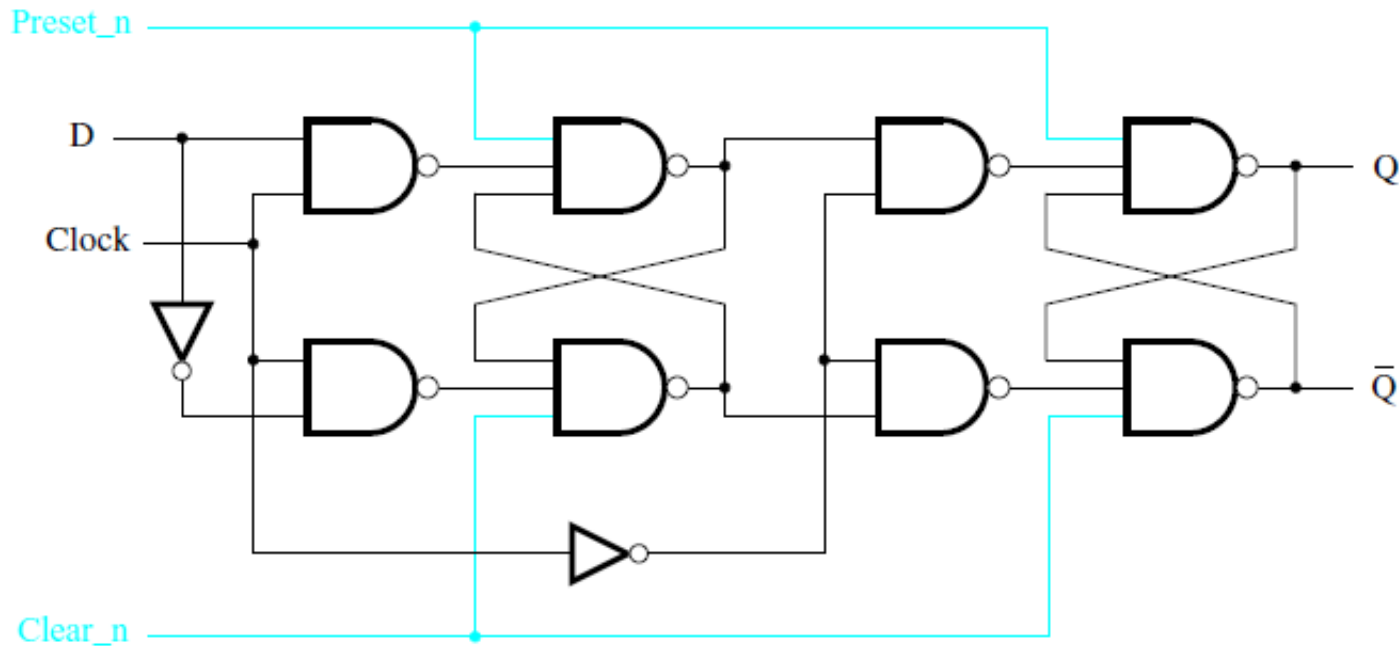




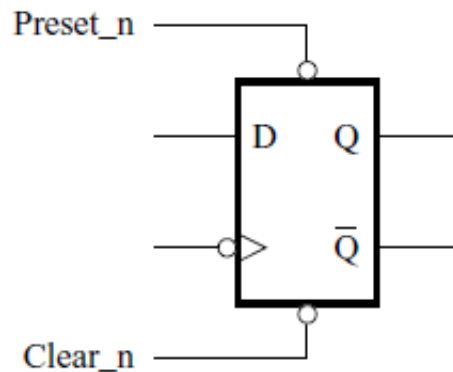
# The Complete Wiring Diagram for a **Negative**-Edge-Triggered D Flip-Flop



# Negative-Edge-Triggered D flip-flop with asynchronous Clear and Preset



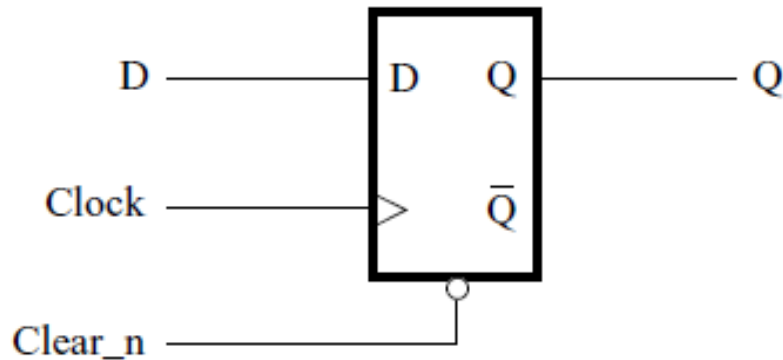
(a) Circuit



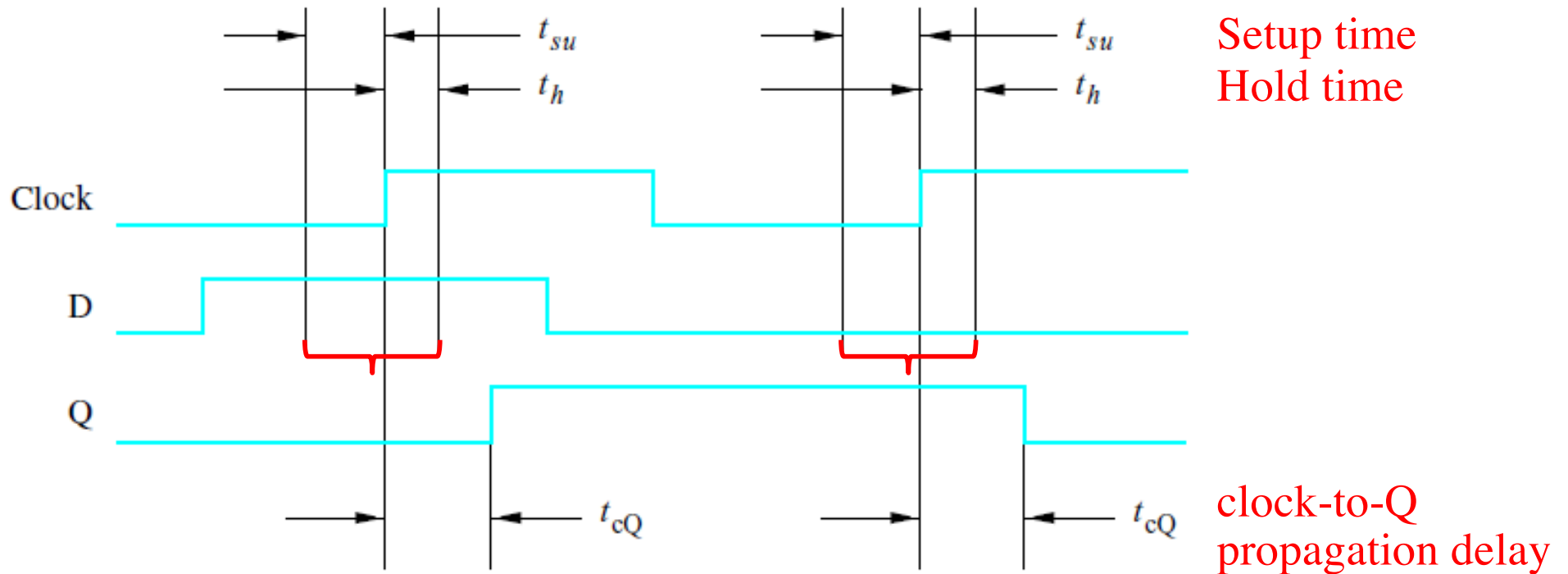
(b) Graphical symbol

[ Figure 5.12 from the textbook ]

# Flip-Flop Timing Parameters



(a) D flip-flop with asynchronous clear



[ Figure 5.14 from the textbook ]

(b) Timing diagram

# Terminology

- **Basic Latch** – is a feedback connection of two NOR gates or two NAND gates, which can store one bit of information. It can be set using the S input and reset to 0 using the R input.
- **Gated Latch** – is a basic latch that includes input gating and a control input signal. The latch retains its existing state when the control input is equal to 0. Its state may be changed when the control signal is equal to 1.

# Terminology

- **Two types of gated latches**  
**(the control input is the clock):**
- **Gated SR Latch** – uses the S and R inputs to set the latch to 1 or reset it to 0.
- **Gated D Latch** – uses the D input to force the latch into a state that has the same logic value as the D input.

# Terminology

- **Flip-Flop** – is a storage element that can have its output state changed only on the edge of the controlling clock signal.
- **Positive-edge triggered** – if the state changes when the clock signal goes from 0 to 1.
- **Negative-edge triggered** – if the state changes when the clock signal goes from 1 to 0.



# Terminology

The word ***latch*** is mainly used for storage elements, while clocked devices are described as ***flip-flops***.

A **latch** is level-sensitive, whereas a **flip-flop** is edge-sensitive. That is, when a latch is enabled it becomes transparent, while a flip flop's output only changes on a single type of clock edge (positive going or negative going).

**Questions?**

**THE END**