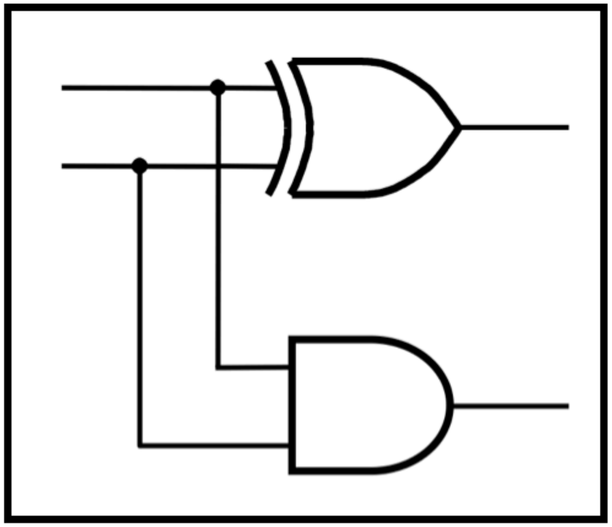


CprE 281: Digital Logic

Instructor: Alexander Stoytchev

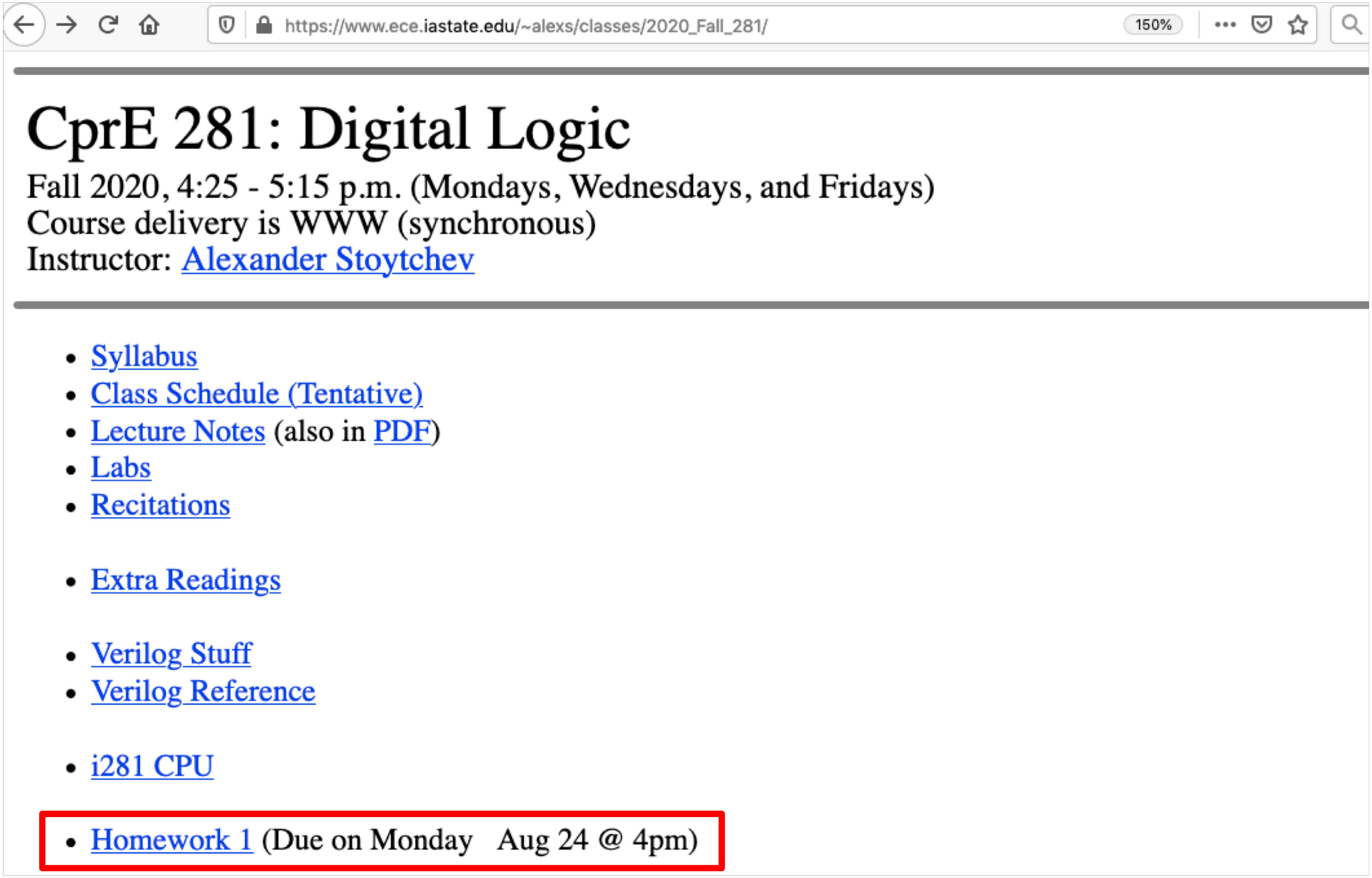
http://www.ece.iastate.edu/~alexs/classes/

Logic Gates

CprE 281: Digital Logic
Iowa State University, Ames, IA

Administrative Stuff

- **HW1 is out. It is due on Monday Aug 24 @ 4pm.**
- **Submit it as a PDF upload on Canvas before the start of the lecture.**
- **You can write the solutions on paper and then scan the pages to make **one** PDF file.**
- **No late homeworks will be accepted.**
- **Please write clearly on the first page:**
  - **your name**
  - **student ID**
  - **lab section number**



https://www.ece.iastate.edu/~alexs/classes/2020_Fall_281/

CprE 281: Digital Logic

Fall 2020, 4:25 - 5:15 p.m. (Mondays, Wednesdays, and Fridays)
Course delivery is WWW (synchronous)
Instructor: Alexander Stoytchev

- Syllabus
- Class Schedule (Tentative)
- Lecture Notes (also in PDF)
- Labs
- Recitations

- Extra Readings

- Verilog Stuff
- Verilog Reference

- i281 CPU

- Homework 1 (Due on Monday Aug 24 @ 4pm)

Labs Next Week

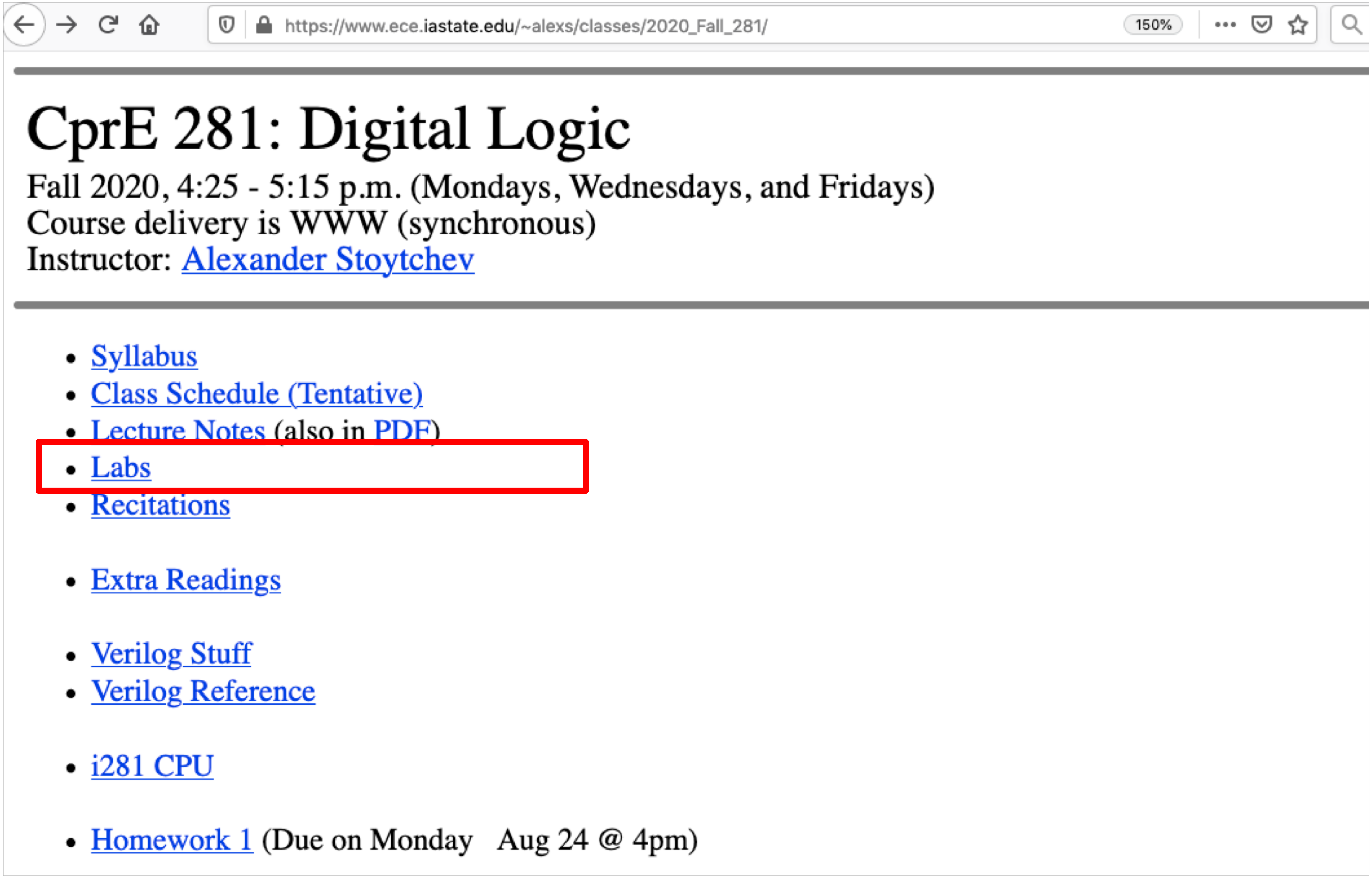
- Please download and read the lab assignment for next week before you go to your lab section.

- https://www.ece.iastate.edu/~alexs/classes/2020_Fall_281/labs/Instructions/

- https://www.ece.iastate.edu/~alexs/classes/2020_Fall_281/labs/Lab_01/

- You must and do the prelab before you go to the lab.

- The TAs will check your prelab answers at the beginning of the recitation. If you don't have it done you'll lose 20% of the lab grade for that lab.



https://www.ece.iastate.edu/~alexs/classes/2020_Fall_281/

CprE 281: Digital Logic

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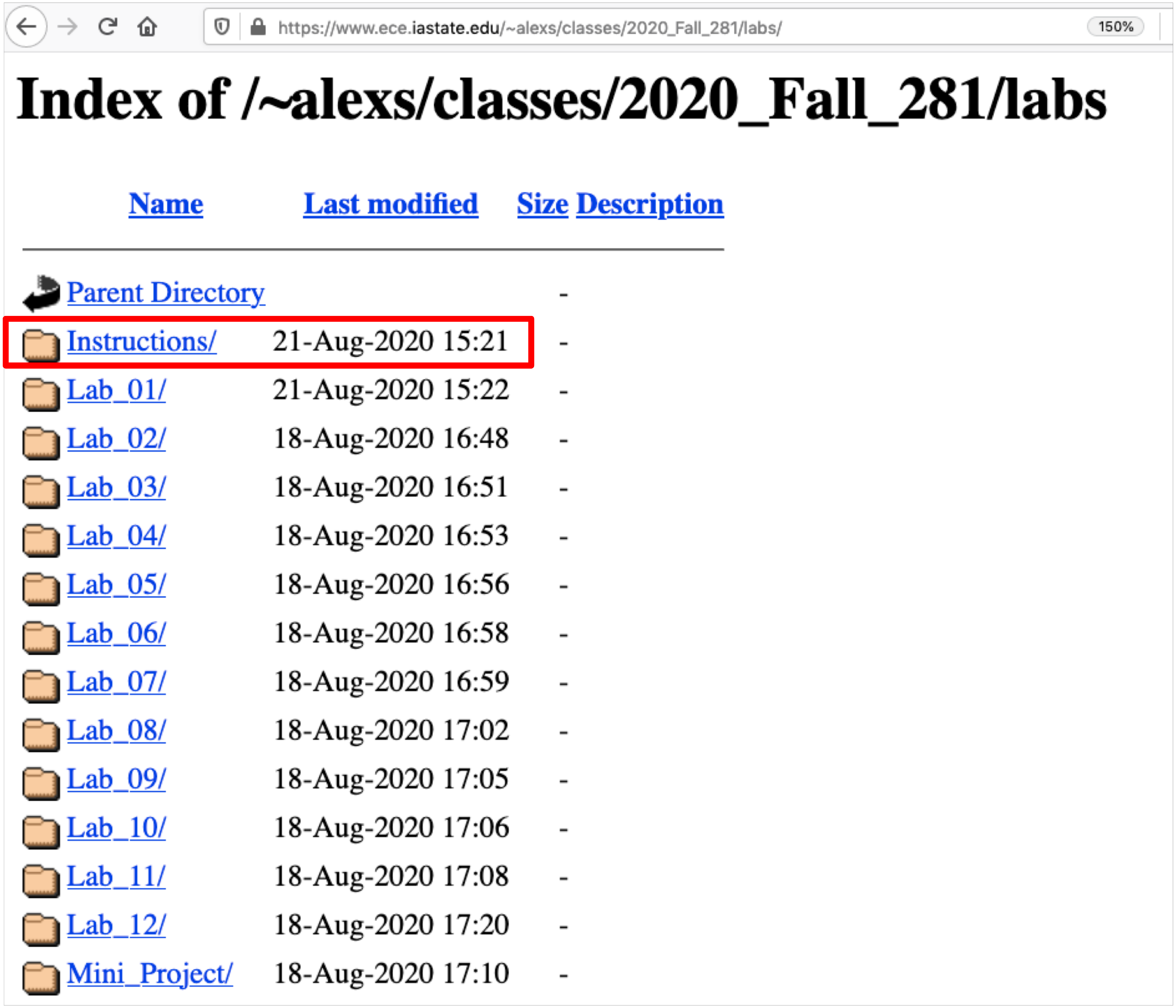
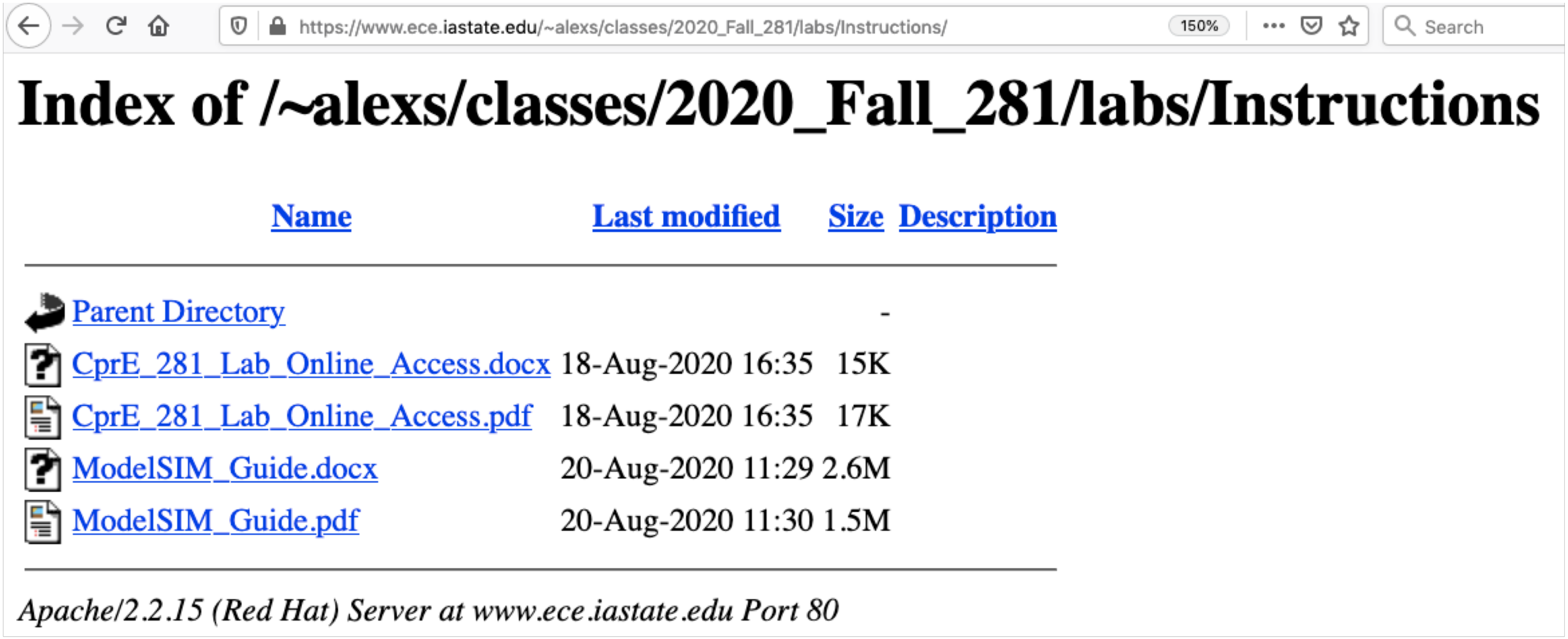

https://www.ece.iastate.edu/~alexs/classes/2020_Fall_281/labs/
150%

Index of /~alexs/classes/2020_Fall_281/labs

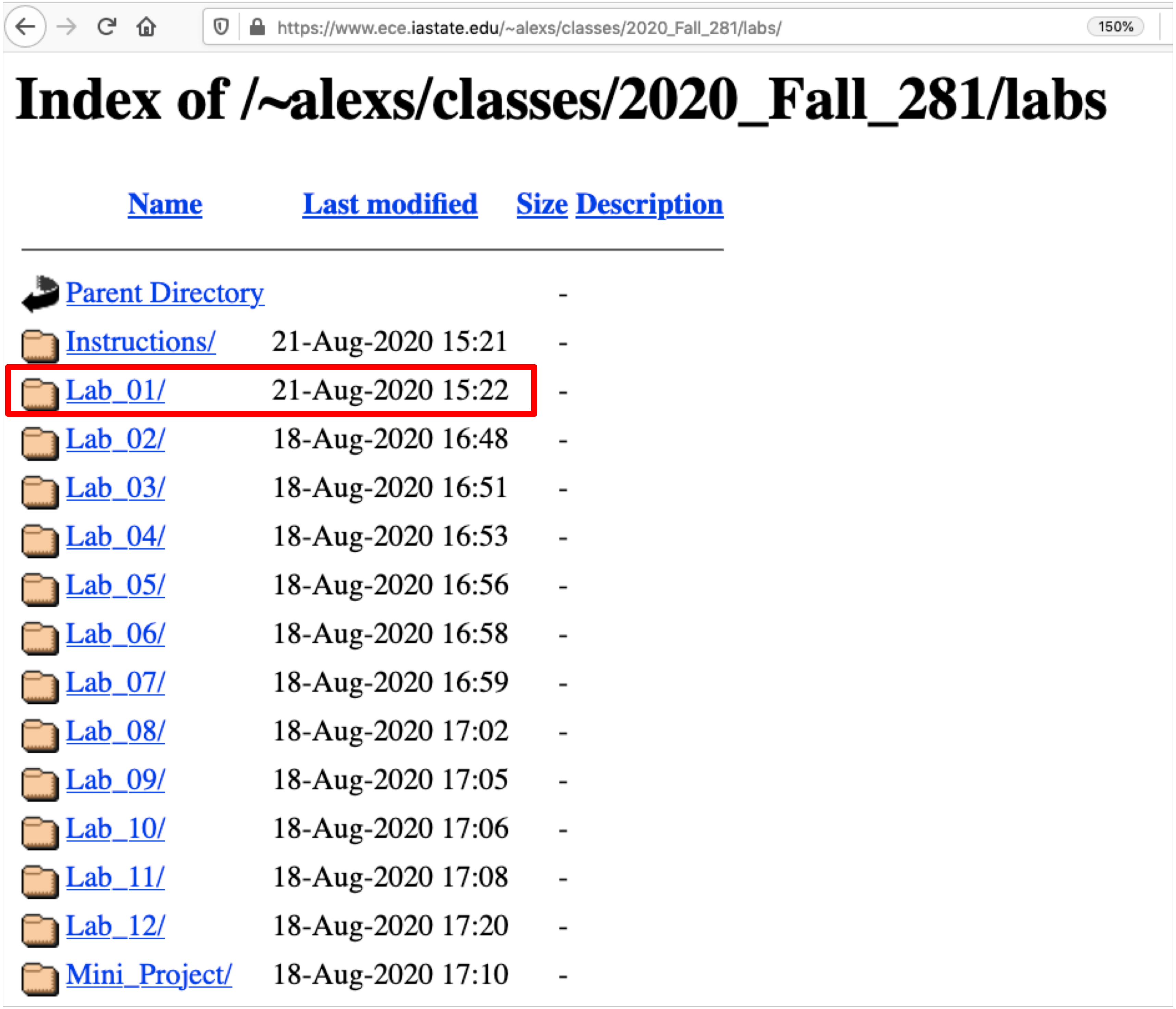
Name	Last modified	Size	Description
Parent Directory		-	
Instructions/	21-Aug-2020 15:21	-	
Lab_01/	21-Aug-2020 15:22	-	
Lab_02/	18-Aug-2020 16:48	-	
Lab_03/	18-Aug-2020 16:51	-	
Lab_04/	18-Aug-2020 16:53	-	
Lab_05/	18-Aug-2020 16:56	-	
Lab_06/	18-Aug-2020 16:58	-	
Lab_07/	18-Aug-2020 16:59	-	
Lab_08/	18-Aug-2020 17:02	-	
Lab_09/	18-Aug-2020 17:05	-	
Lab_10/	18-Aug-2020 17:06	-	
Lab_11/	18-Aug-2020 17:08	-	
Lab_12/	18-Aug-2020 17:20	-	
Mini_Project/	18-Aug-2020 17:10	-	


https://www.ece.iastate.edu/~alexs/classes/2020_Fall_281/labs/Instructions/
150%
Search

Index of /~alexs/classes/2020_Fall_281/labs/Instructions

Name	Last modified	Size	Description
Parent Directory		-	
CprE_281_Lab_Online_Access.docx	18-Aug-2020 16:35	15K	
CprE_281_Lab_Online_Access.pdf	18-Aug-2020 16:35	17K	
ModelSIM_Guide.docx	20-Aug-2020 11:29	2.6M	
ModelSIM_Guide.pdf	20-Aug-2020 11:30	1.5M	

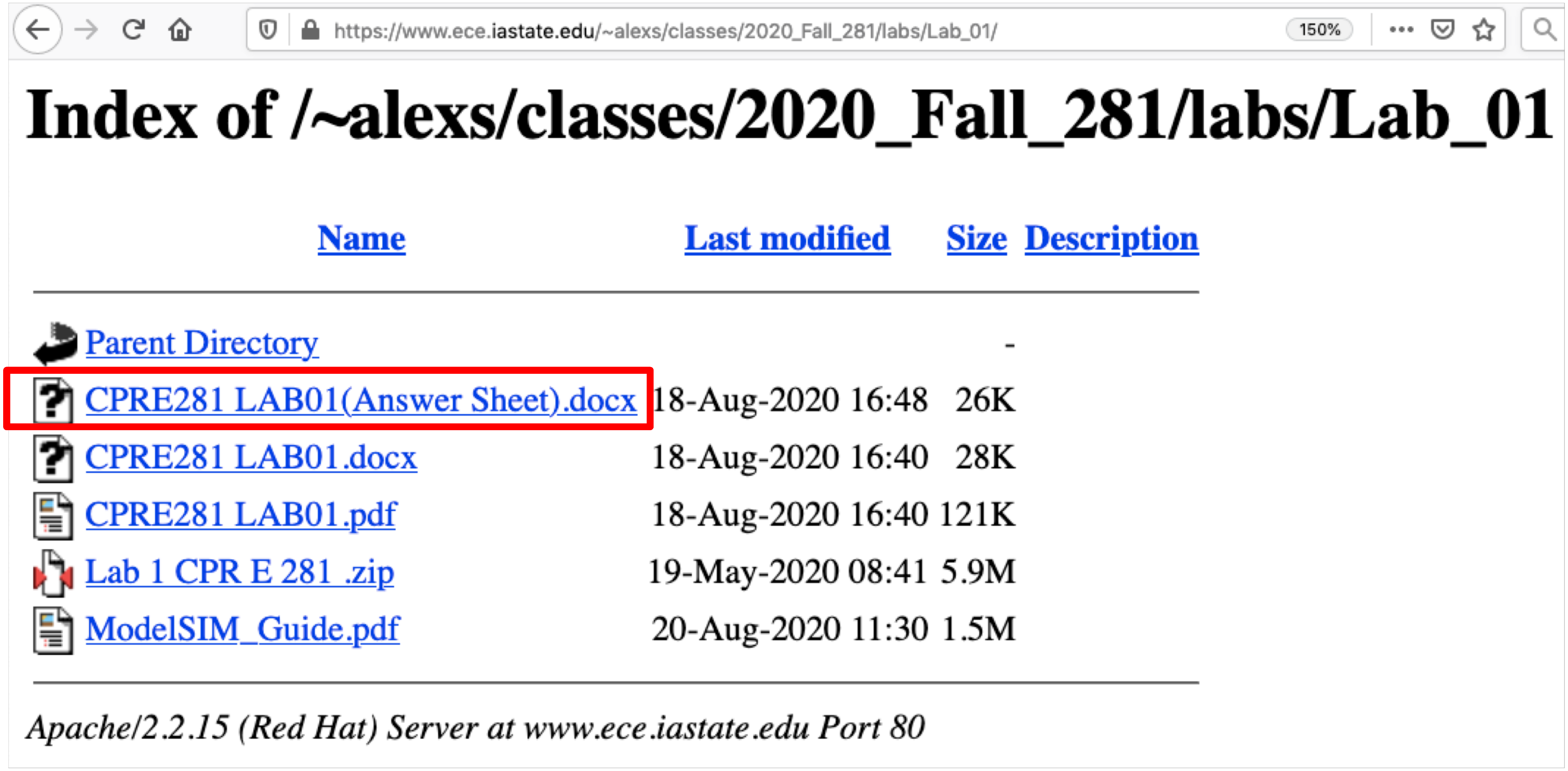
Apache/2.2.15 (Red Hat) Server at www.ece.iastate.edu Port 80



https://www.ece.iastate.edu/~alexs/classes/2020_Fall_281/labs/

Index of /~alexs/classes/2020_Fall_281/labs

Name	Last modified	Size	Description
Parent Directory		-	
Instructions/	21-Aug-2020 15:21	-	
Lab_01/	21-Aug-2020 15:22	-	
Lab_02/	18-Aug-2020 16:48	-	
Lab_03/	18-Aug-2020 16:51	-	
Lab_04/	18-Aug-2020 16:53	-	
Lab_05/	18-Aug-2020 16:56	-	
Lab_06/	18-Aug-2020 16:58	-	
Lab_07/	18-Aug-2020 16:59	-	
Lab_08/	18-Aug-2020 17:02	-	
Lab_09/	18-Aug-2020 17:05	-	
Lab_10/	18-Aug-2020 17:06	-	
Lab_11/	18-Aug-2020 17:08	-	
Lab_12/	18-Aug-2020 17:20	-	
Mini_Project/	18-Aug-2020 17:10	-	

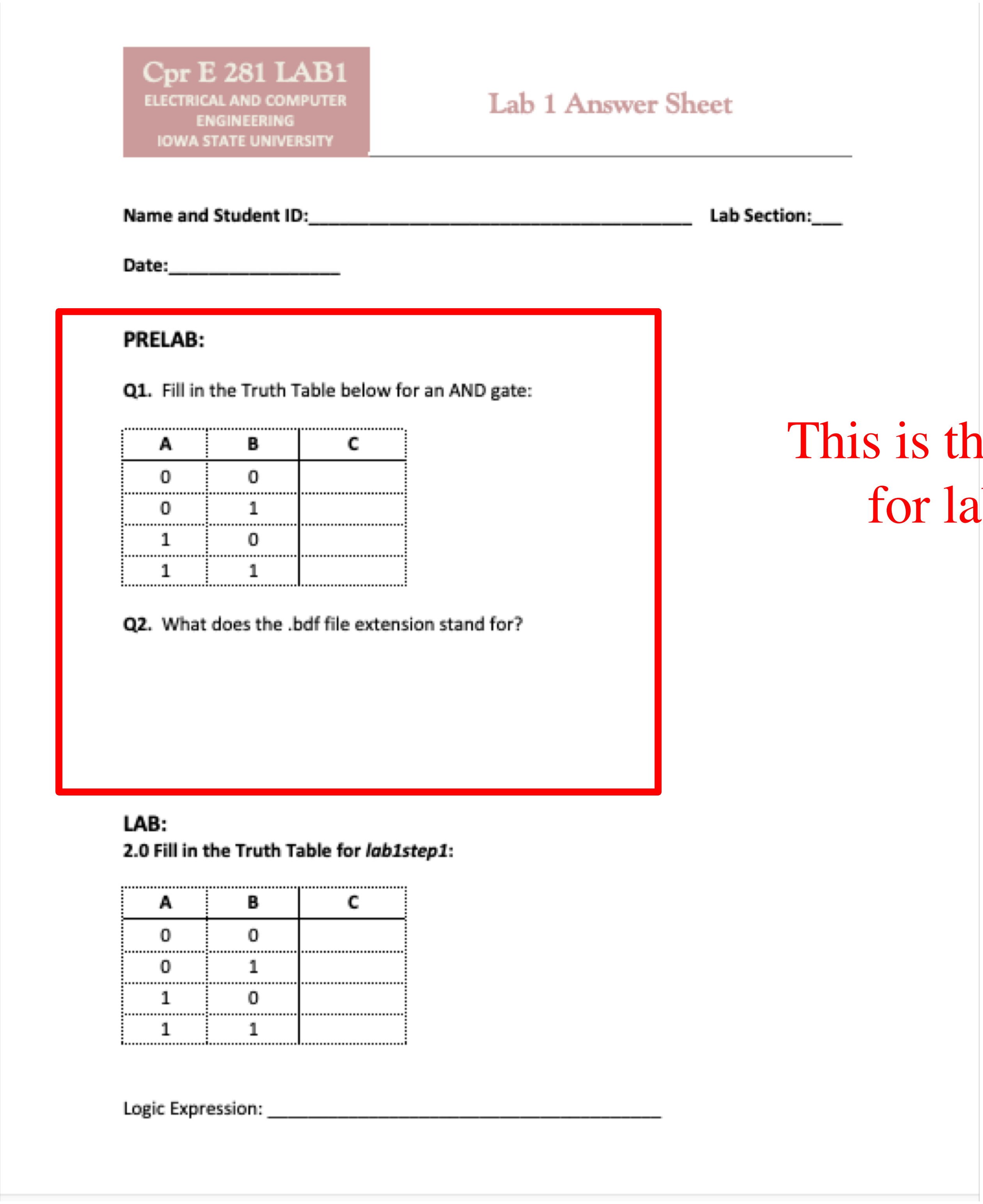


https://www.ece.iastate.edu/~alexs/classes/2020_Fall_281/labs/Lab_01/

Index of /~alexs/classes/2020_Fall_281/labs/Lab_01

Name	Last modified	Size	Description
Parent Directory		-	
CPRE281 LAB01(Answer Sheet).docx	18-Aug-2020 16:48	26K	
CPRE281 LAB01.docx	18-Aug-2020 16:40	28K	
CPRE281 LAB01.pdf	18-Aug-2020 16:40	121K	
Lab 1 CPR E 281 .zip	19-May-2020 08:41	5.9M	
ModelSIM_Guide.pdf	20-Aug-2020 11:30	1.5M	

Apache/2.2.15 (Red Hat) Server at www.ece.iastate.edu Port 80



Cpr E 281 LAB1
ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

Lab 1 Answer Sheet

Name and Student ID:____ Lab Section:___

Date:__________________

PRELAB:

Q1. Fill in the Truth Table below for an AND gate:

A	B	C
0	0	
0	1	
1	0	
1	1	

Q2. What does the .bdf file extension stand for?

LAB:

2.0 Fill in the Truth Table for *lab1step1*:

A	B	C
0	0	
0	1	
1	0	
1	1	

Logic Expression: ____

This is the prelab for lab #1

Cpr E 281 LAB1
ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

Lab 1 Answer Sheet

4.0 Fill in the Truth Table for *lab1step2*:

W	X	Y	Z
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

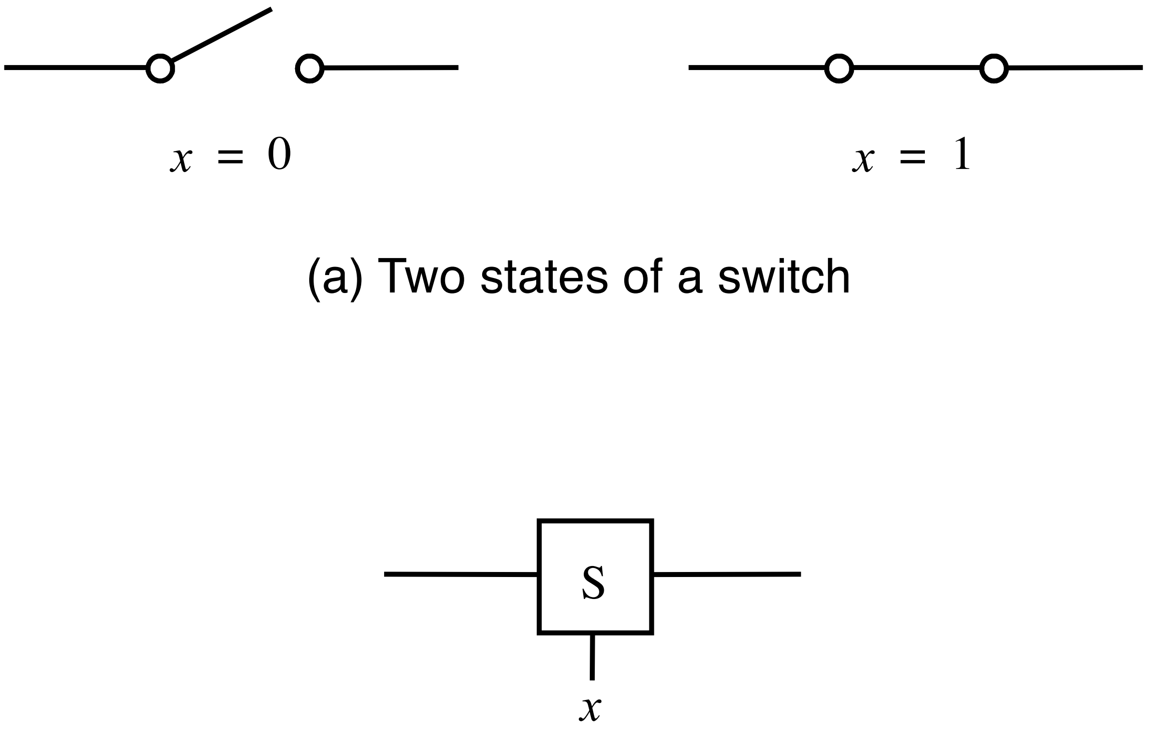
Logic Expression: ____

4.0 Fill in the Truth Table for *lab1step3*:

A	B	C	F

Logic Expression: ____

A Binary Switch

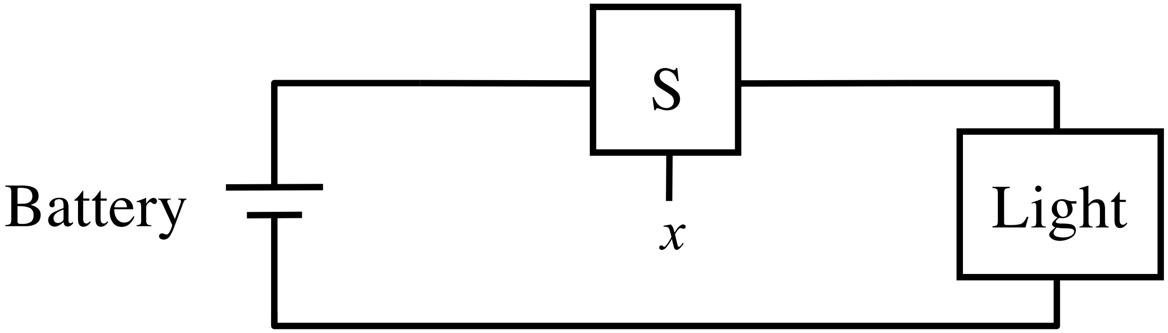


(a) Two states of a switch

(b) Symbol for a switch

[Figure 2.1 from the textbook]

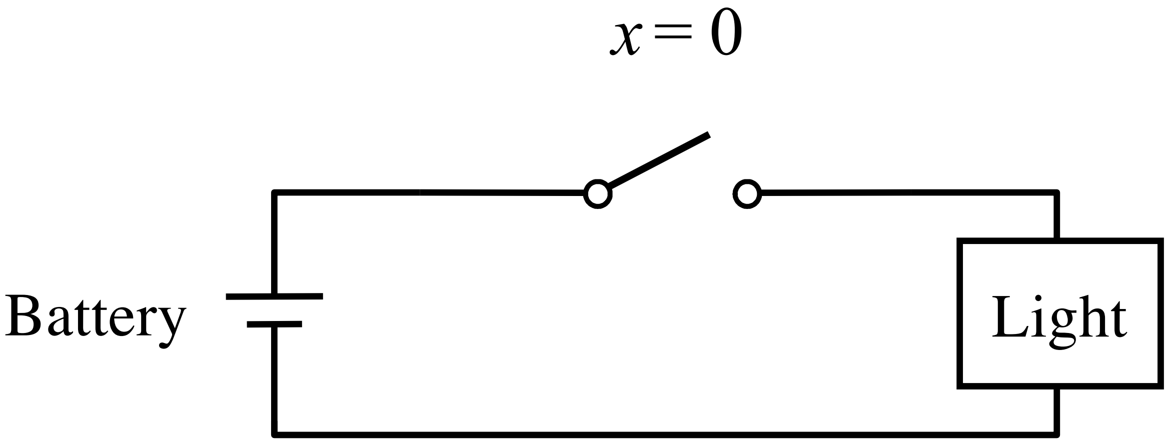
A Light Controlled by a Switch



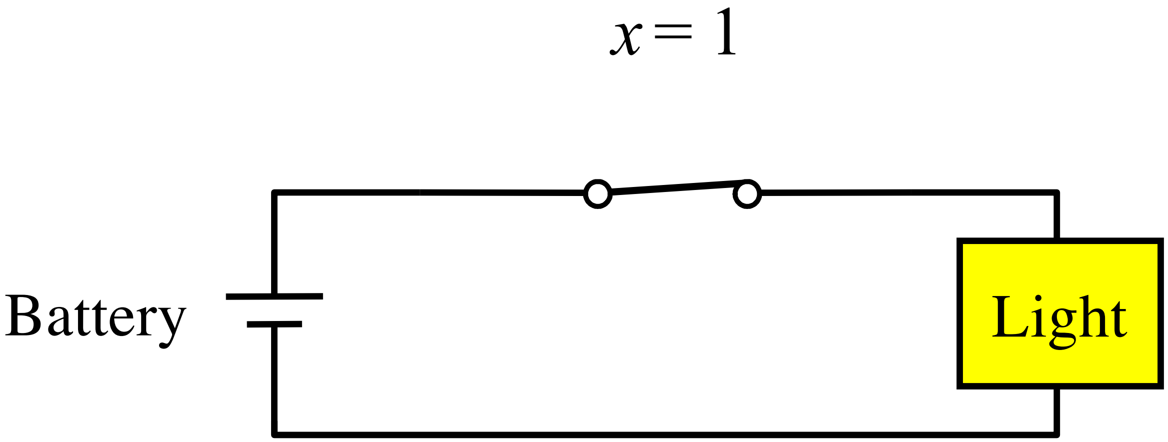
(a) Simple connection to a battery

[Figure 2.2a from the textbook]

A Light Controlled by a Switch



A Light Controlled by a Switch

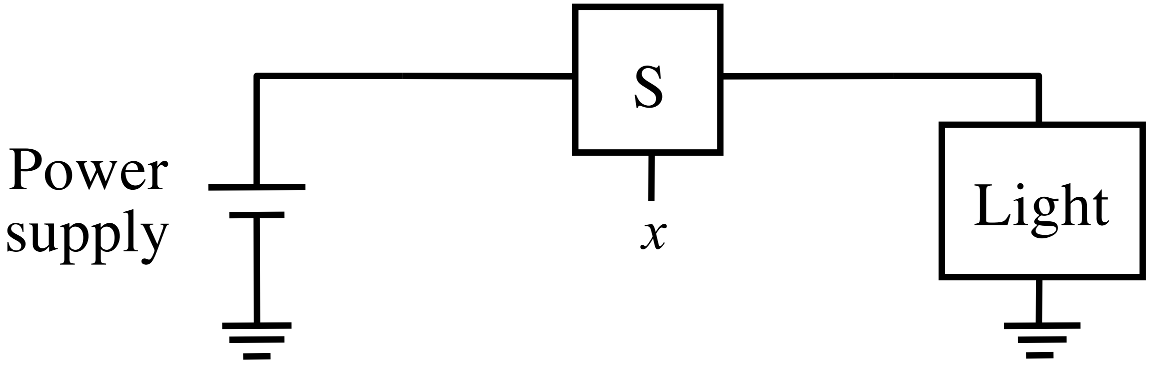


$x = 1$

Battery

Light

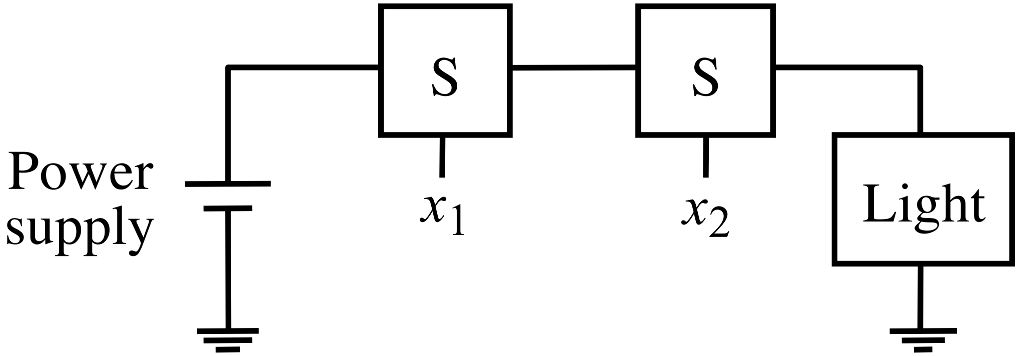
A Light Controlled by a Switch



(b) Using a ground connection as the return path

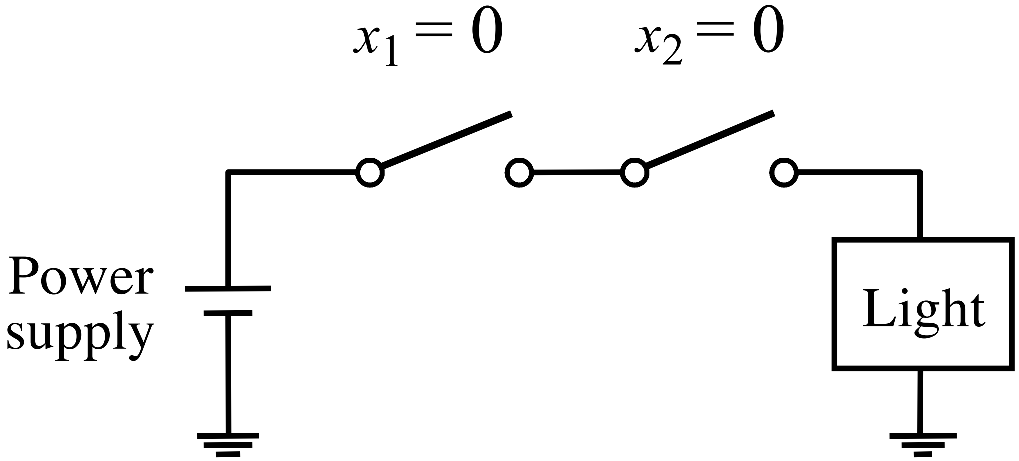
[Figure 2.2b from the textbook]

The Logical AND function
(series connection of the switches)



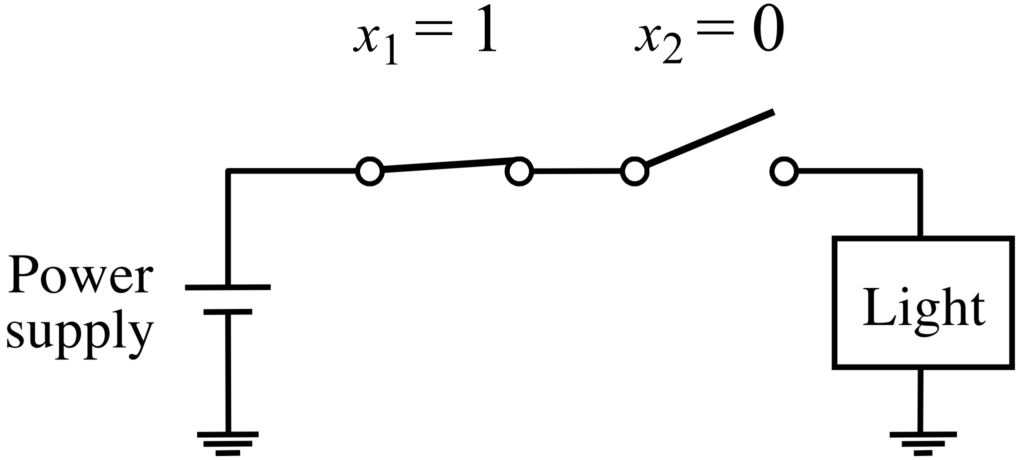
[Figure 2.3a from the textbook]

The Logical AND function
(series connection of the switches)

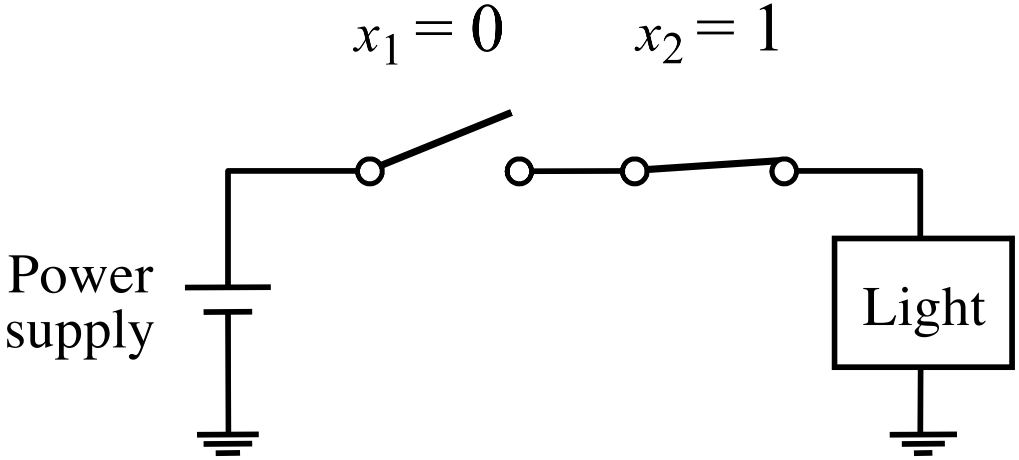


The Logical AND function

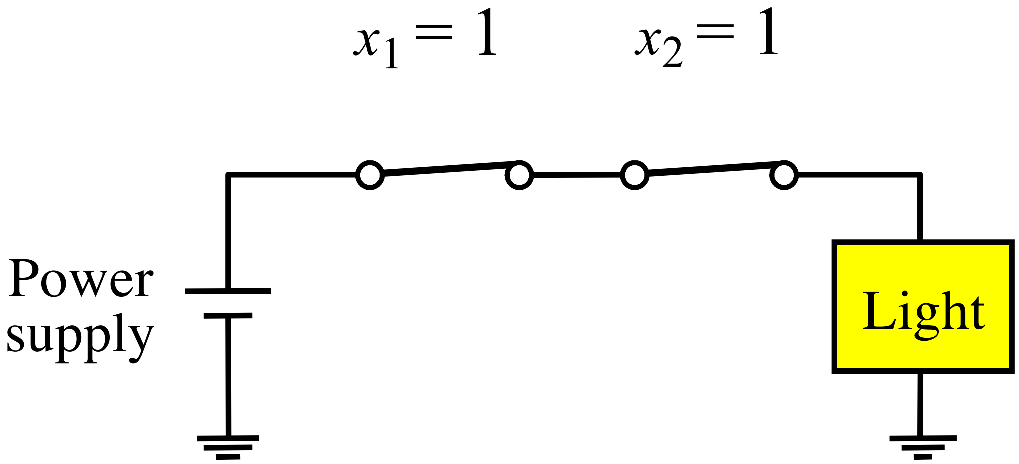
(series connection of the switches)



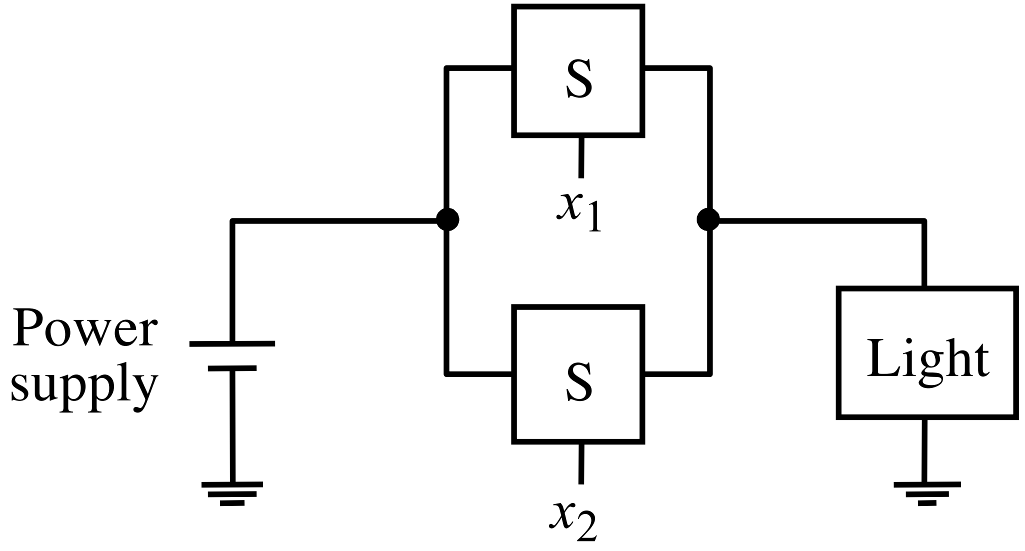
The Logical AND function
(series connection of the switches)



The Logical AND function
(series connection of the switches)

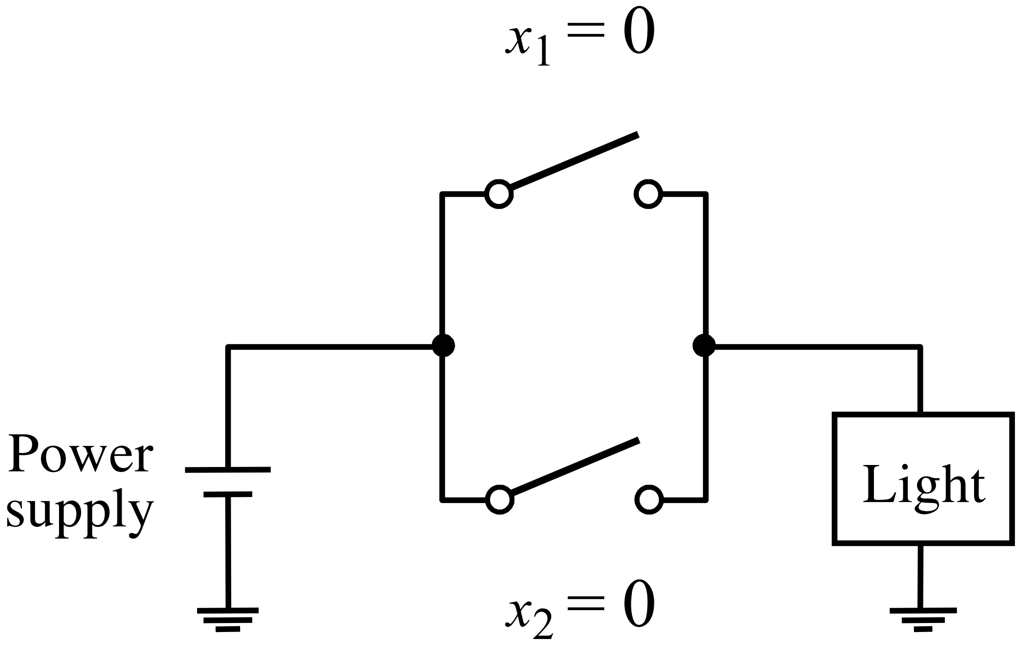


The Logical OR function
(parallel connection of the switches)

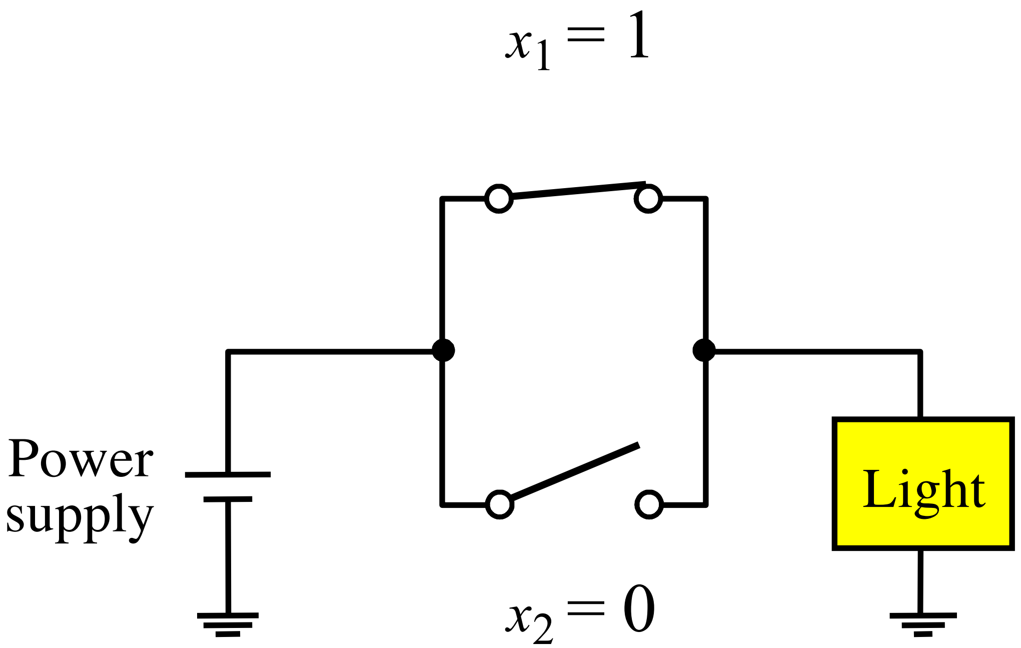


[Figure 2.3b from the textbook]

The Logical OR function
(parallel connection of the switches)

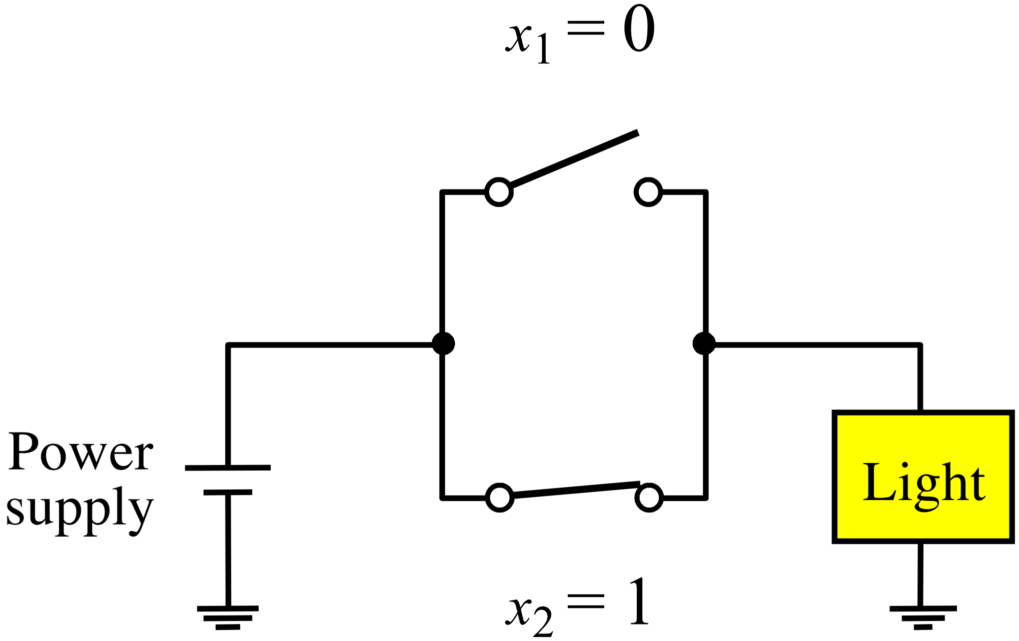


The Logical OR function
(parallel connection of the switches)

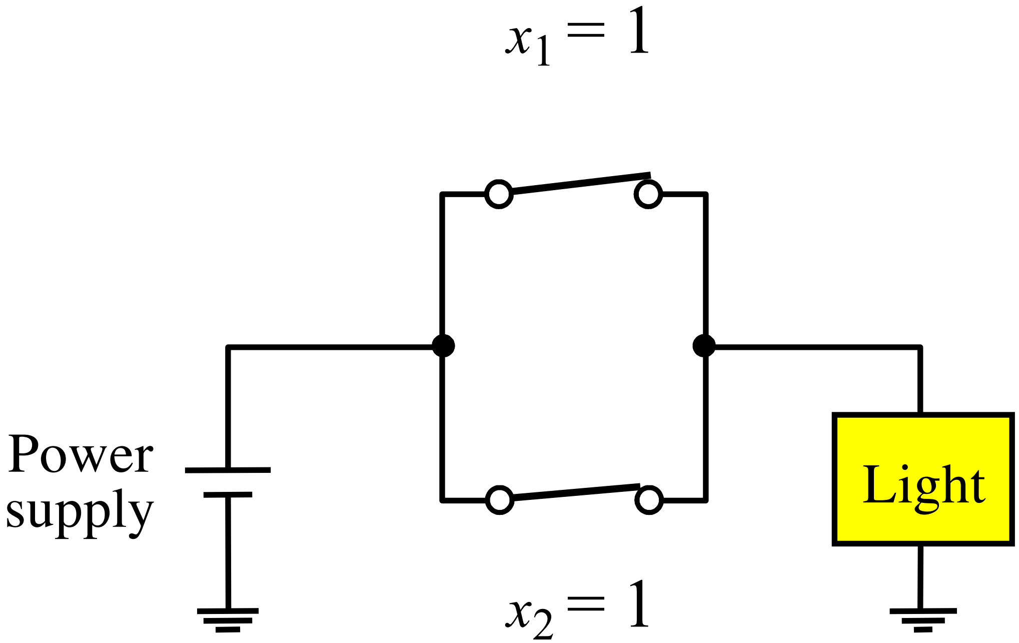


The Logical OR function

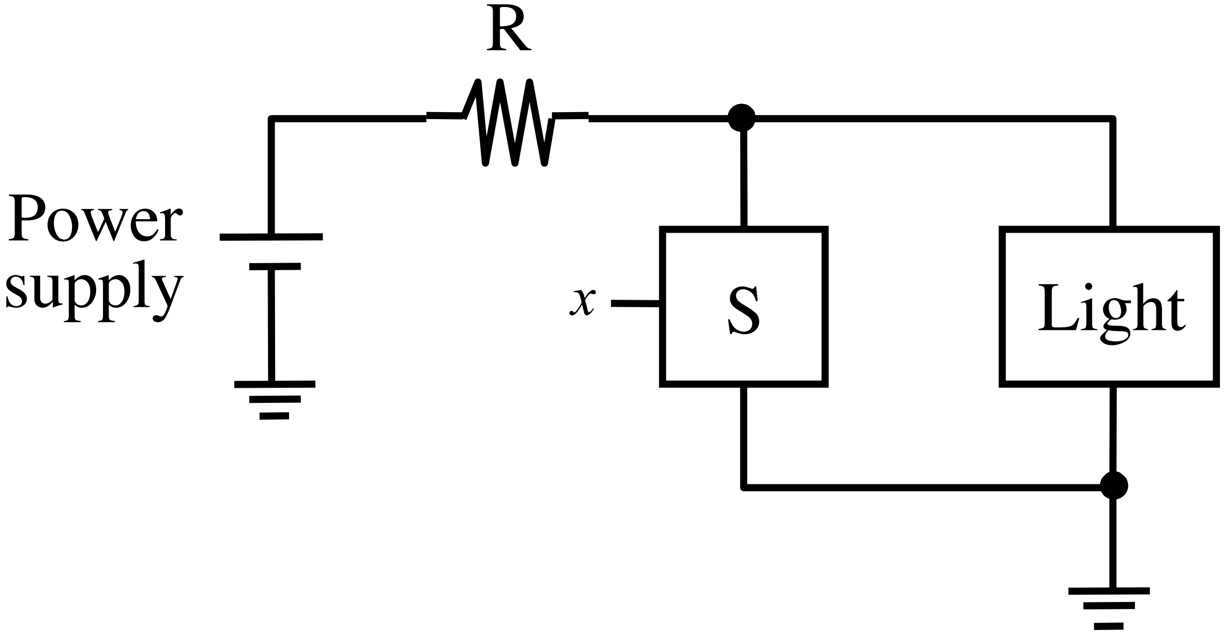
(parallel connection of the switches)



The Logical OR function
(parallel connection of the switches)

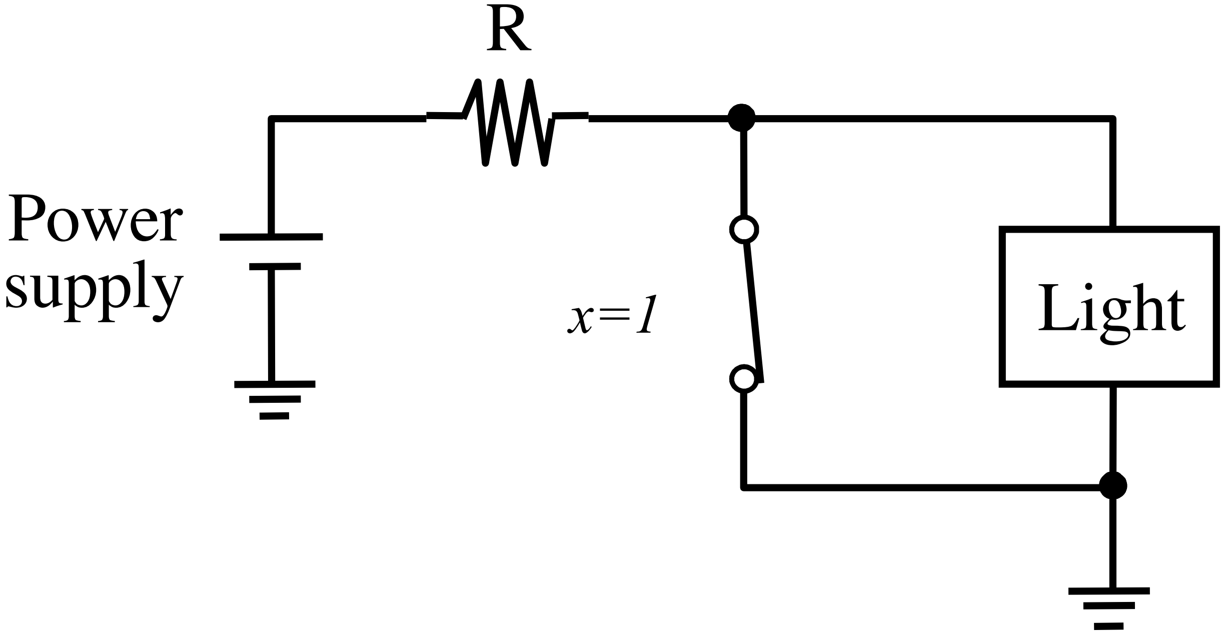


An Inverting Circuit

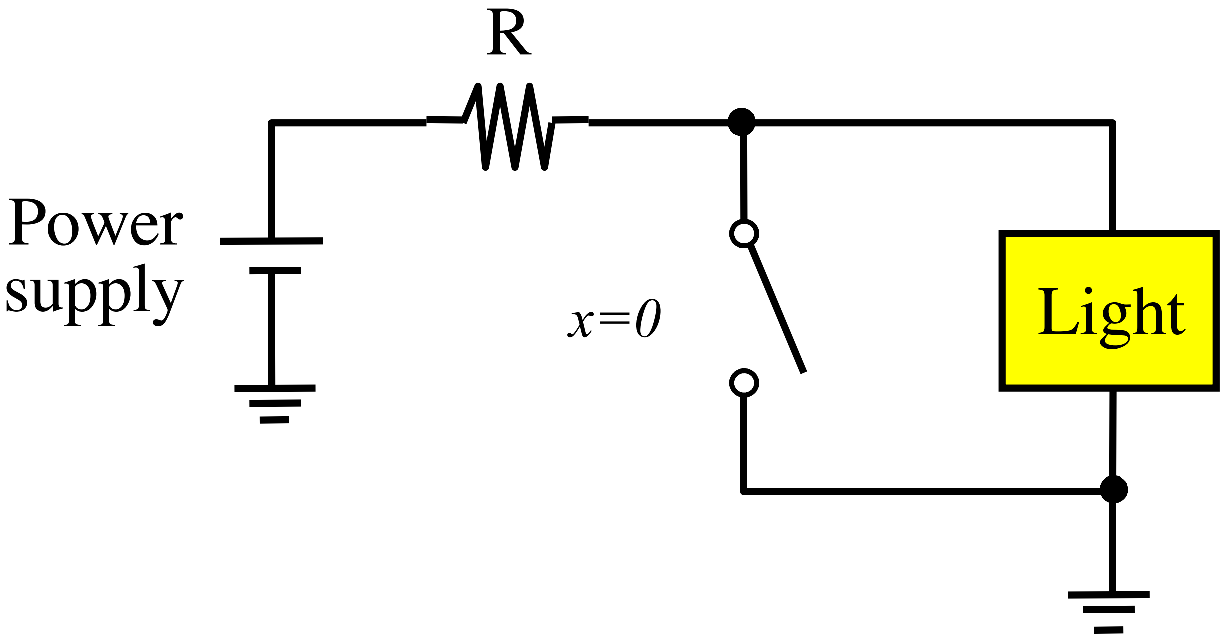


[Figure 2.5 from the textbook]

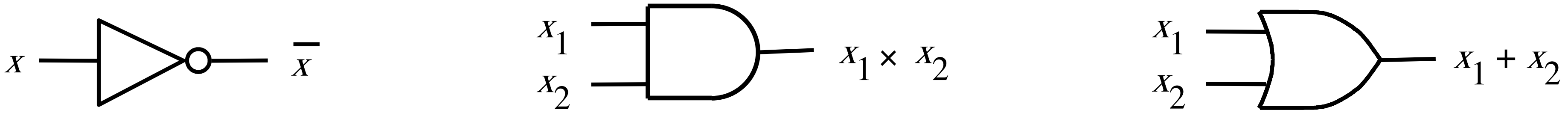
An Inverting Circuit



An Inverting Circuit



The Three Basic Logic Gates



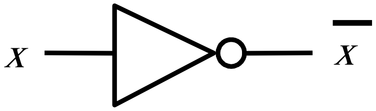
NOT gate

AND gate

OR gate

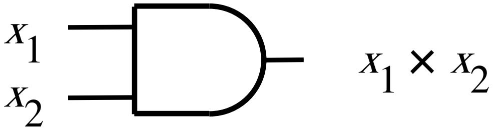
[Figure 2.8 from the textbook]

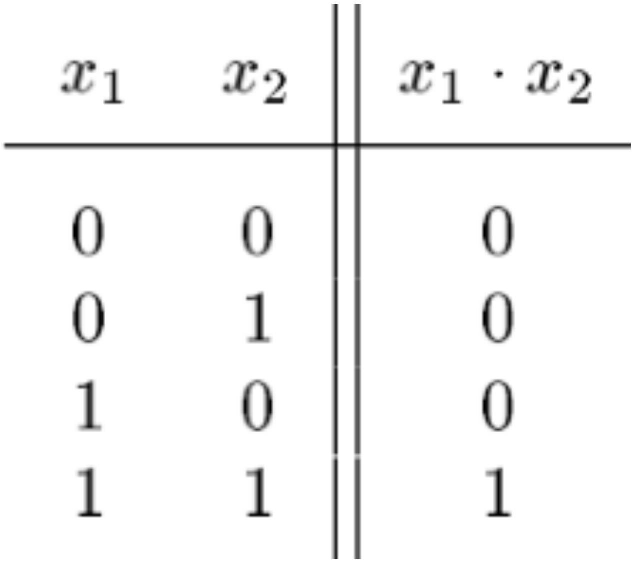
Truth Table for NOT



x	$\overline{x}$
0	1
1	0

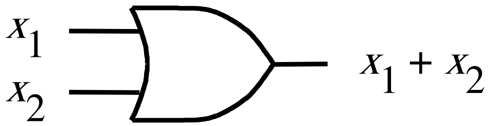
Truth Table for AND





x_1	x_2	$x_1 \cdot x_2$
0	0	0
0	1	0
1	0	0
1	1	1

Truth Table for OR



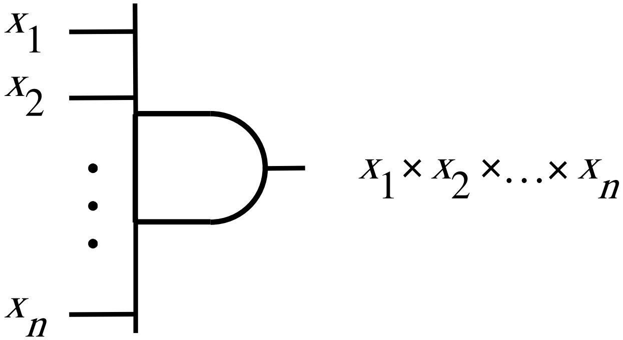
x_1	x_2	$x_1 + x_2$
0	0	0
0	1	1
1	0	1
1	1	1

Truth Tables for AND and OR

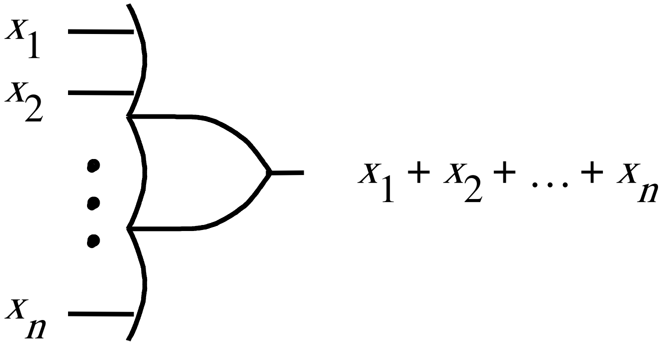
x_1	x_2	$x_1 \ x_2$	$x_1 + x_2$
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	1
		AND	OR

[Figure 2.6b from the textbook]

Logic Gates with n Inputs



AND gate



OR gate

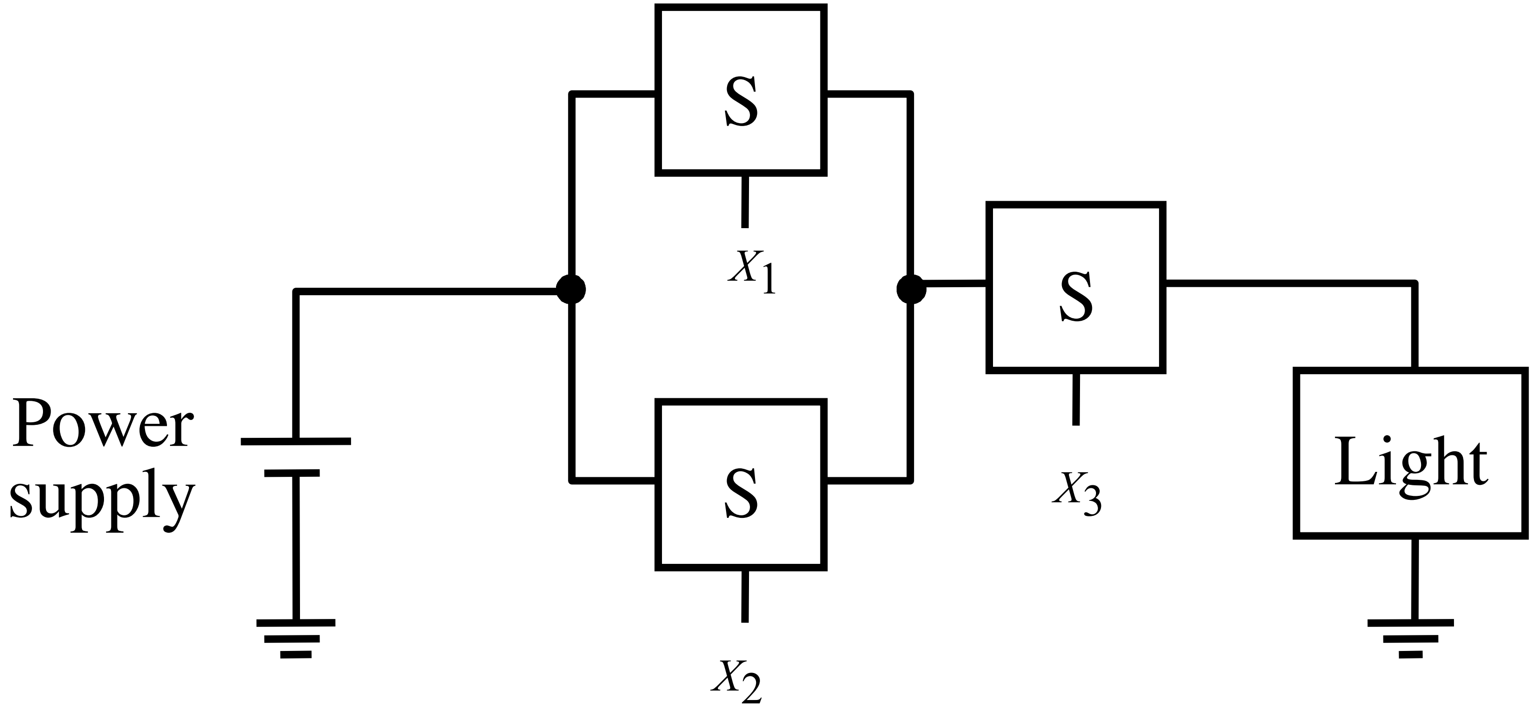
[Figure 2.8 from the textbook]

Truth Table for 3-input AND and OR

x_1	x_2	x_3	$x_1 \; x_2 \; x_3$	$x_1 + x_2 + x_3$
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	0	1
1	0	0	0	1
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

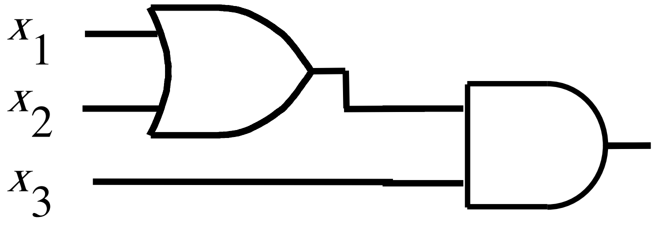
[Figure 2.7 from the textbook]

A series-parallel connection of the switches



[Figure 2.4 from the textbook]

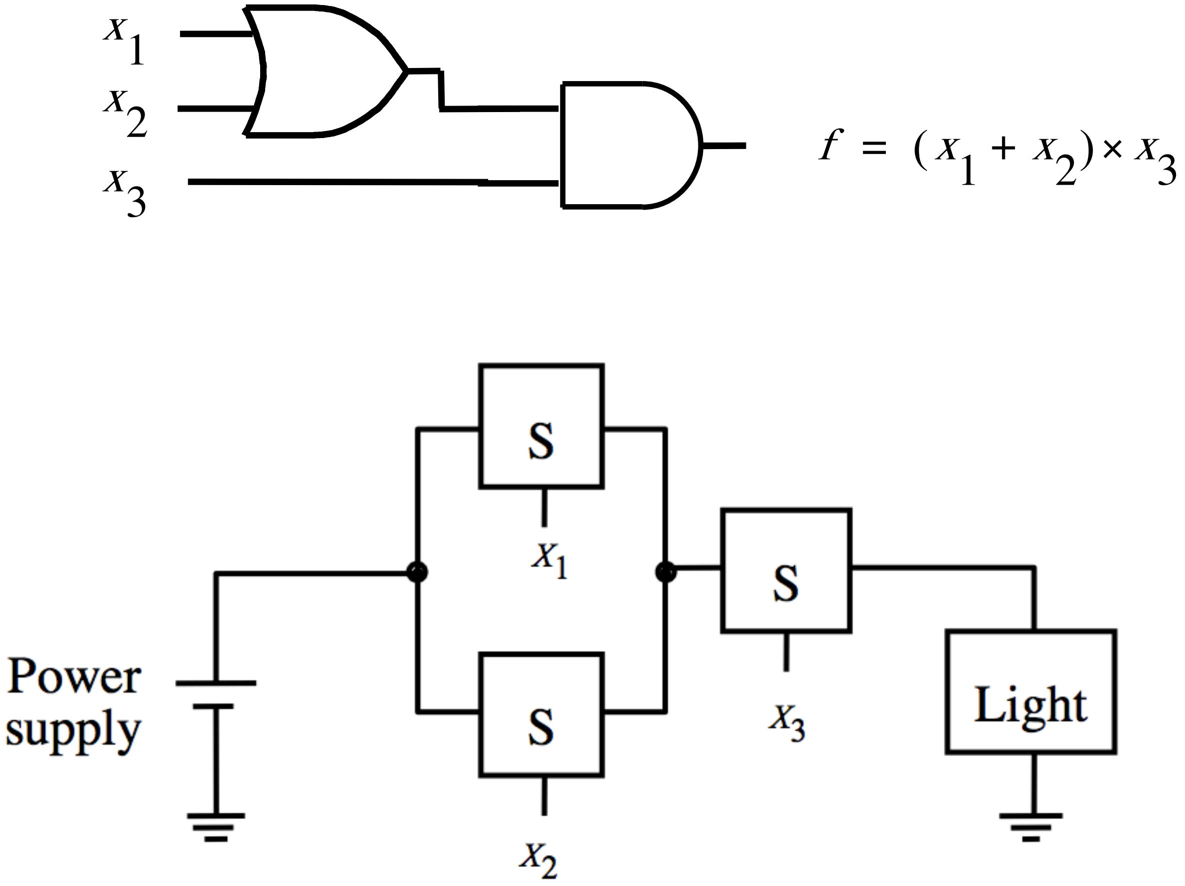
Example of a Logic Circuit Implemented with Logic Gates



$f = (x_1 + x_2) \times x_3$

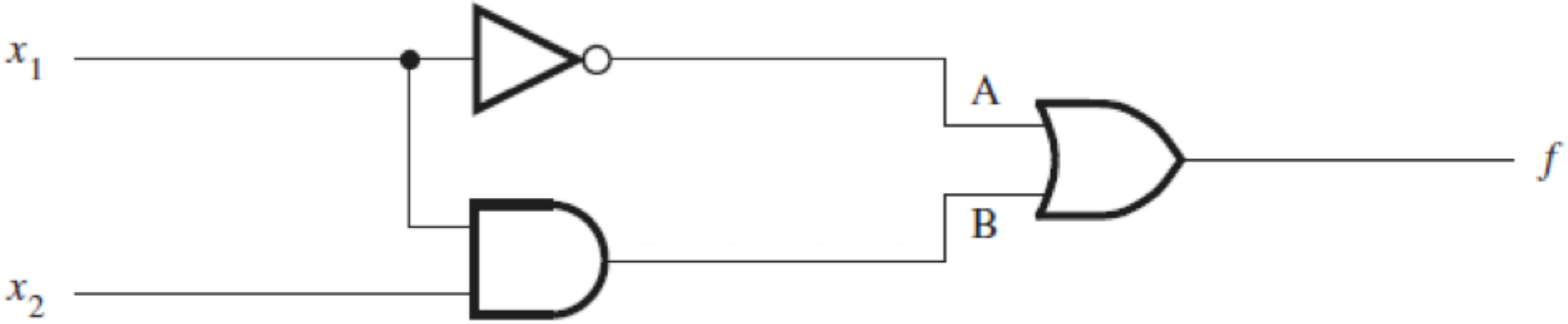
[Figure 2.8 from the textbook]

Example of a Logic Circuit Implemented with Logic Gates


$$f = (x_1 + x_2) \times x_3$$

[Figure 2.8 from the textbook]

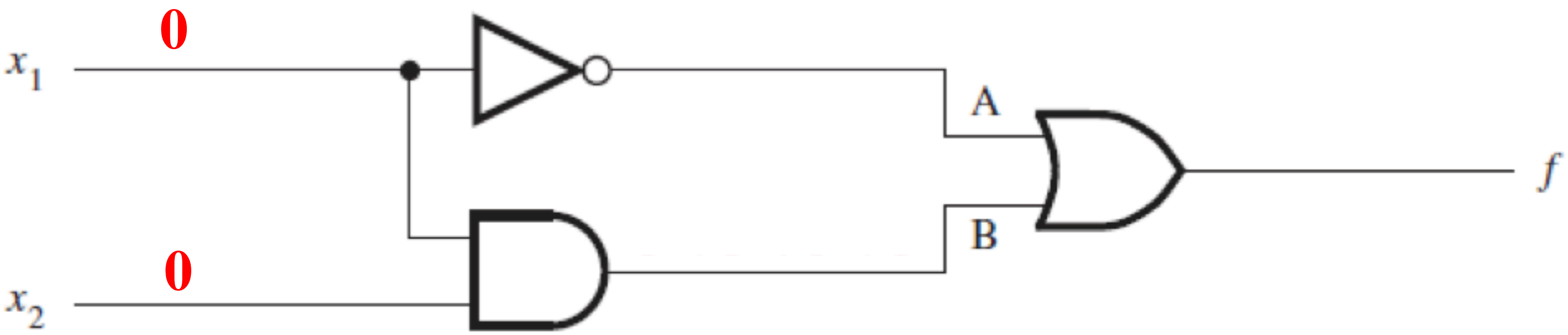
Circuit Analysis



(a) Network that implements $f = \bar{x}_1 + x_1 \cdot x_2$

[Figure 2.10 from the textbook]

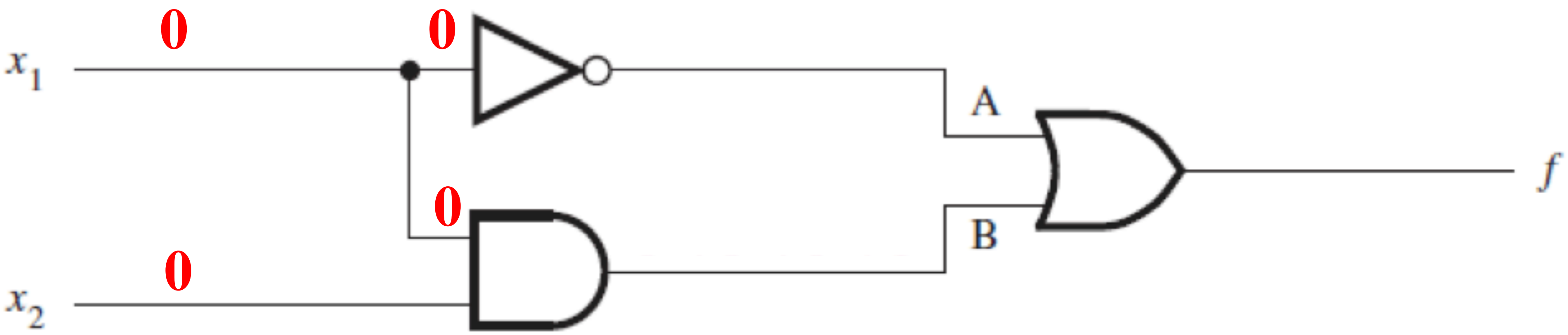
Circuit Analysis



(a) Network that implements $f = \bar{x}_1 + x_1 \cdot x_2$

[Figure 2.10 from the textbook]

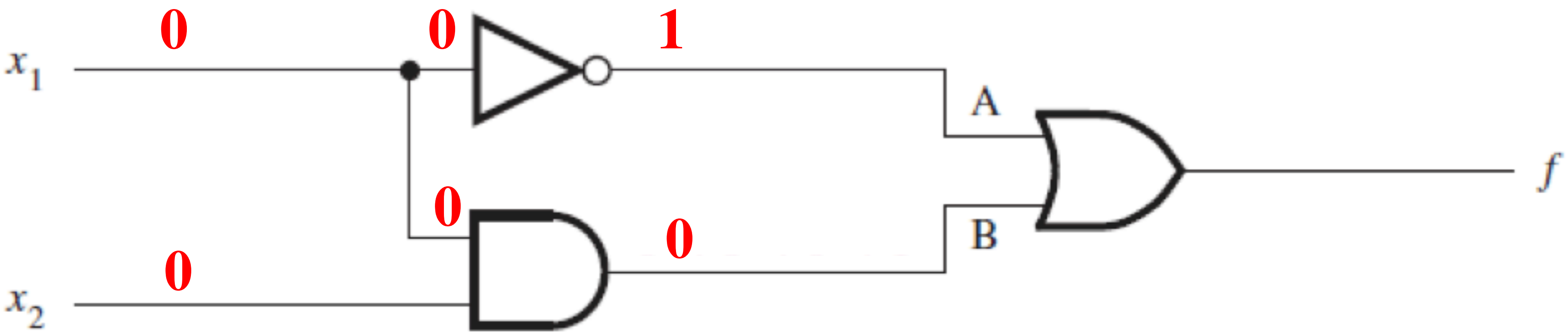
Circuit Analysis



(a) Network that implements $f = \bar{x}_1 + x_1 \cdot x_2$

[Figure 2.10 from the textbook]

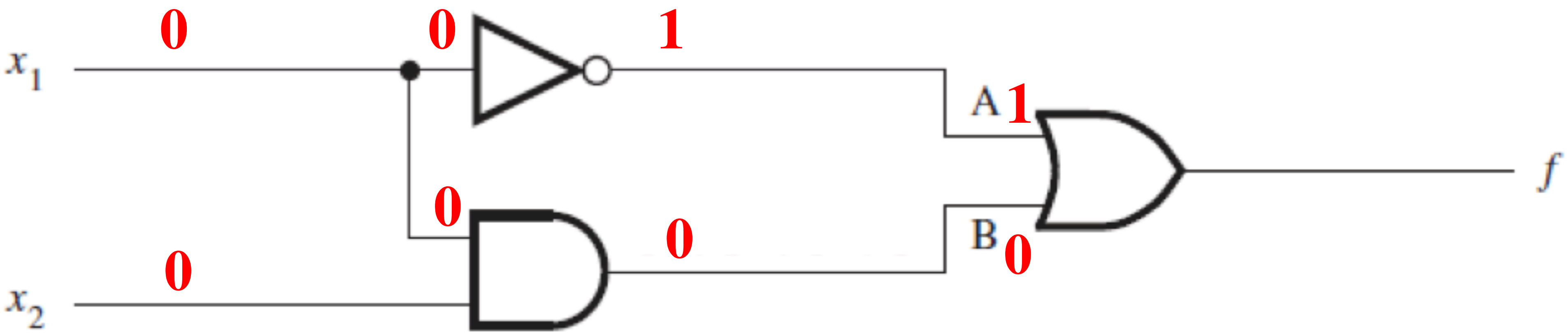
Circuit Analysis



(a) Network that implements $f = \bar{x}_1 + x_1 \cdot x_2$

[Figure 2.10 from the textbook]

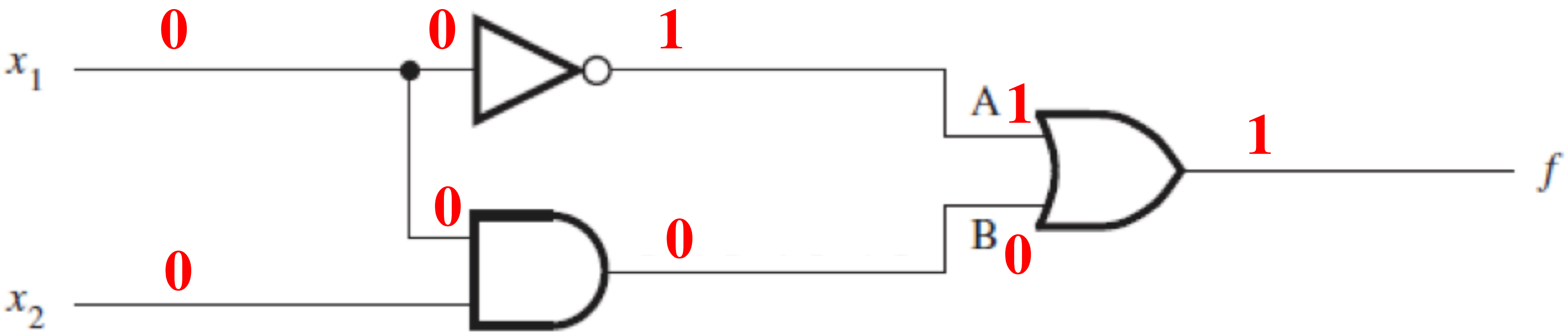
Circuit Analysis



(a) Network that implements $f = \bar{x}_1 + x_1 \cdot x_2$

[Figure 2.10 from the textbook]

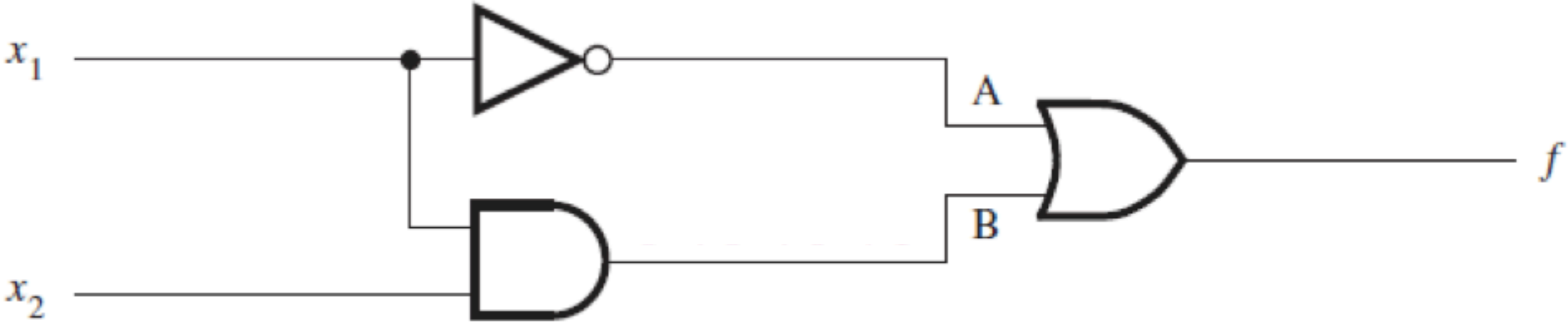
Circuit Analysis



(a) Network that implements $f = \bar{x}_1 + x_1 \cdot x_2$

[Figure 2.10 from the textbook]

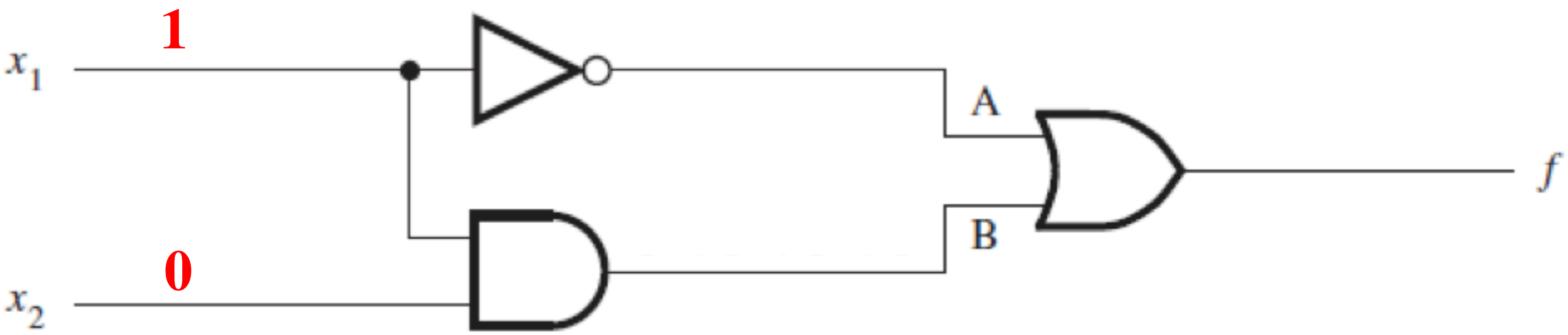
Circuit Analysis



(a) Network that implements $f = \bar{x}_1 + x_1 \cdot x_2$

[Figure 2.10 from the textbook]

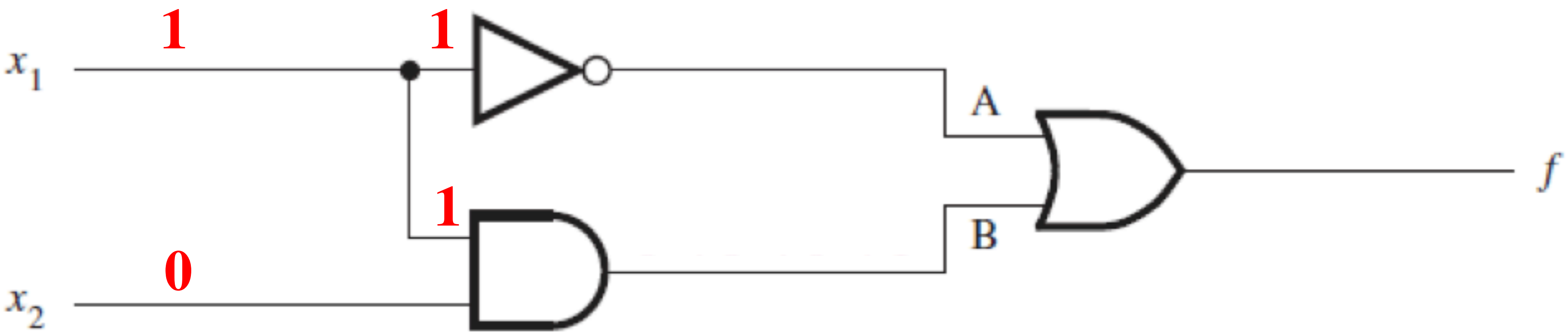
Circuit Analysis



(a) Network that implements $f = \bar{x}_1 + x_1 \cdot x_2$

[Figure 2.10 from the textbook]

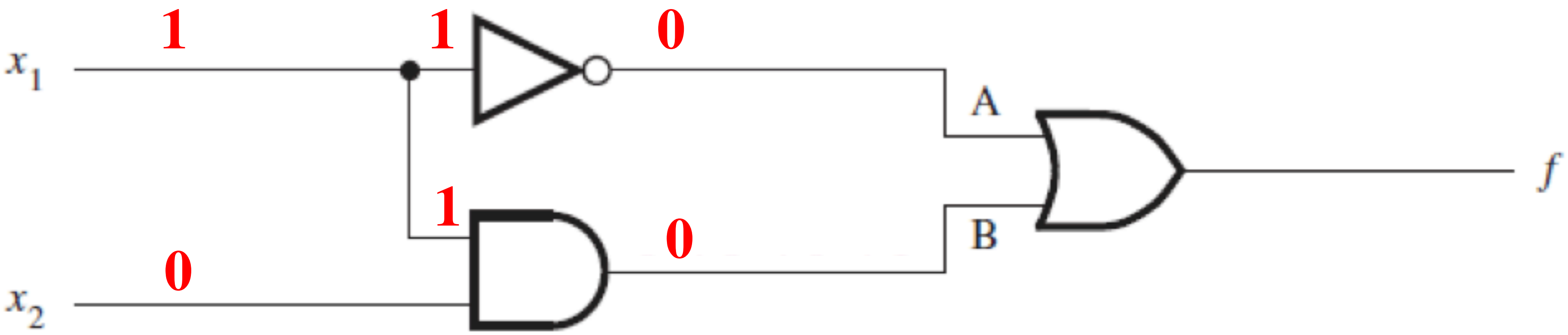
Circuit Analysis



(a) Network that implements $f = \bar{x}_1 + x_1 \cdot x_2$

[Figure 2.10 from the textbook]

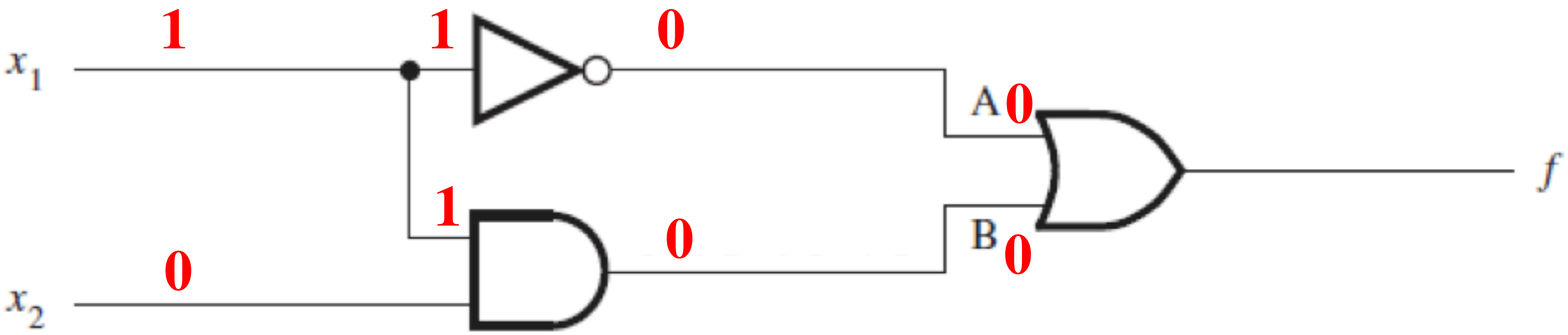
Circuit Analysis



(a) Network that implements $f = \bar{x}_1 + x_1 \cdot x_2$

[Figure 2.10 from the textbook]

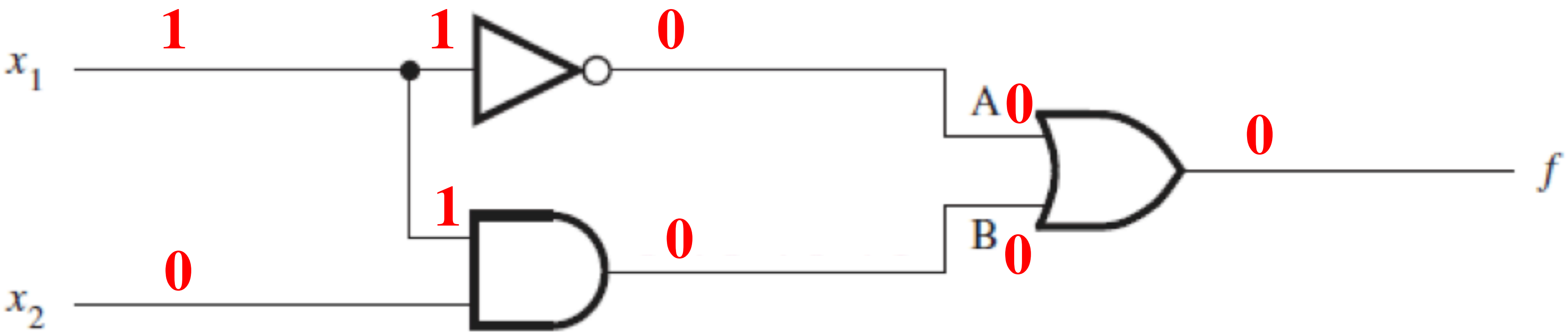
Circuit Analysis



(a) Network that implements $f = \bar{x}_1 + x_1 \cdot x_2$

[Figure 2.10 from the textbook]

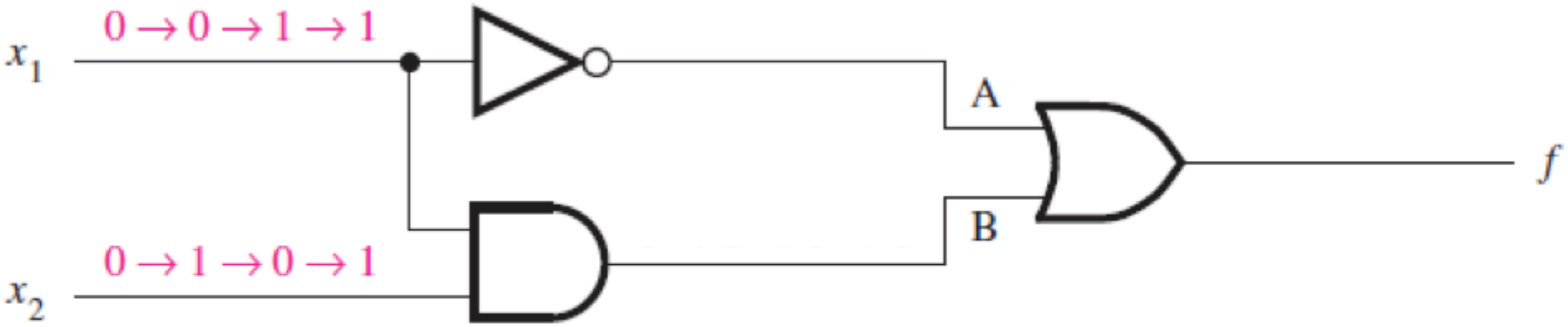
Circuit Analysis



(a) Network that implements $f = \bar{x}_1 + x_1 \cdot x_2$

[Figure 2.10 from the textbook]

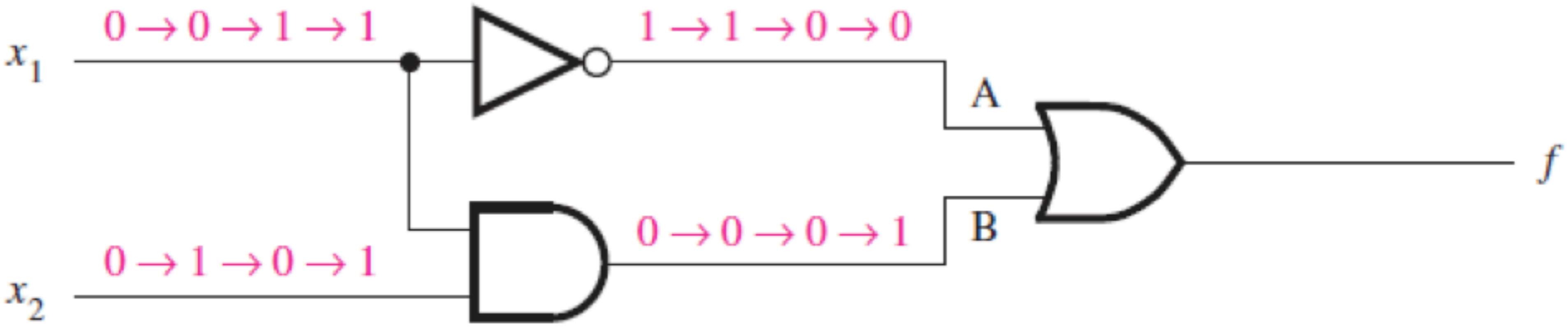
Circuit Analysis with Sequential Inputs



(a) Network that implements $f = \bar{x}_1 + x_1 \cdot x_2$

[Figure 2.10 from the textbook]

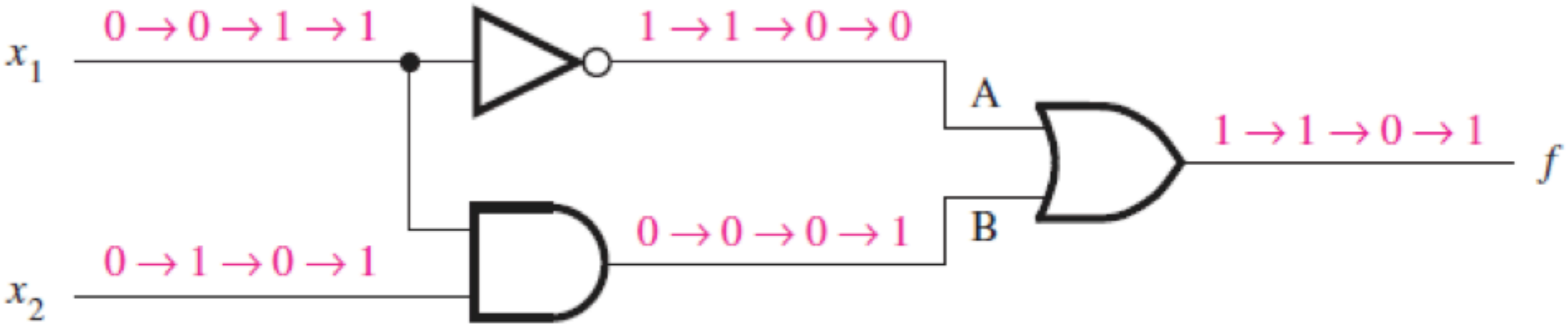
Circuit Analysis with Sequential Inputs



(a) Network that implements $f = \bar{x}_1 + x_1 \cdot x_2$

[Figure 2.10 from the textbook]

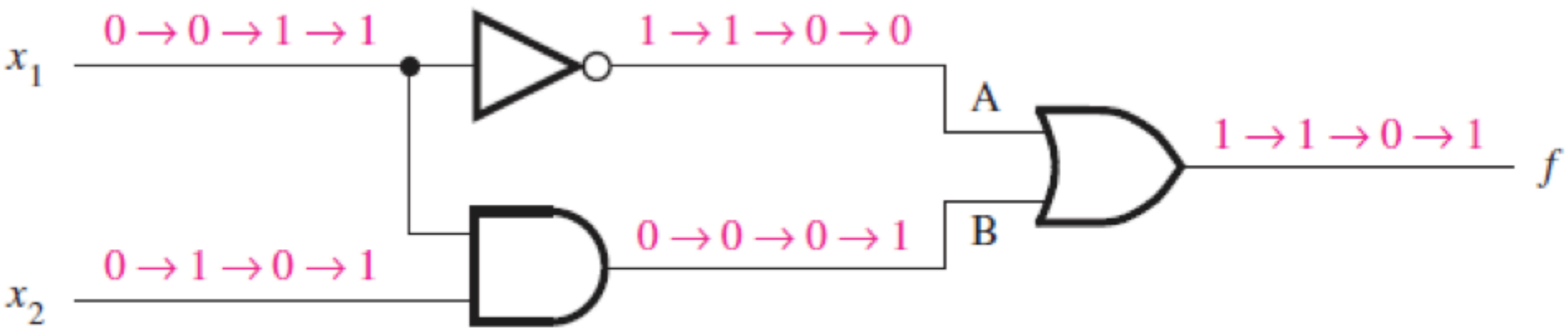
Circuit Analysis with Sequential Inputs


x_1
$0 \rightarrow 0 \rightarrow 1 \rightarrow 1$
$1 \rightarrow 1 \rightarrow 0 \rightarrow 0$
A
$1 \rightarrow 1 \rightarrow 0 \rightarrow 1$
f
$0 \rightarrow 0 \rightarrow 0 \rightarrow 1$
B
$0 \rightarrow 1 \rightarrow 0 \rightarrow 1$
x_2

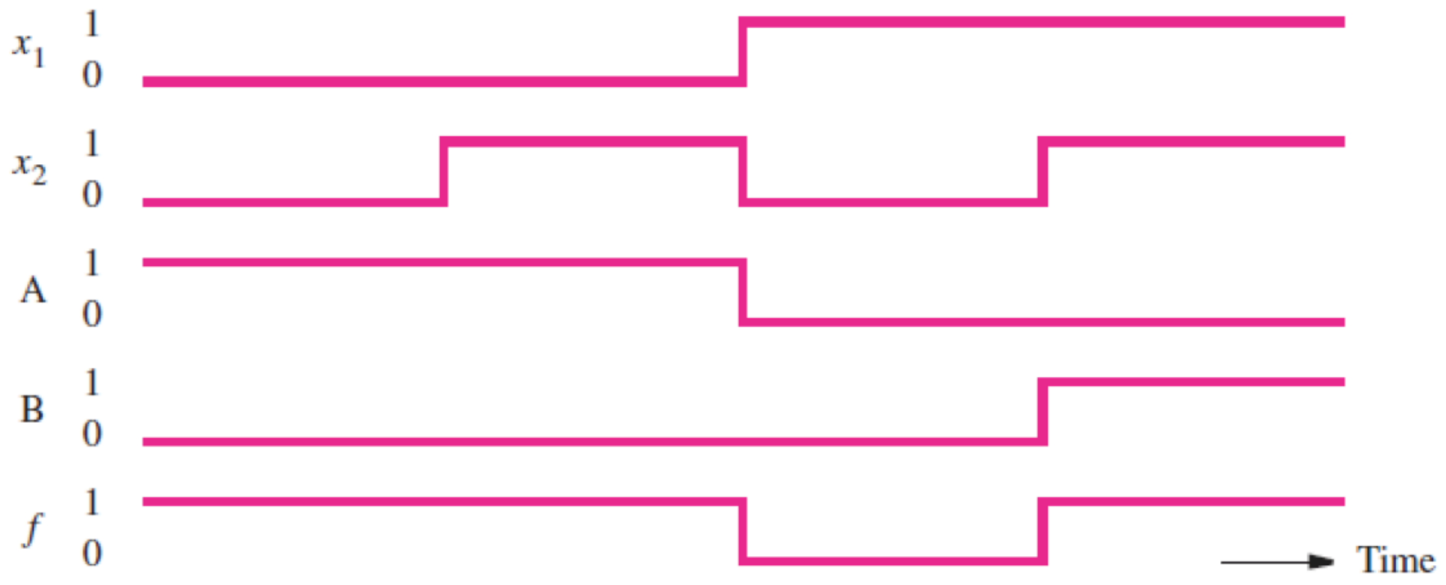
(a) Network that implements $f = \bar{x}_1 + x_1 \cdot x_2$

[Figure 2.10 from the textbook]

Circuit Analysis with Sequential Inputs

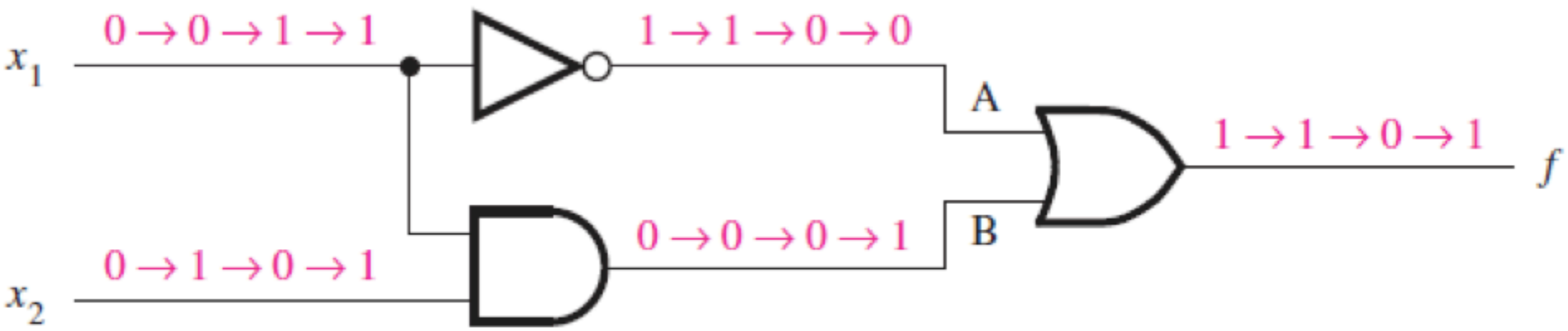

x_1
$0 \rightarrow 0 \rightarrow 1 \rightarrow 1$
$1 \rightarrow 1 \rightarrow 0 \rightarrow 0$
A
$1 \rightarrow 1 \rightarrow 0 \rightarrow 1$
f
B
$0 \rightarrow 0 \rightarrow 0 \rightarrow 1$
$0 \rightarrow 1 \rightarrow 0 \rightarrow 1$
x_2

(a) Network that implements $f = \bar{x}_1 + x_1 \cdot x_2$

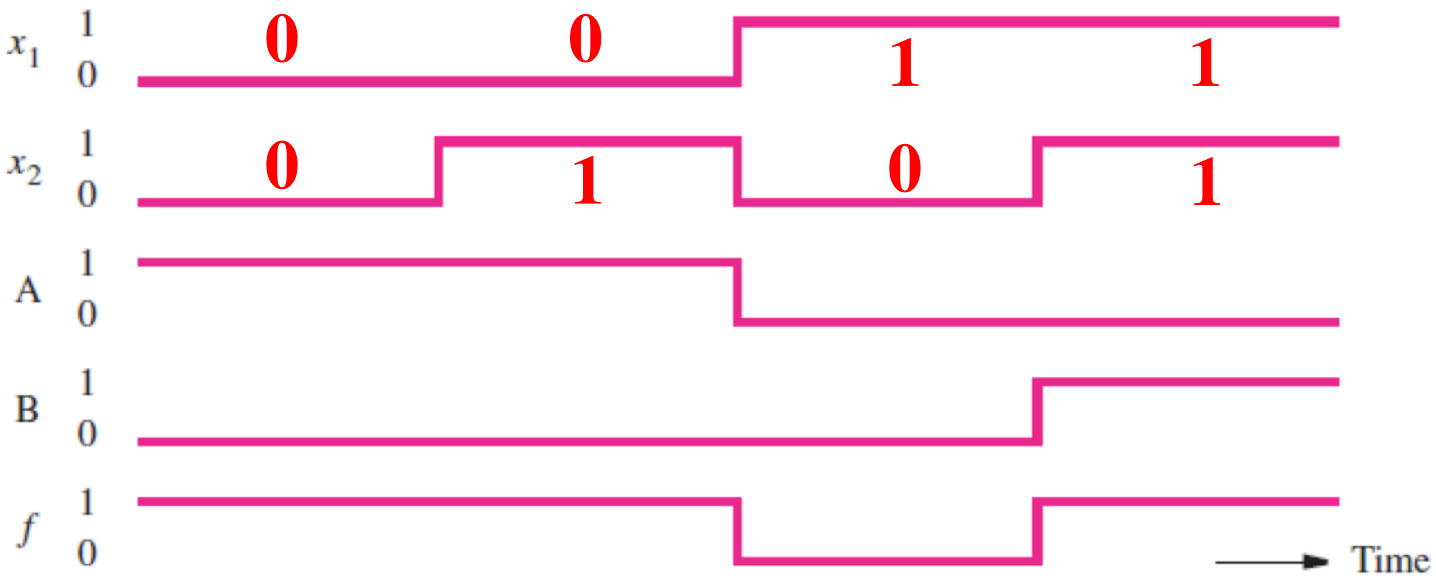


[Figure 2.10 from the textbook]

Circuit Analysis with Sequential Inputs

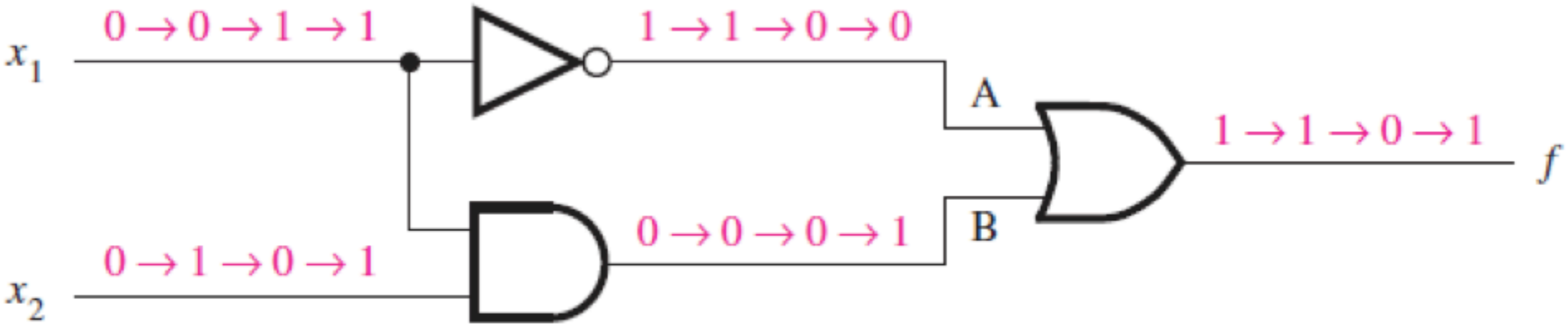


(a) Network that implements $f = \bar{x}_1 + x_1 \cdot x_2$

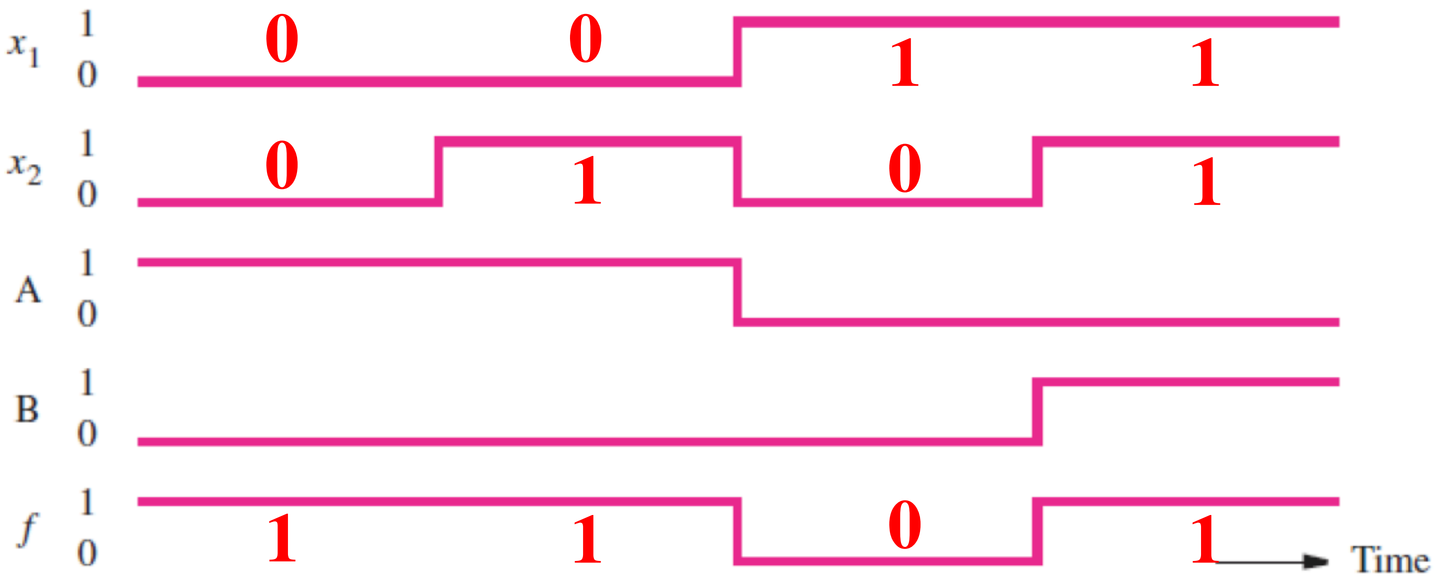


[Figure 2.10 from the textbook]

Circuit Analysis with Sequential Inputs

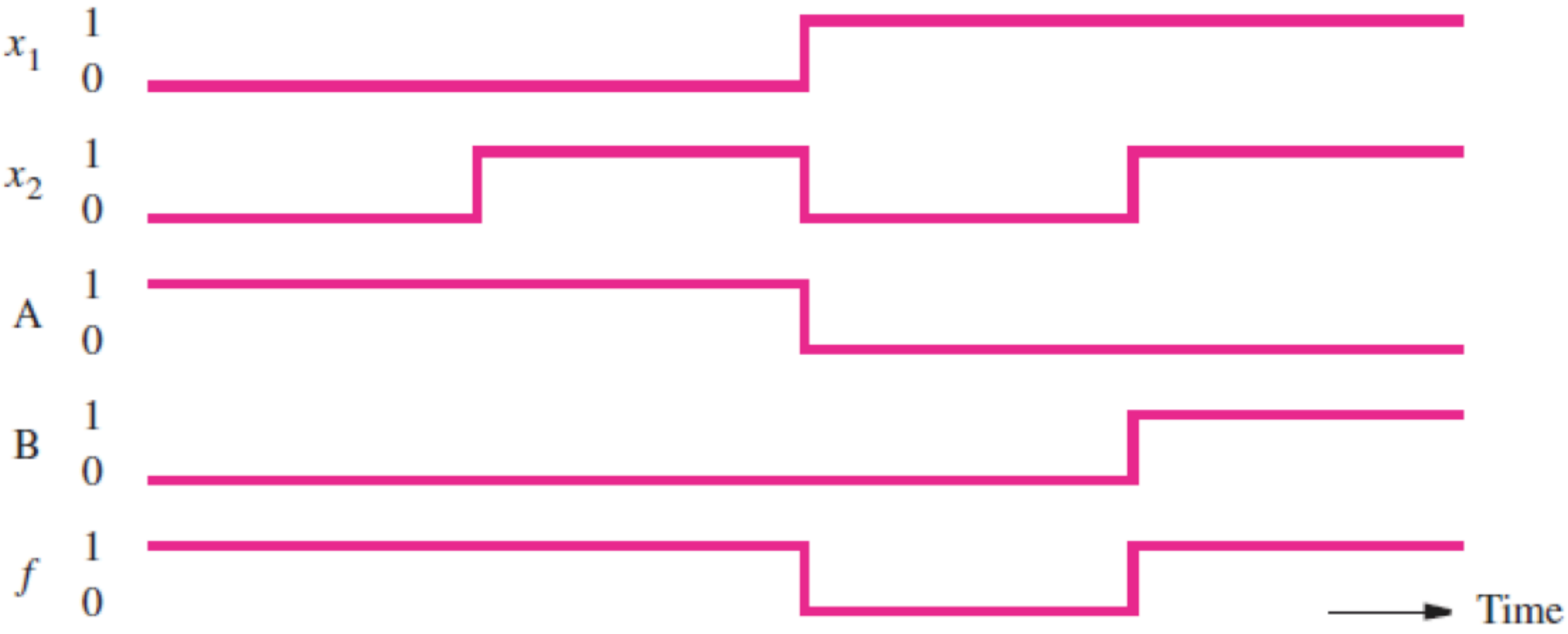


(a) Network that implements $f = \bar{x}_1 + x_1 \cdot x_2$



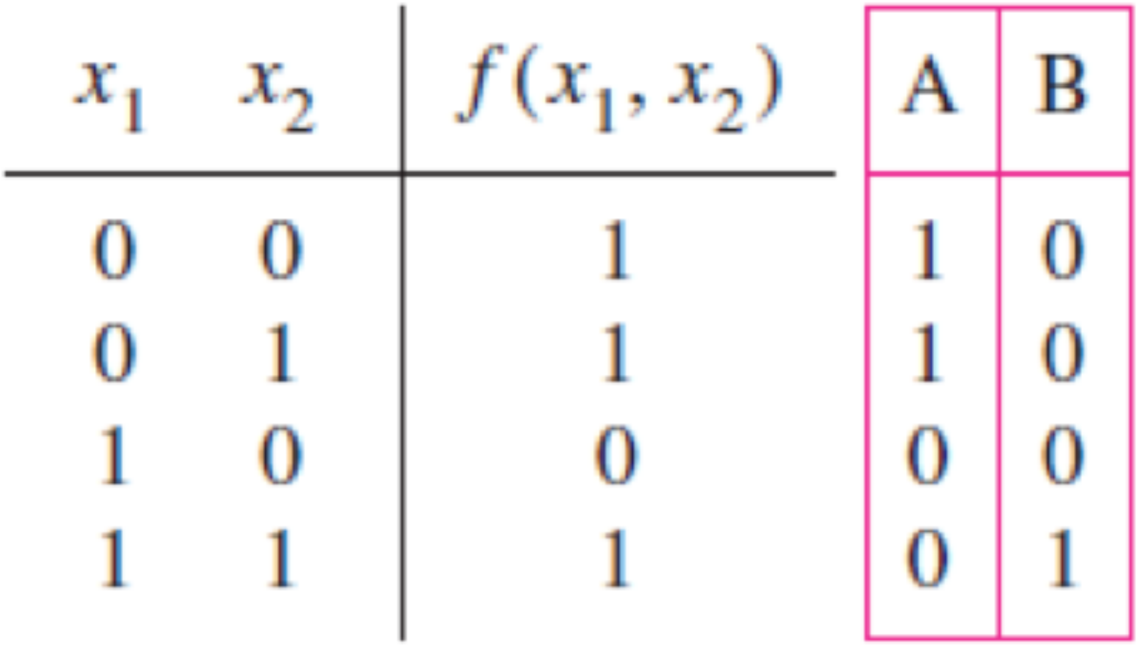
[Figure 2.10 from the textbook]

Timing Diagram



[Figure 2.10 from the textbook]

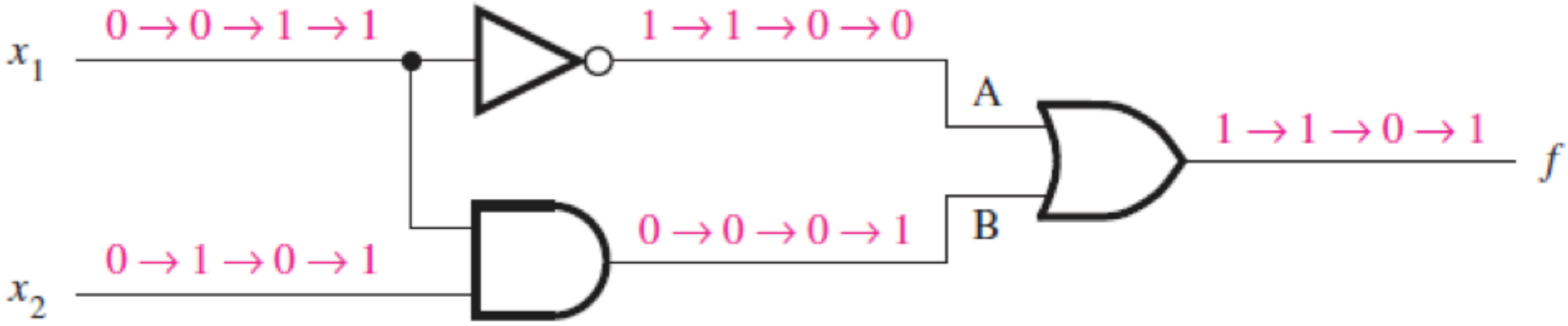
Truth Table for this Logic Circuit



x_1	x_2	$f(x_1, x_2)$	A	B
0	0	1	1	0
0	1	1	1	0
1	0	0	0	0
1	1	1	0	1

[Figure 2.10 from the textbook]

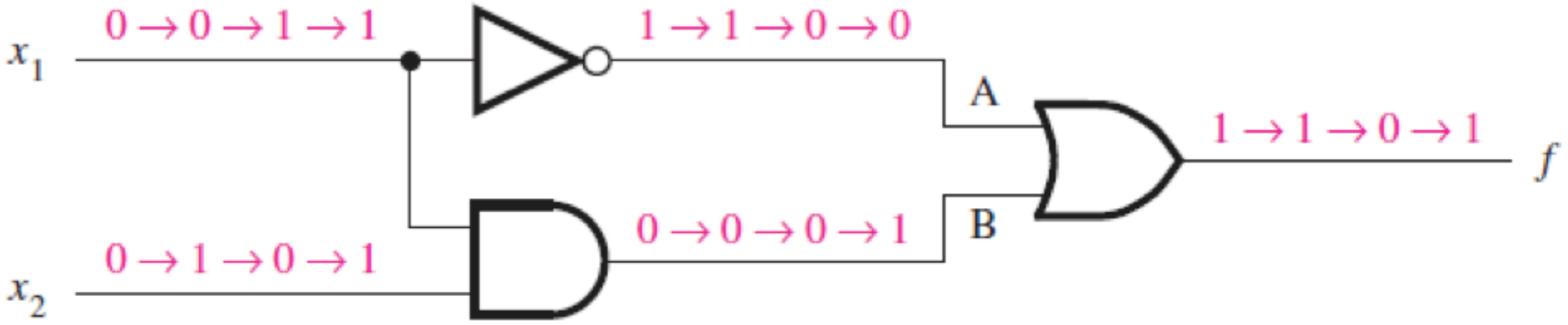
Functionally Equivalent Circuits


x_1
$0 \rightarrow 0 \rightarrow 1 \rightarrow 1$
$1 \rightarrow 1 \rightarrow 0 \rightarrow 0$
A
$1 \rightarrow 1 \rightarrow 0 \rightarrow 1$
f
$0 \rightarrow 0 \rightarrow 0 \rightarrow 1$
B
$0 \rightarrow 1 \rightarrow 0 \rightarrow 1$
x_2

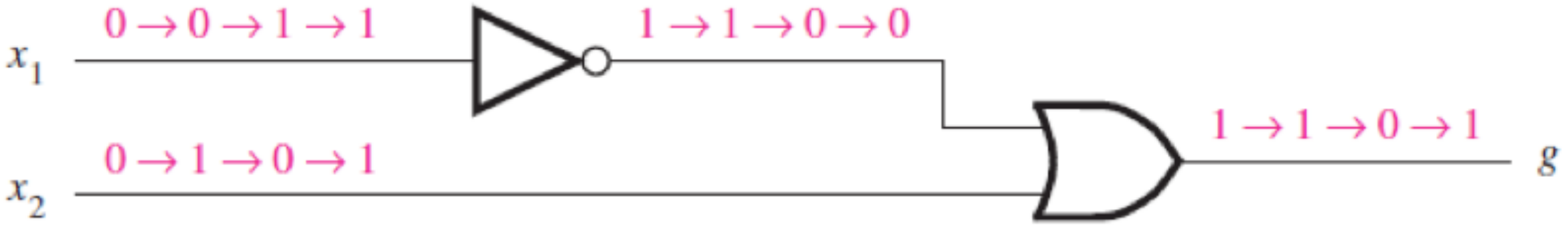
(a) Network that implements $f = \bar{x}_1 + x_1 \cdot x_2$

[Figure 2.10 from the textbook]

Functionally Equivalent Circuits


x_1
$0 \rightarrow 0 \rightarrow 1 \rightarrow 1$
$1 \rightarrow 1 \rightarrow 0 \rightarrow 0$
A
$1 \rightarrow 1 \rightarrow 0 \rightarrow 1$
f
$0 \rightarrow 0 \rightarrow 0 \rightarrow 1$
B
x_2
$0 \rightarrow 1 \rightarrow 0 \rightarrow 1$

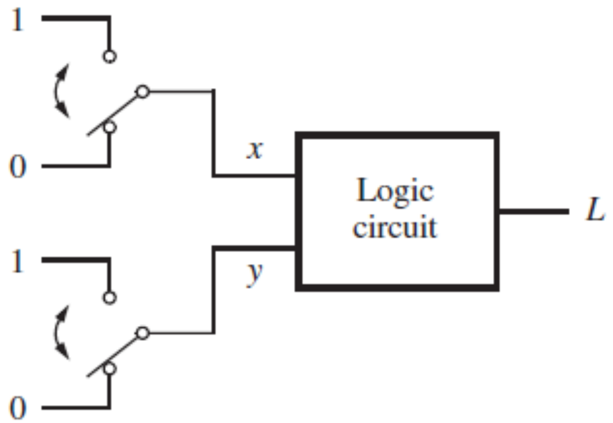
(a) Network that implements $f = \bar{x}_1 + x_1 \cdot x_2$


x_1
$0 \rightarrow 0 \rightarrow 1 \rightarrow 1$
$1 \rightarrow 1 \rightarrow 0 \rightarrow 0$
$1 \rightarrow 1 \rightarrow 0 \rightarrow 1$
g
x_2
$0 \rightarrow 1 \rightarrow 0 \rightarrow 1$

(d) Network that implements $g = \bar{x}_1 + x_2$

[Figure 2.10 from the textbook]

The XOR Logic Gate



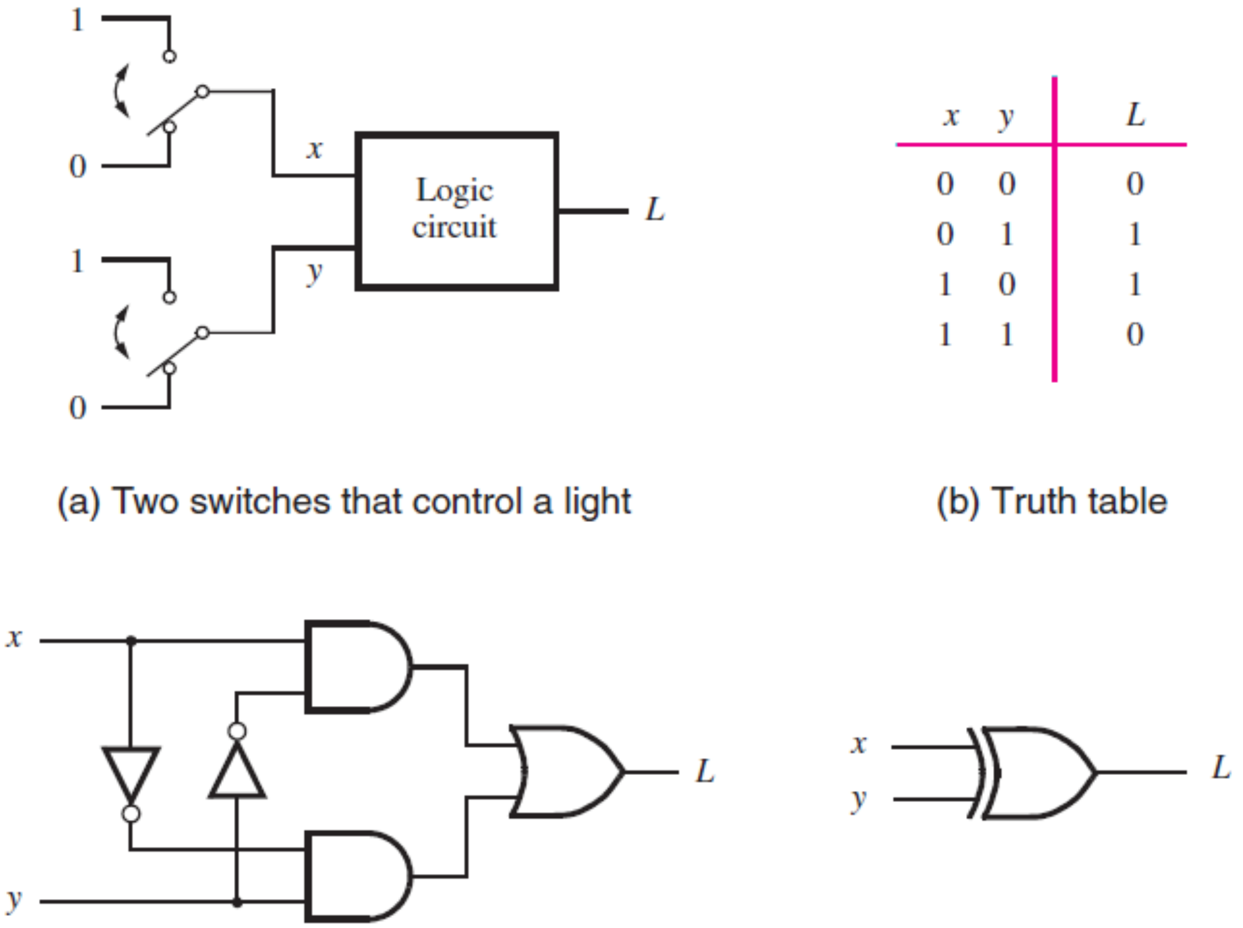
(a) Two switches that control a light

x	y	L
0	0	0
0	1	1
1	0	1
1	1	0

(b) Truth table

[Figure 2.11 from the textbook]

The XOR Logic Gate



(a) Two switches that control a light

x	y	L
0	0	0
0	1	1
1	0	1
1	1	0

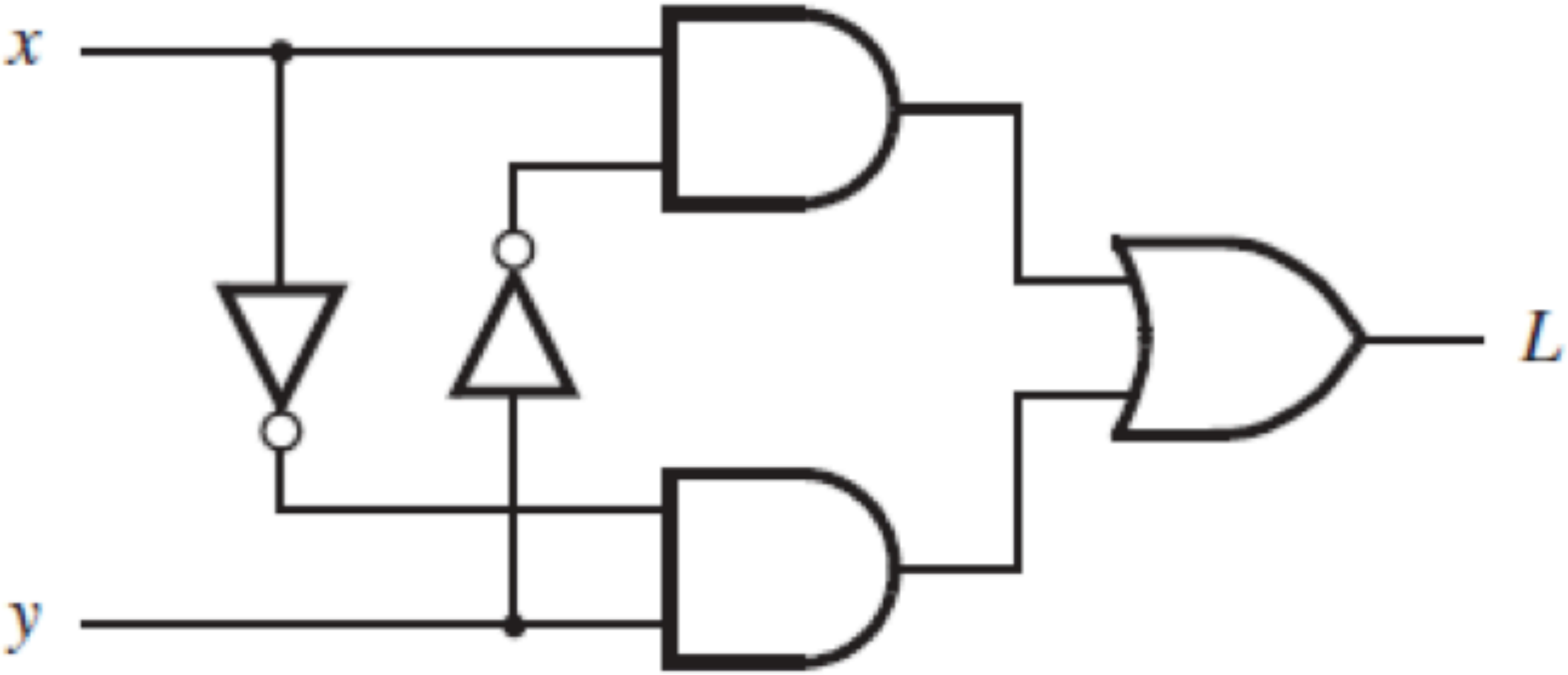
(b) Truth table

(c) Logic network

(d) XOR gate symbol

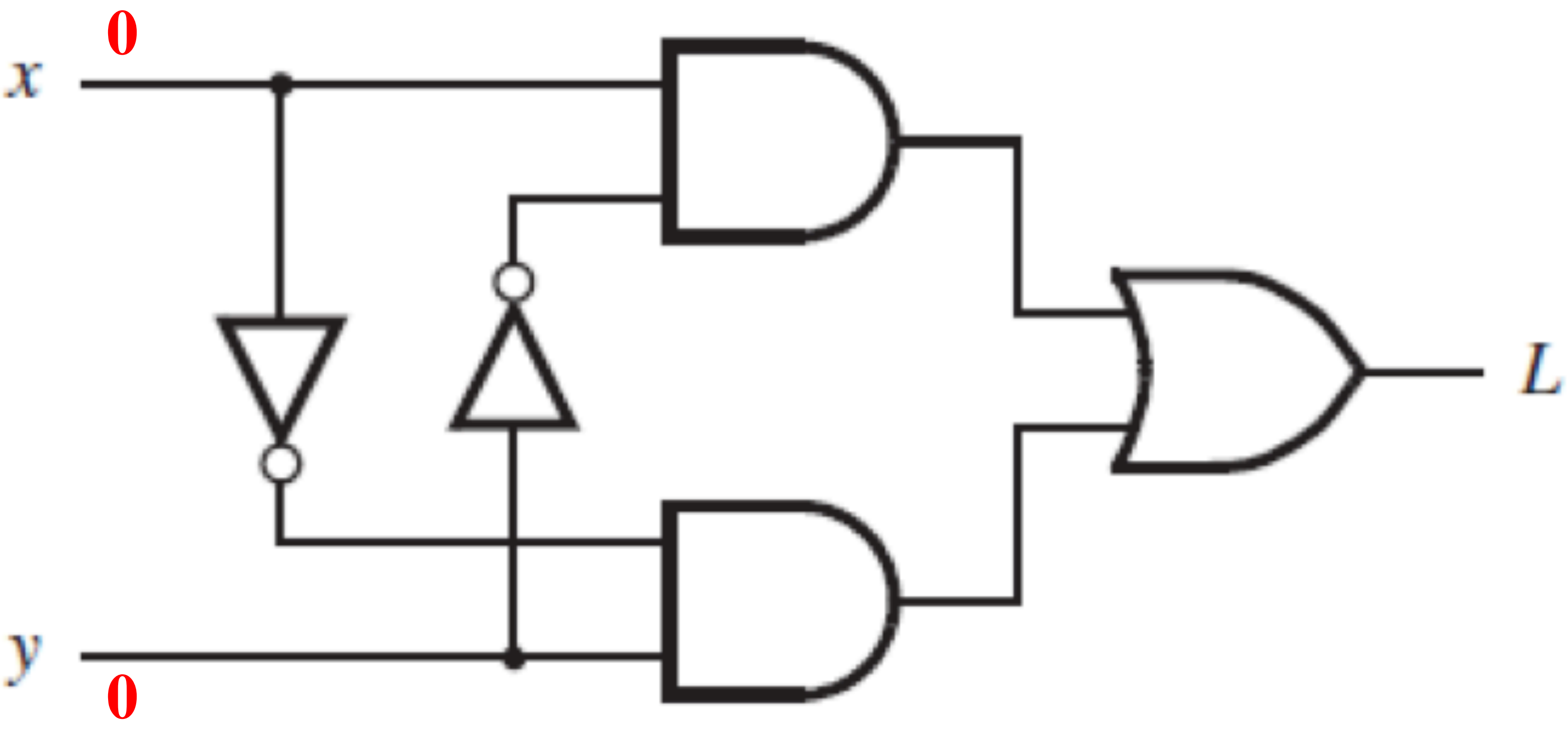
[Figure 2.11 from the textbook]

XOR Analysis

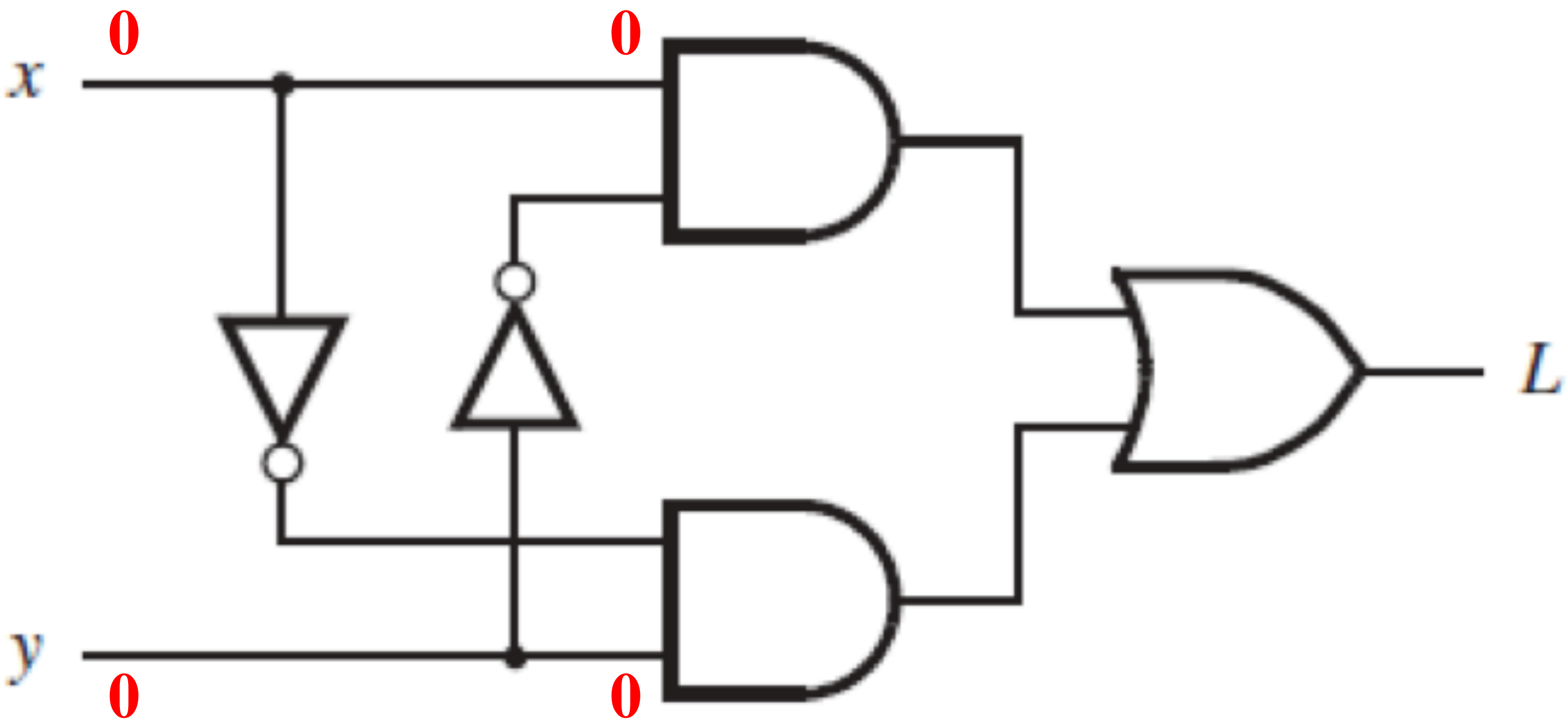


[Figure 2.11c from the textbook]

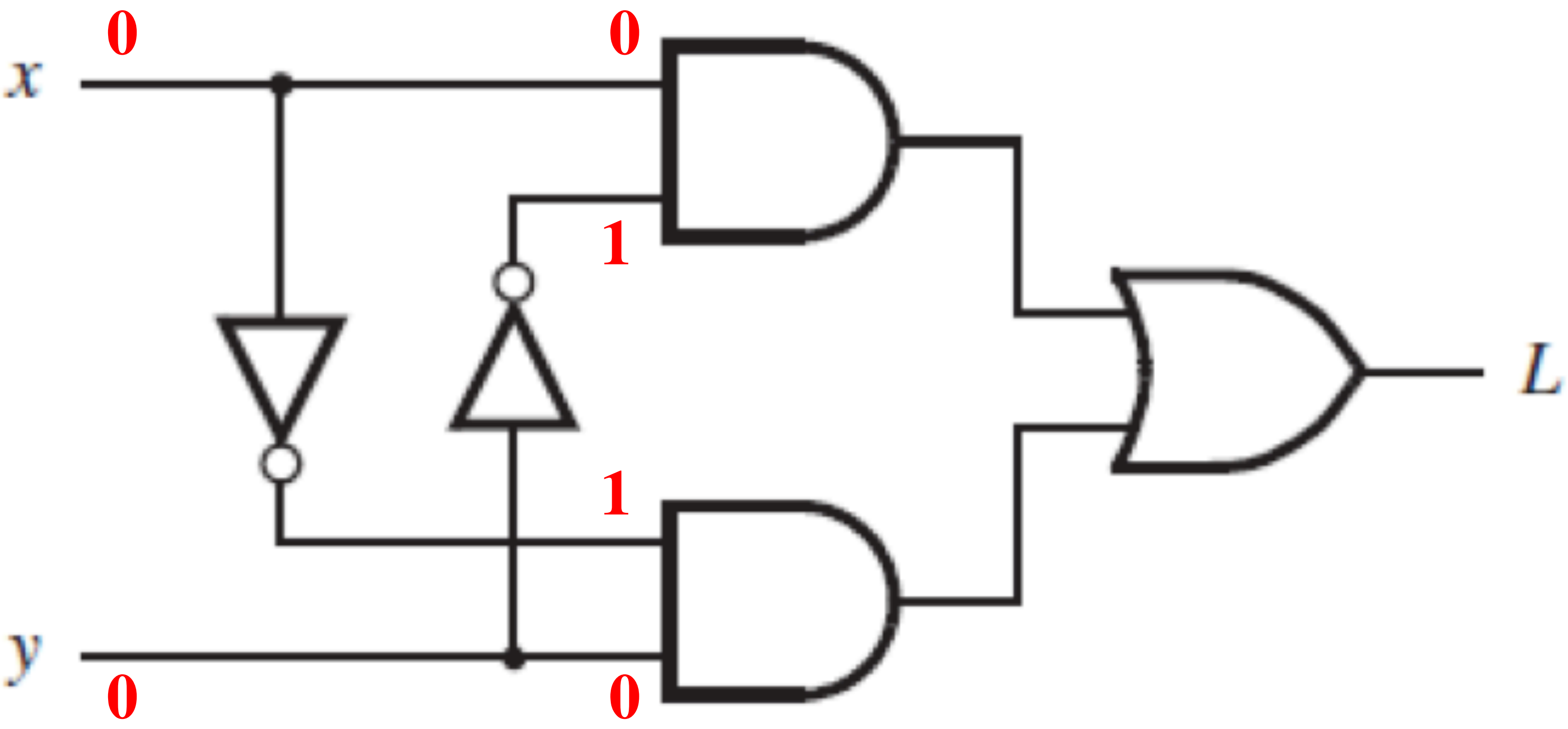
XOR Analysis (x=0, y=0)



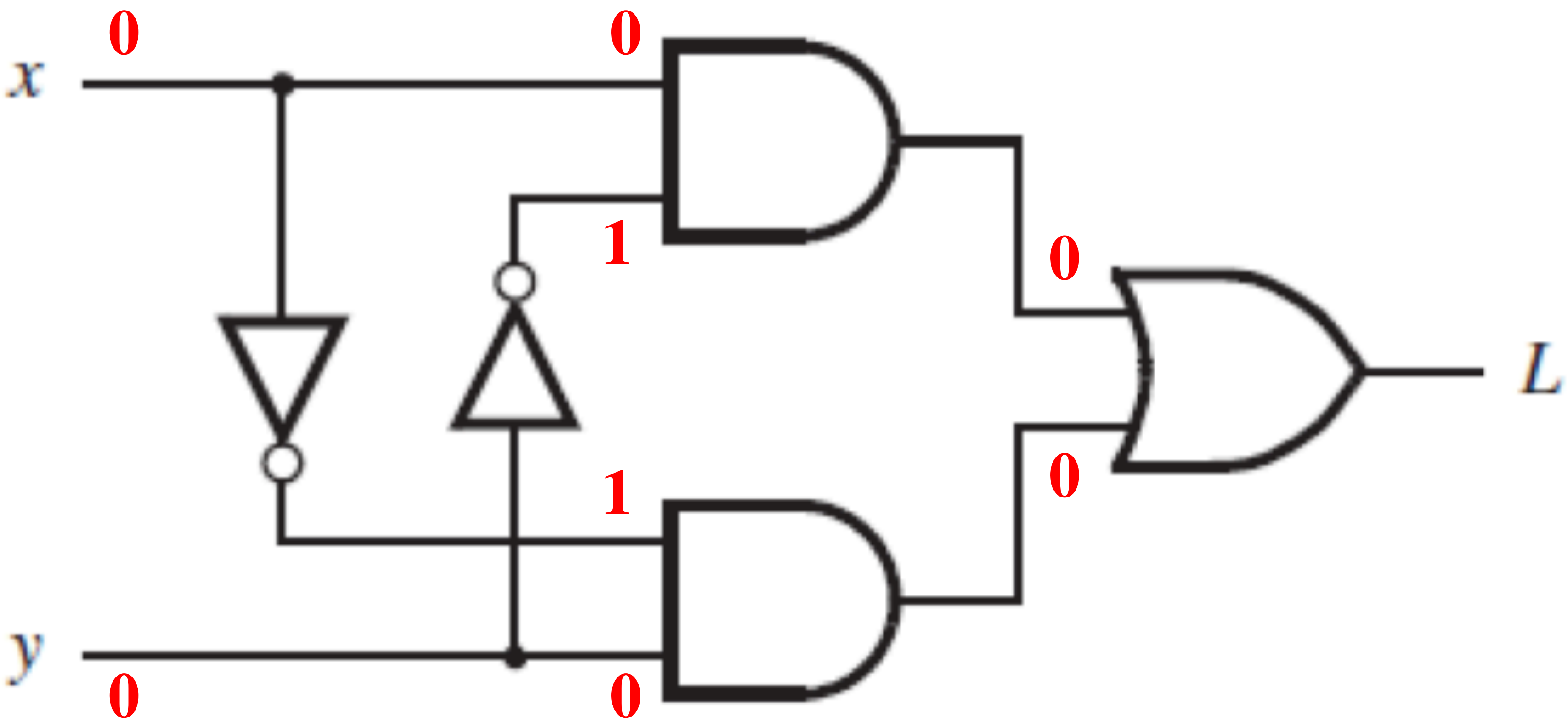
XOR Analysis (x=0, y=0)



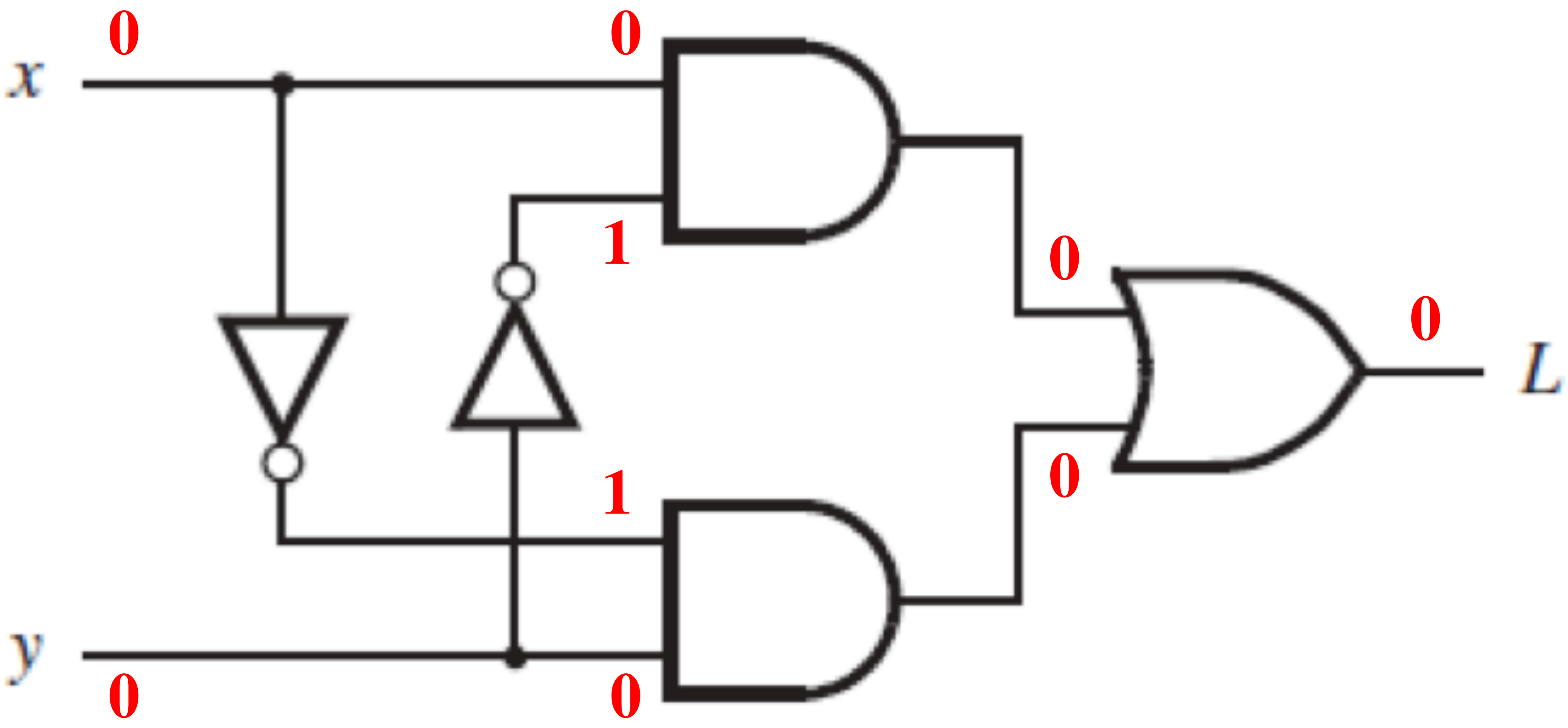
XOR Analysis (x=0, y=0)



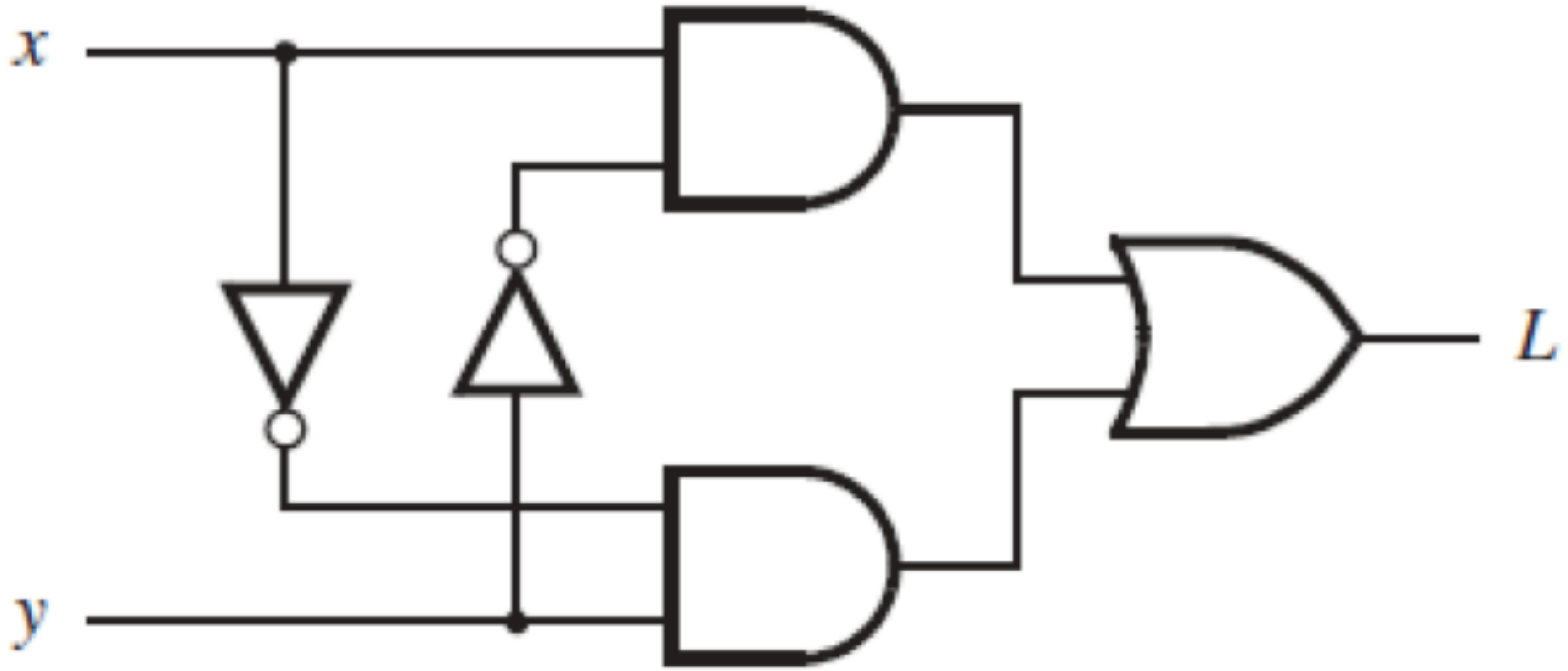
XOR Analysis (x=0, y=0)



XOR Analysis (x=0, y=0)

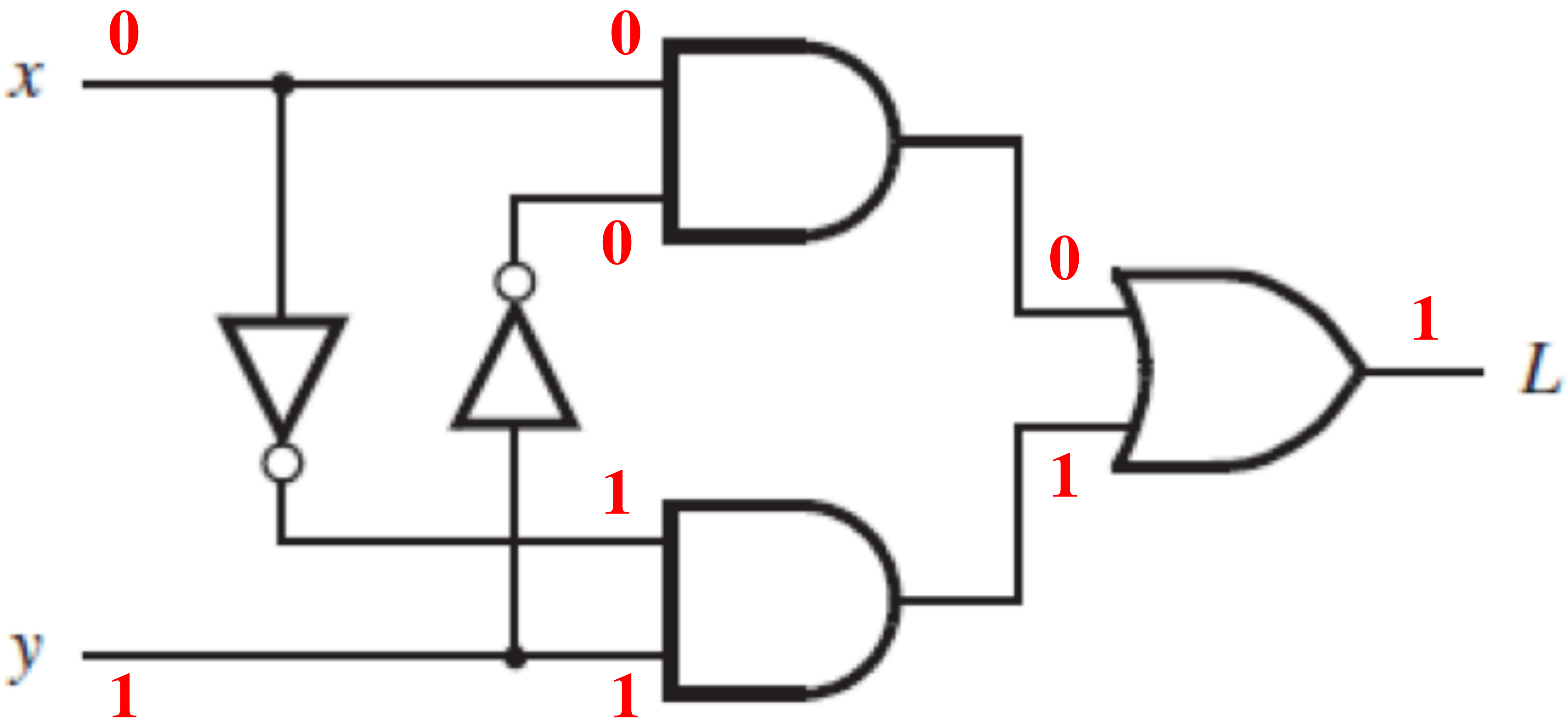


XOR Analysis

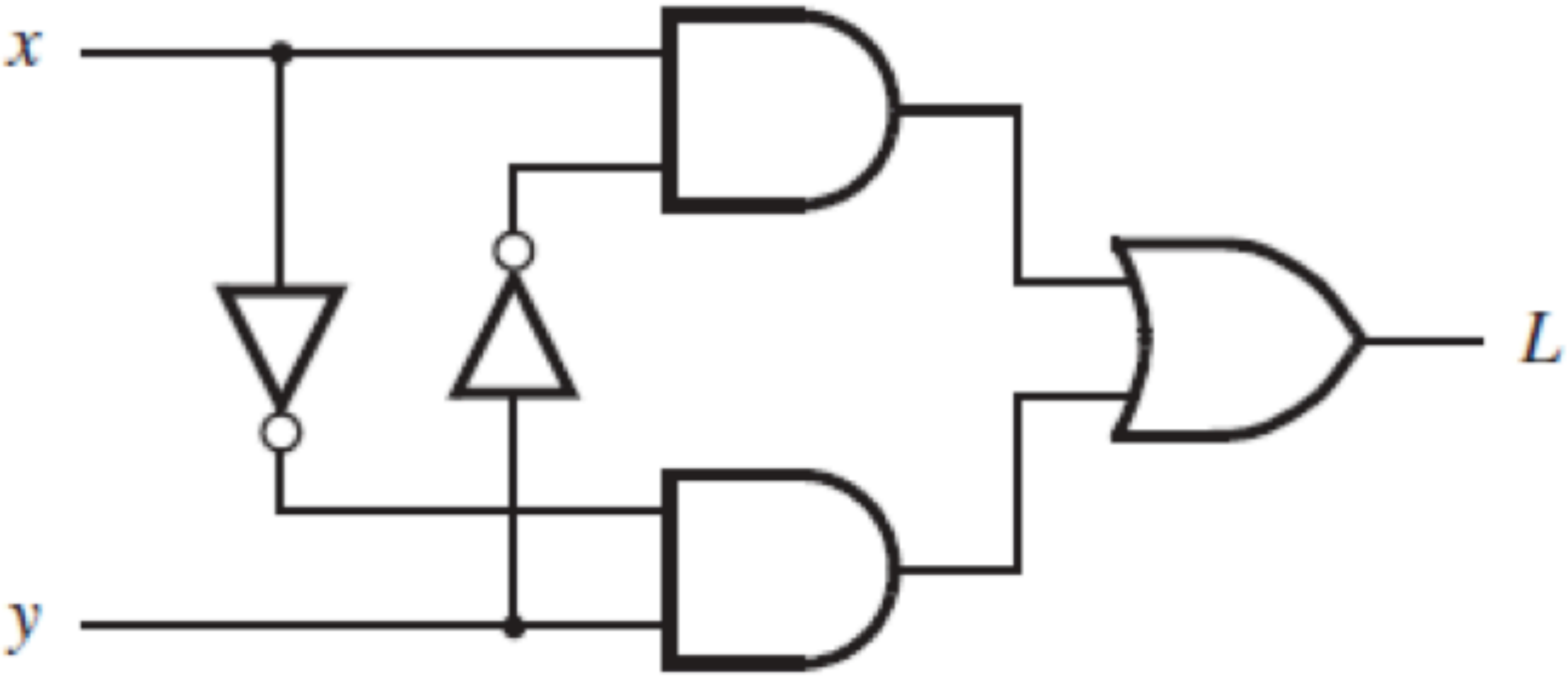


[Figure 2.11c from the textbook]

XOR Analysis (x=0, y=1)

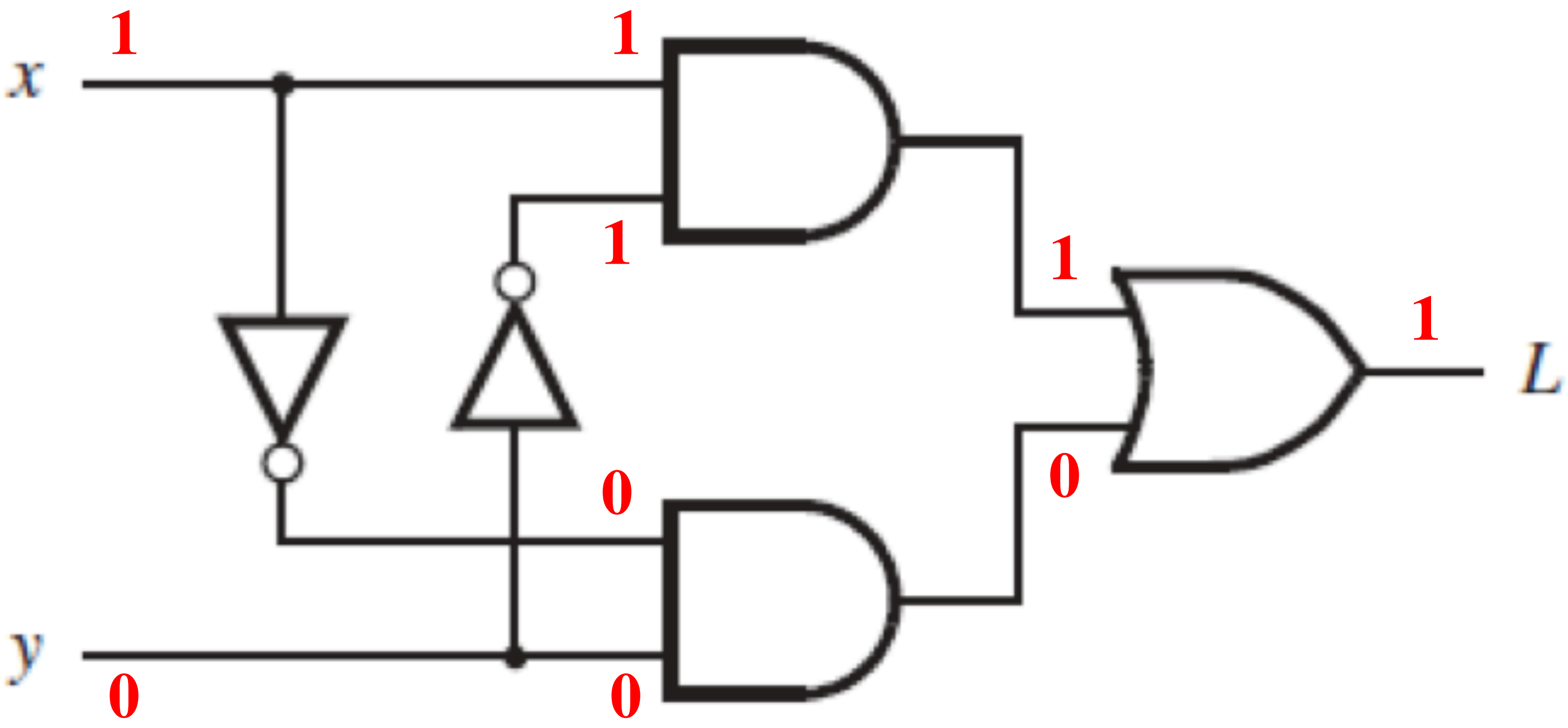


XOR Analysis

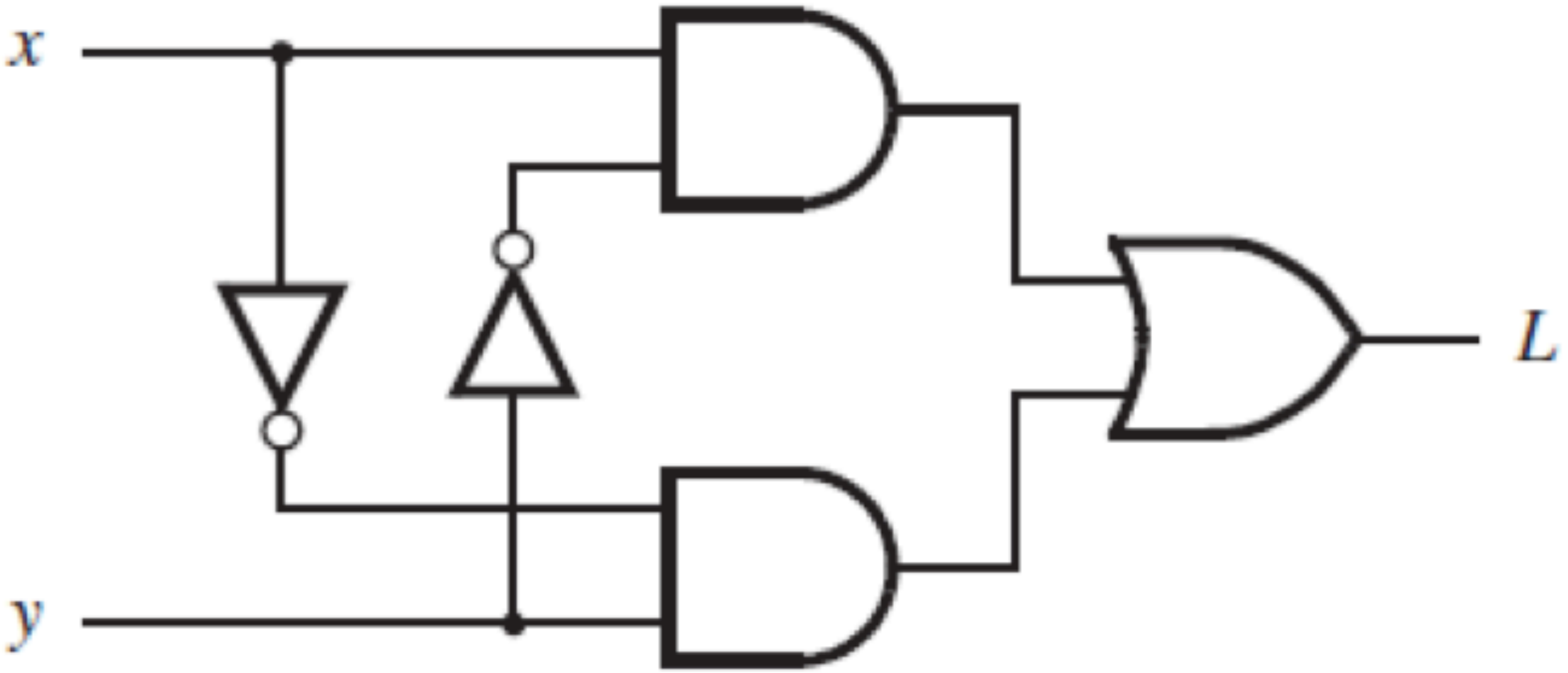


[Figure 2.11c from the textbook]

XOR Analysis (x=1, y=0)

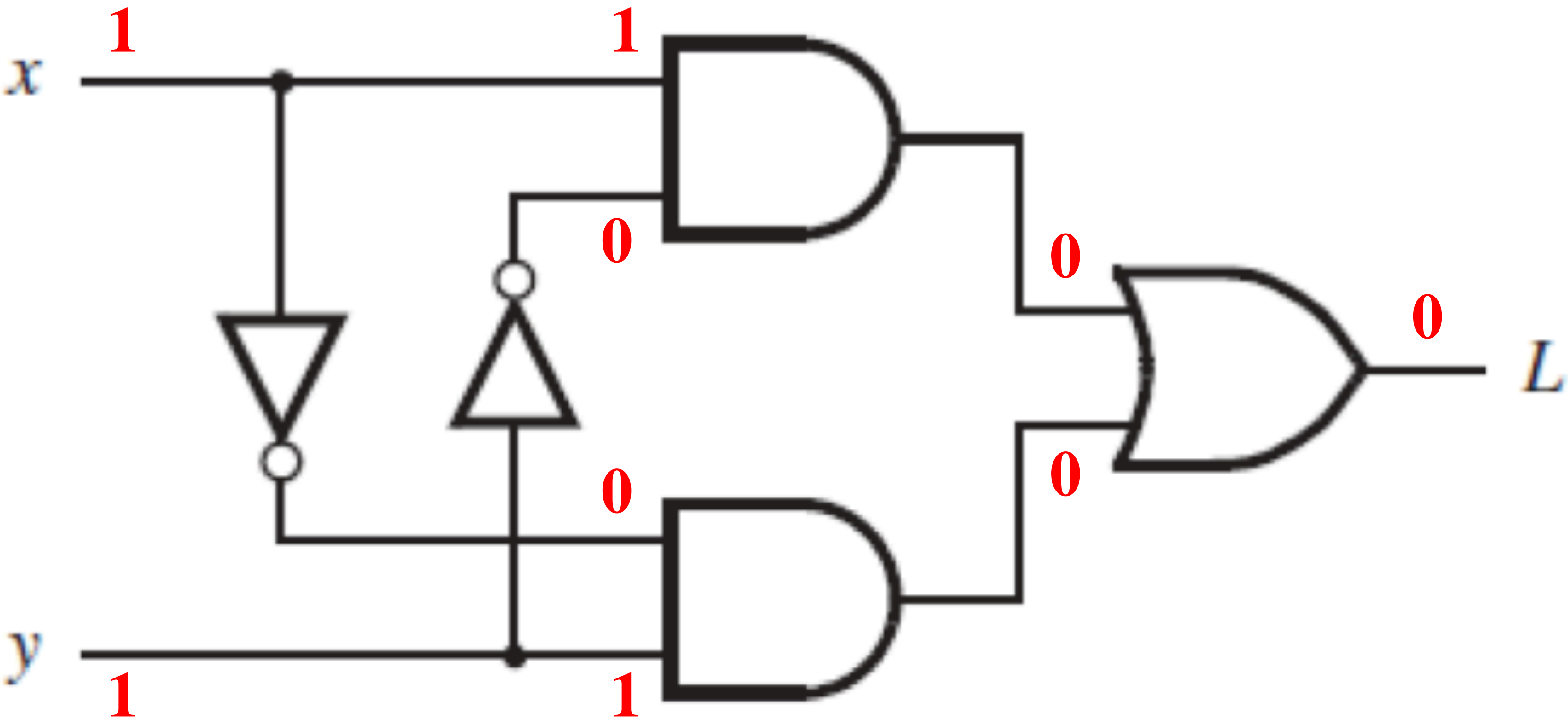


XOR Analysis

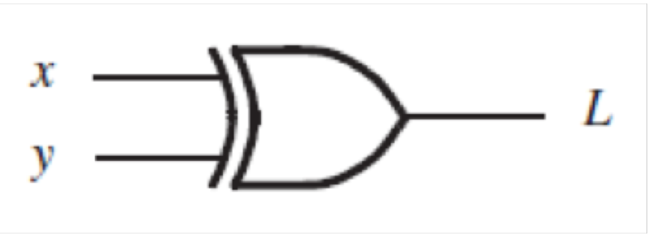


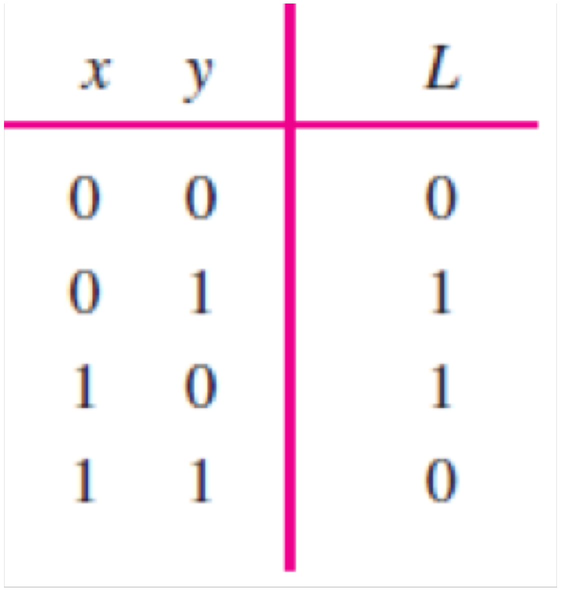
[Figure 2.11c from the textbook]

XOR Analysis (x=1, y=1)



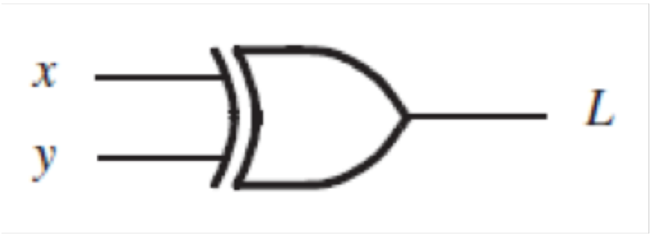
Truth Table for XOR

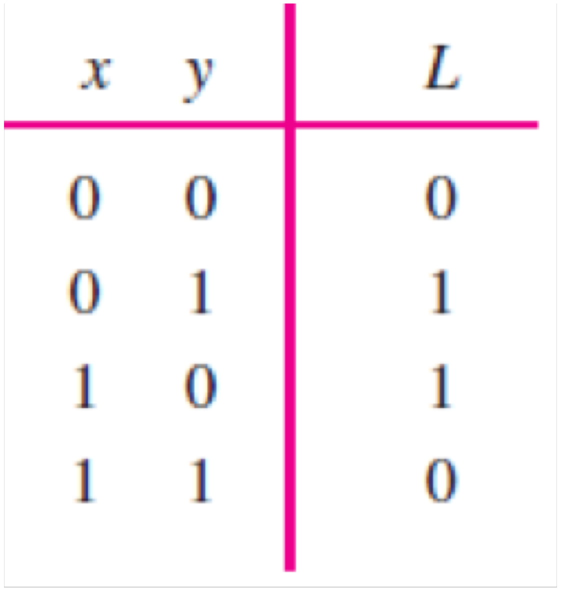




x	y	L
0	0	0
0	1	1
1	0	1
1	1	0

Truth Table for XOR





x	y	L
0	0	0
0	1	1
1	0	1
1	1	0

The output is 1 only if both inputs are different.

Addition of Binary Numbers

$$
\begin{array}{r}
a\\
+\,b\\
\hline
s_1\,s_0
\end{array}
\qquad\qquad
\begin{array}{r}
0\\
+\,0\\
\hline
0\;0
\end{array}
\qquad
\begin{array}{r}
0\\
+\,1\\
\hline
0\;1
\end{array}
\qquad
\begin{array}{r}
1\\
+\,0\\
\hline
0\;1
\end{array}
\qquad
\begin{array}{r}
1\\
+\,1\\
\hline
1\;0
\end{array}
$$

[Figure 2.12 from the textbook]

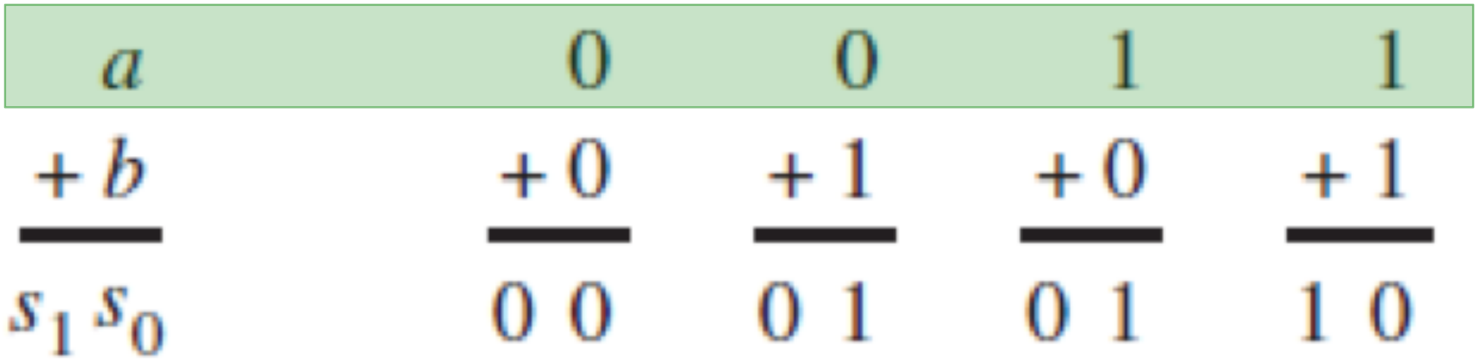
Addition of Binary Numbers

$$\begin{array}{r} a \\ +\,b \\ \hline s_1\, s_0 \end{array} \qquad \begin{array}{r} 0 \\ +\,0 \\ \hline 0\;0 \end{array} \quad \begin{array}{r} 0 \\ +\,1 \\ \hline 0\;1 \end{array} \quad \begin{array}{r} 1 \\ +\,0 \\ \hline 0\;1 \end{array} \quad \begin{array}{r} 1 \\ +\,1 \\ \hline 1\;0 \end{array}$$

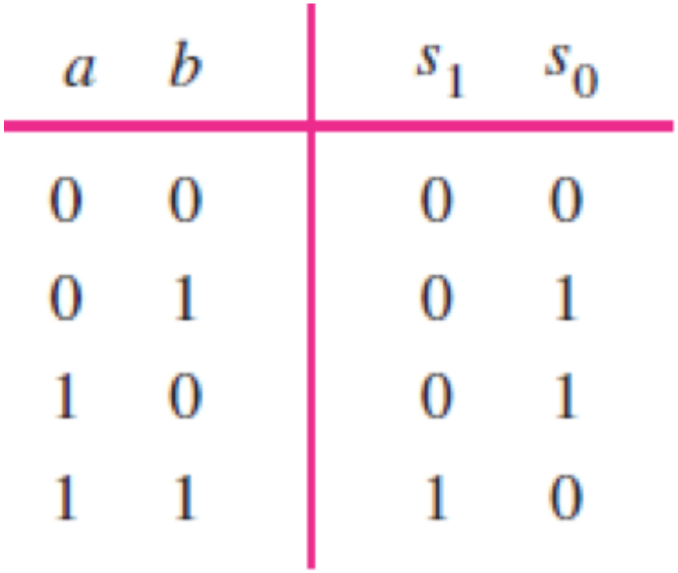
a	b	s_1	s_0
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

[Figure 2.12 from the textbook]

Addition of Binary Numbers

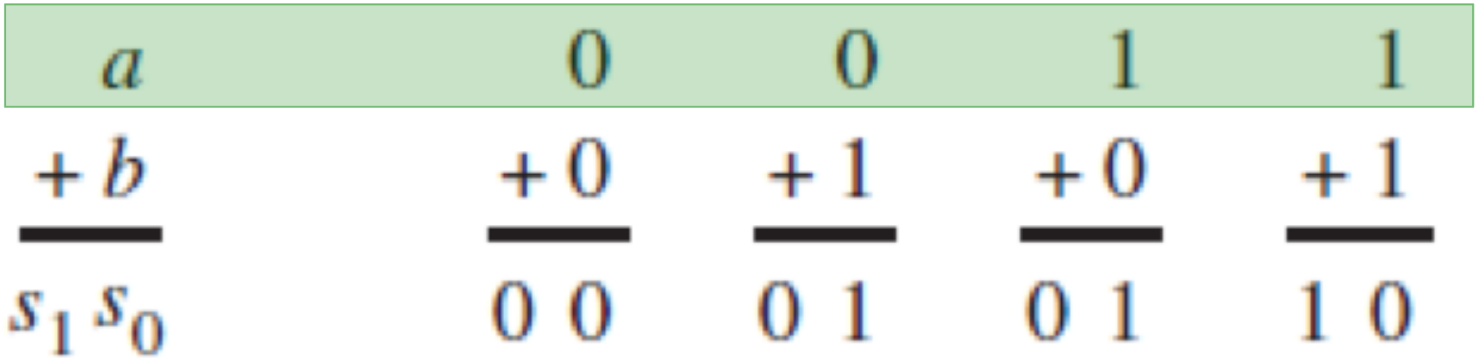


a	0	0	1	1
$+b$	$+0$	$+1$	$+0$	$+1$
$s_1\ s_0$	0 0	0 1	0 1	1 0

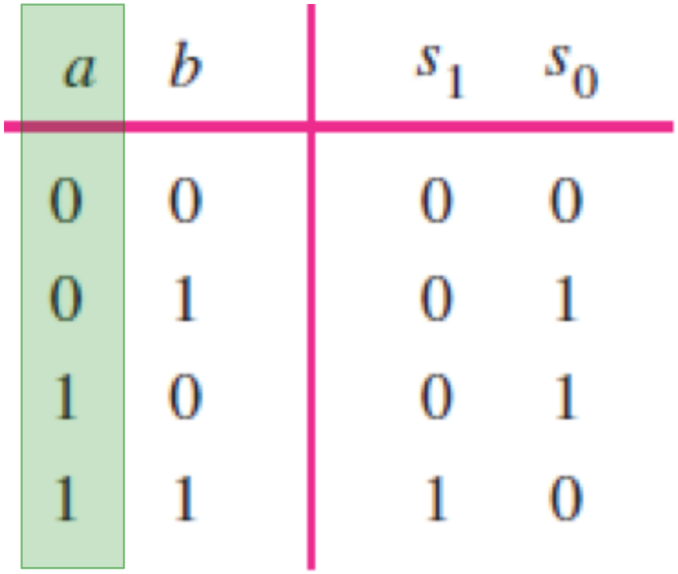


a	b	s_1	s_0
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Addition of Binary Numbers



a	0	0	1	1
$+b$	$+0$	$+1$	$+0$	$+1$
$s_1 s_0$	0 0	0 1	0 1	1 0



a	b	s_1	s_0
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Addition of Binary Numbers

$$\begin{array}{r} a \\ +\,b \\ \hline s_1\,s_0 \end{array} \qquad \begin{array}{r} 0 \\ +\,0 \\ \hline 0\;0 \end{array} \quad \begin{array}{r} 0 \\ +\,1 \\ \hline 0\;1 \end{array} \quad \begin{array}{r} 1 \\ +\,0 \\ \hline 0\;1 \end{array} \quad \begin{array}{r} 1 \\ +\,1 \\ \hline 1\;0 \end{array}$$

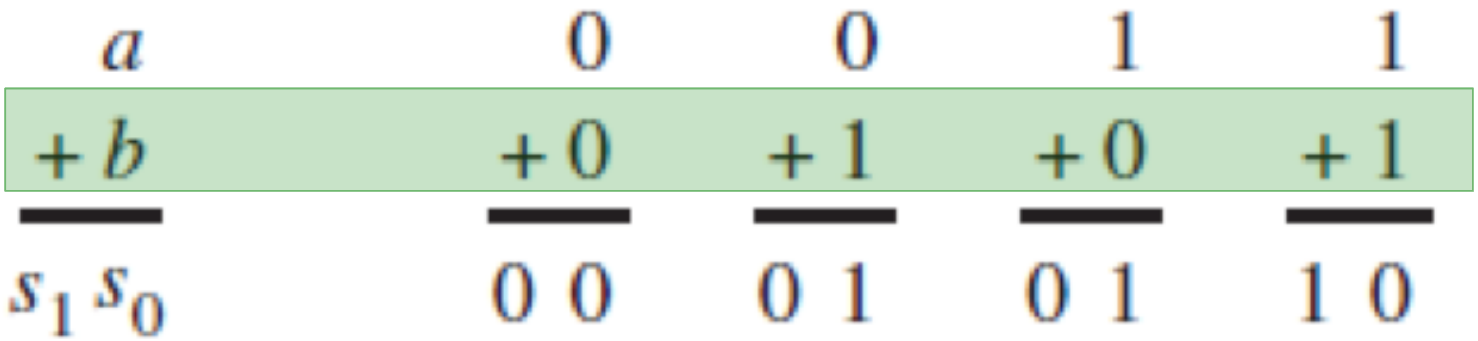
a	b	s_1	s_0
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Addition of Binary Numbers

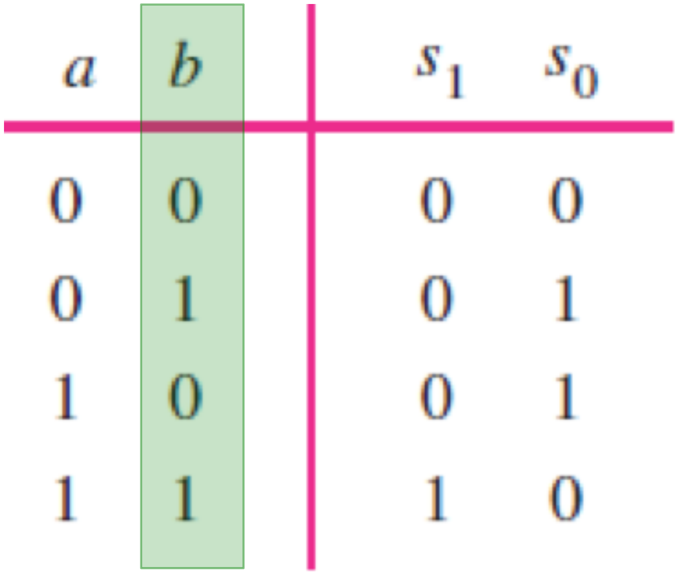
a	0	0	1	1
$+b$	$+0$	$+1$	$+0$	$+1$
$s_1\ s_0$	0 0	0 1	0 1	1 0

a	b	s_1	s_0
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Addition of Binary Numbers



a	0	0	1	1
$+b$	+0	+1	+0	+1
$s_1 s_0$	0 0	0 1	0 1	1 0



a	b	s_1	s_0
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Addition of Binary Numbers

$$\begin{array}{r} a \\ +\,b \\ \hline s_1\,s_0 \end{array} \qquad \begin{array}{r} 0 \\ +\,0 \\ \hline 0\;0 \end{array} \quad \begin{array}{r} 0 \\ +\,1 \\ \hline 0\;1 \end{array} \quad \begin{array}{r} 1 \\ +\,0 \\ \hline 0\;1 \end{array} \quad \begin{array}{r} 1 \\ +\,1 \\ \hline 1\;0 \end{array}$$

a	b	s_1	s_0
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Addition of Binary Numbers

$$\begin{array}{r} a \\ +\,b \\ \hline \boxed{s_1}\,s_0 \end{array} \qquad\qquad \begin{array}{r} 0 \\ +\,0 \\ \hline \boxed{0}\,0 \end{array} \qquad \begin{array}{r} 0 \\ +\,1 \\ \hline \boxed{0}\,1 \end{array} \qquad \begin{array}{r} 1 \\ +\,0 \\ \hline \boxed{0}\,1 \end{array} \qquad \begin{array}{r} 1 \\ +\,1 \\ \hline \boxed{1}\,0 \end{array}$$

a	b	s_1	s_0
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Addition of Binary Numbers

$$\begin{array}{r} a \\ +\,b \\ \hline s_1\,s_0 \end{array} \qquad \begin{array}{r} 0 \\ +\,0 \\ \hline 0\,0 \end{array} \qquad \begin{array}{r} 0 \\ +\,1 \\ \hline 0\,1 \end{array} \qquad \begin{array}{r} 1 \\ +\,0 \\ \hline 0\,1 \end{array} \qquad \begin{array}{r} 1 \\ +\,1 \\ \hline 1\,0 \end{array}$$

a	b	s_1	s_0
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Addition of Binary Numbers

$$\begin{array}{r} a \\ +\,b \\ \hline s_1\,s_0 \end{array} \qquad\qquad \begin{array}{r} 0 \\ +\,0 \\ \hline 0\;0 \end{array} \qquad \begin{array}{r} 0 \\ +\,1 \\ \hline 0\;1 \end{array} \qquad \begin{array}{r} 1 \\ +\,0 \\ \hline 0\;1 \end{array} \qquad \begin{array}{r} 1 \\ +\,1 \\ \hline 1\;0 \end{array}$$

a	b	s_1	s_0
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Addition of Binary Numbers

$$\begin{array}{r} a \\ +\,b \\ \hline s_1\,\boxed{s_0} \end{array} \qquad\qquad \begin{array}{r} 0 \\ +\,0 \\ \hline 0\,\boxed{0} \end{array} \quad \begin{array}{r} 0 \\ +\,1 \\ \hline 0\,\boxed{1} \end{array} \quad \begin{array}{r} 1 \\ +\,0 \\ \hline 0\,\boxed{1} \end{array} \quad \begin{array}{r} 1 \\ +\,1 \\ \hline 1\,\boxed{0} \end{array}$$

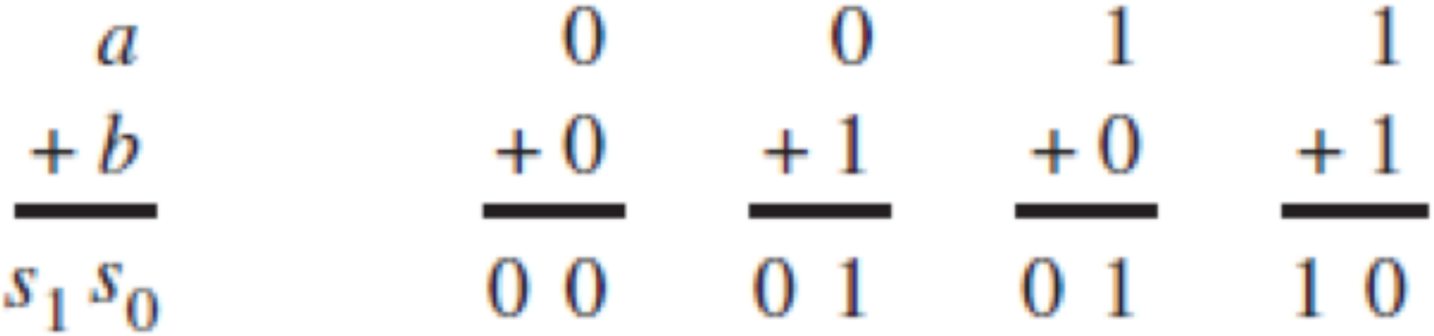
a	b	s_1	s_0
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Addition of Binary Numbers

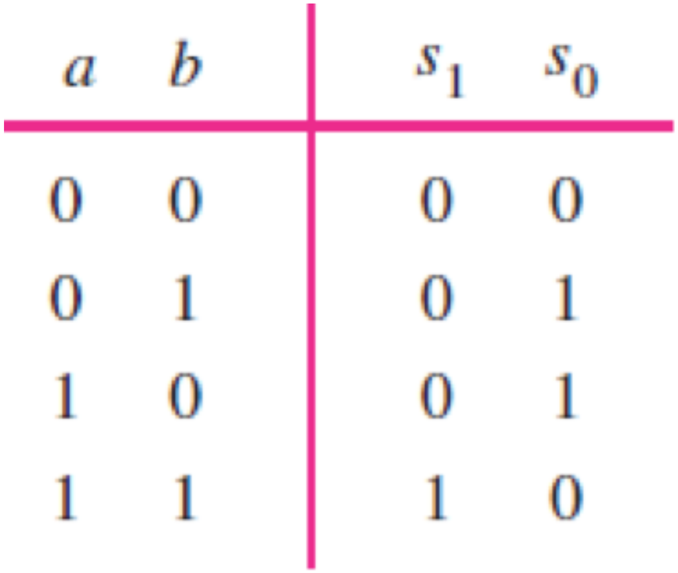
$$\begin{array}{r} a \\ +\,b \\ \hline s_1\,s_0 \end{array} \qquad \begin{array}{r} 0 \\ +\,0 \\ \hline 0\,0 \end{array} \quad \begin{array}{r} 0 \\ +\,1 \\ \hline 0\,1 \end{array} \quad \begin{array}{r} 1 \\ +\,0 \\ \hline 0\,1 \end{array} \quad \begin{array}{r} 1 \\ +\,1 \\ \hline 1\,0 \end{array}$$

a	b	s_1	s_0
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Addition of Binary Numbers

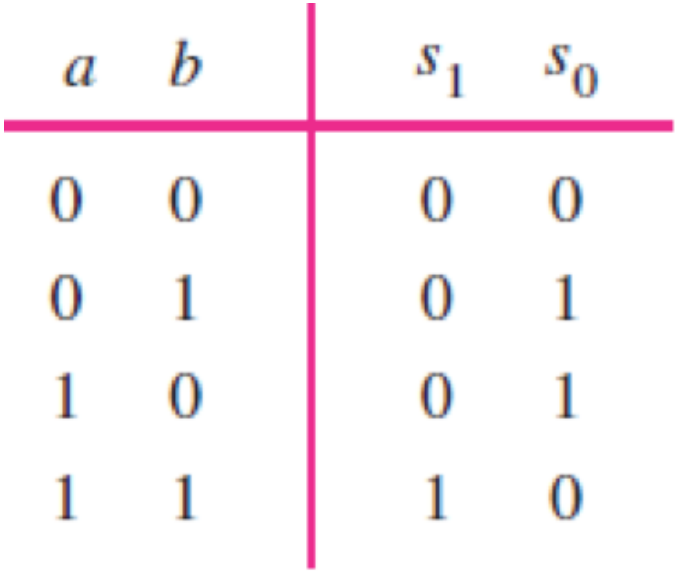


$$\begin{array}{r} a \\ +b \\ \hline s_1\,s_0 \end{array} \qquad \begin{array}{r} 0 \\ +0 \\ \hline 0\;0 \end{array} \qquad \begin{array}{r} 0 \\ +1 \\ \hline 0\;1 \end{array} \qquad \begin{array}{r} 1 \\ +0 \\ \hline 0\;1 \end{array} \qquad \begin{array}{r} 1 \\ +1 \\ \hline 1\;0 \end{array}$$



a	b	s_1	s_0
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

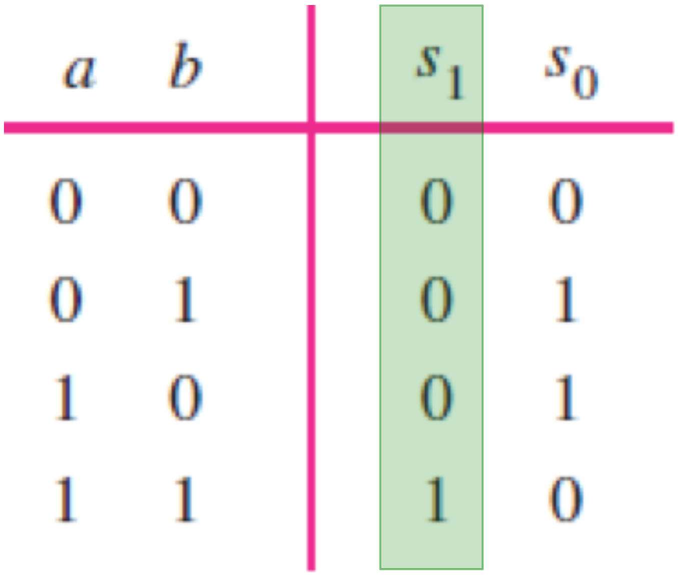
Addition of Binary Numbers



a	b	s_1	s_0
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Addition of Binary Numbers

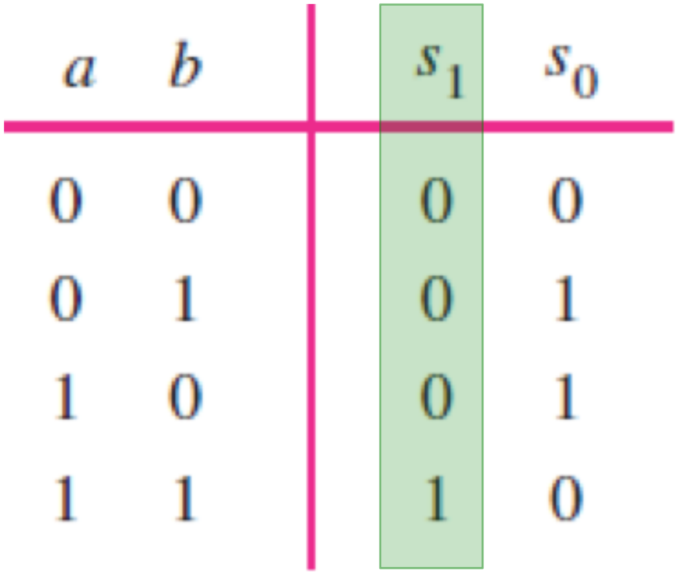
?



a	b	s_1	s_0
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

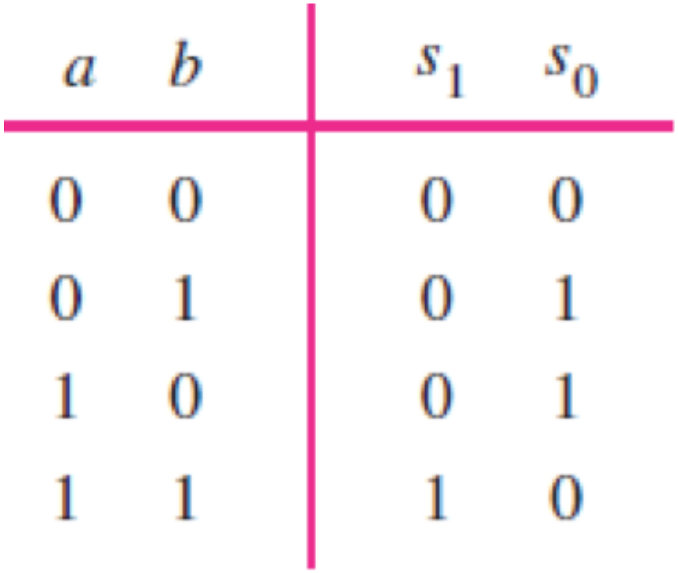
Addition of Binary Numbers

AND



a	b	s_1	s_0
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

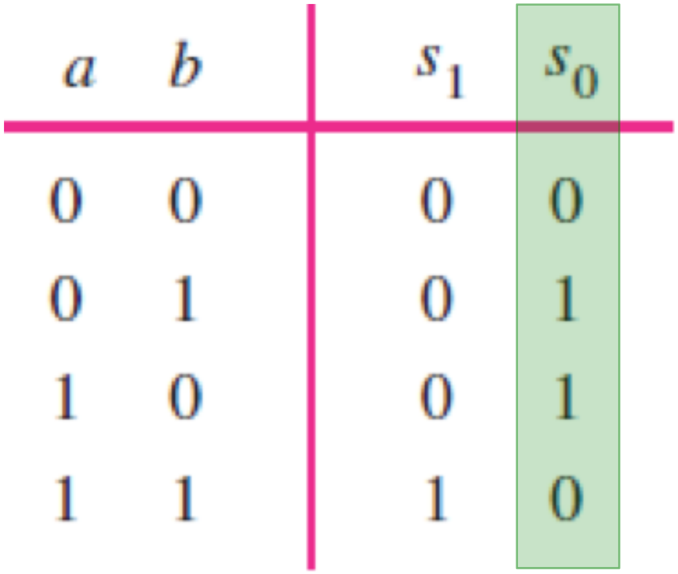
Addition of Binary Numbers



a	b	s_1	s_0
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Addition of Binary Numbers

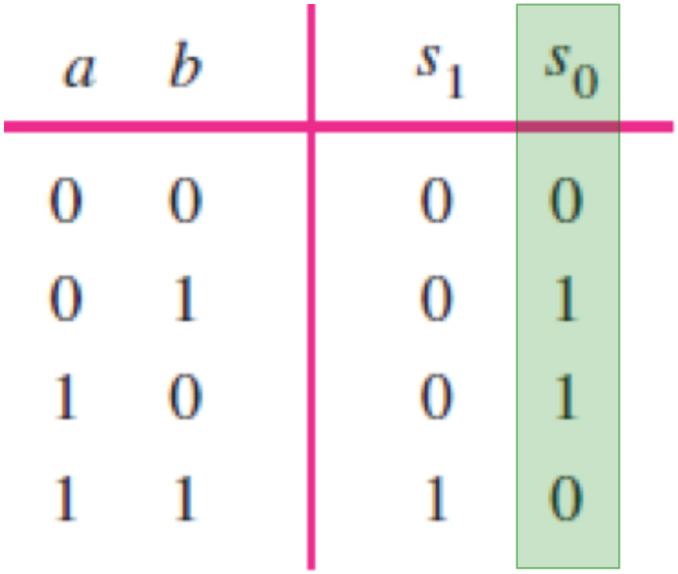
?



a	b	s_1	s_0
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

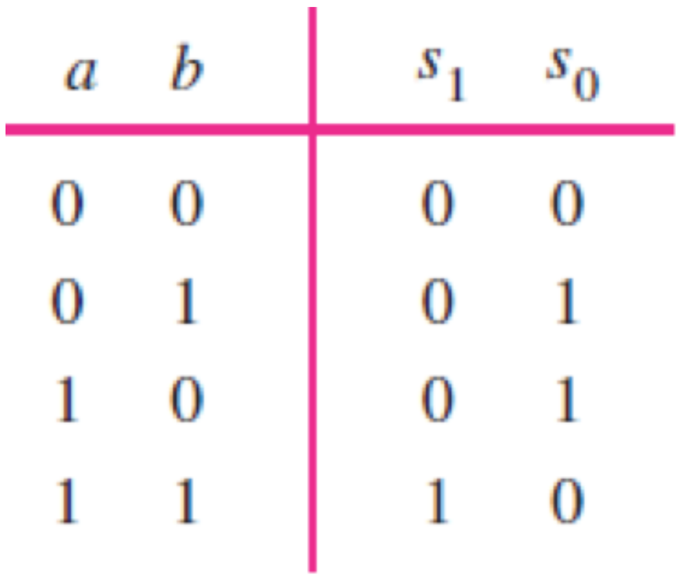
Addition of Binary Numbers

XOR



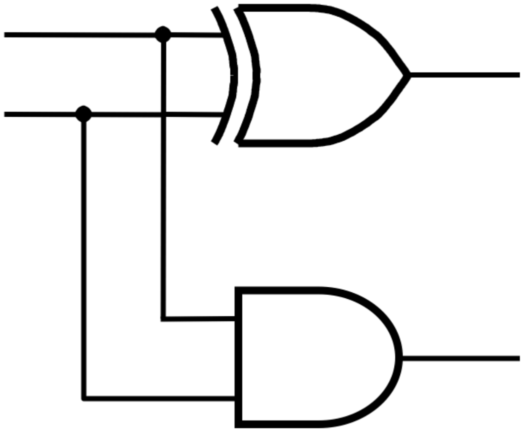
a	b	s_1	s_0
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Addition of Binary Numbers



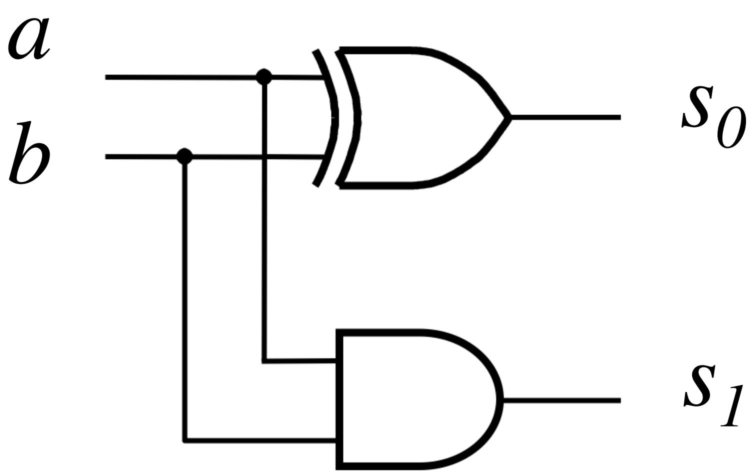
a	b	s_1	s_0
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

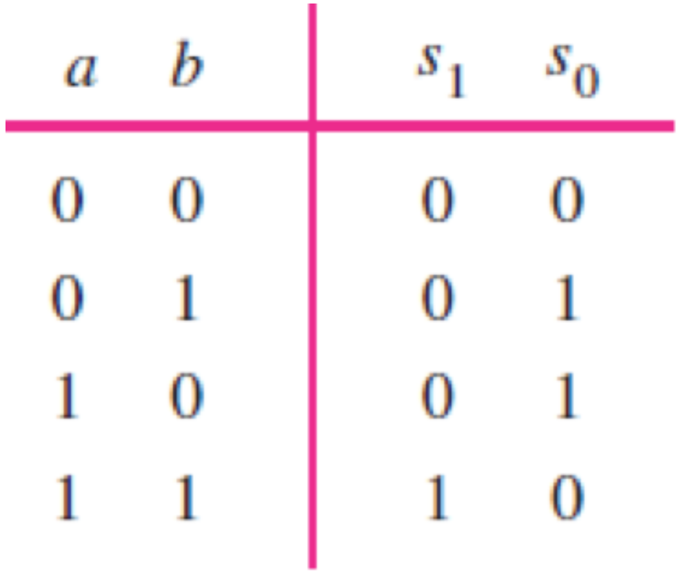
Addition of Binary Numbers



a	b	s_1	s_0
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

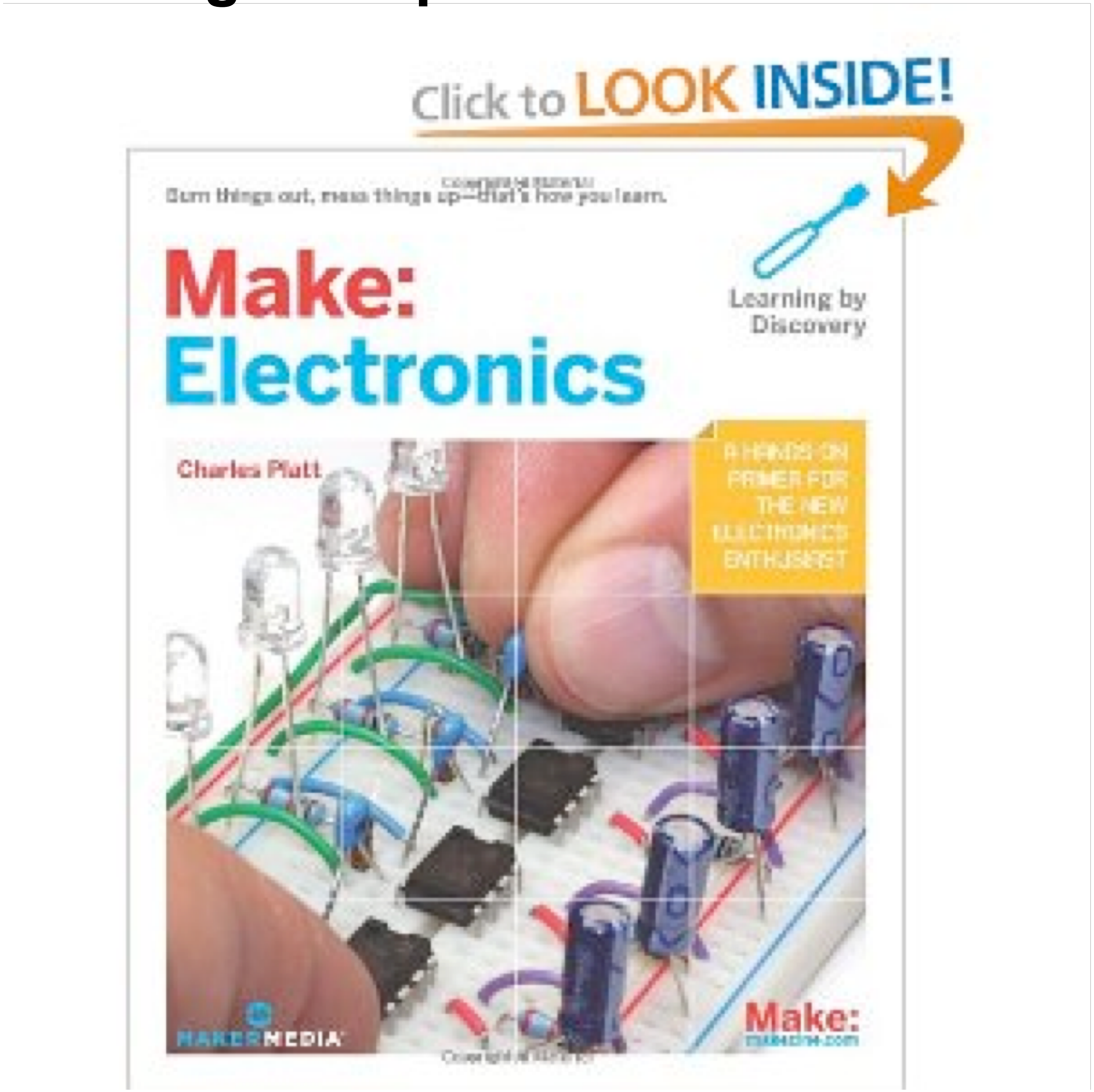
Addition of Binary Numbers





a	b	s_1	s_0
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

The following examples came from this book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Burn things out, mess things up—that's how you learn.
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A HANDS-ON PRIMER FOR THE NEW ELECTRONICS ENTHUSIAST
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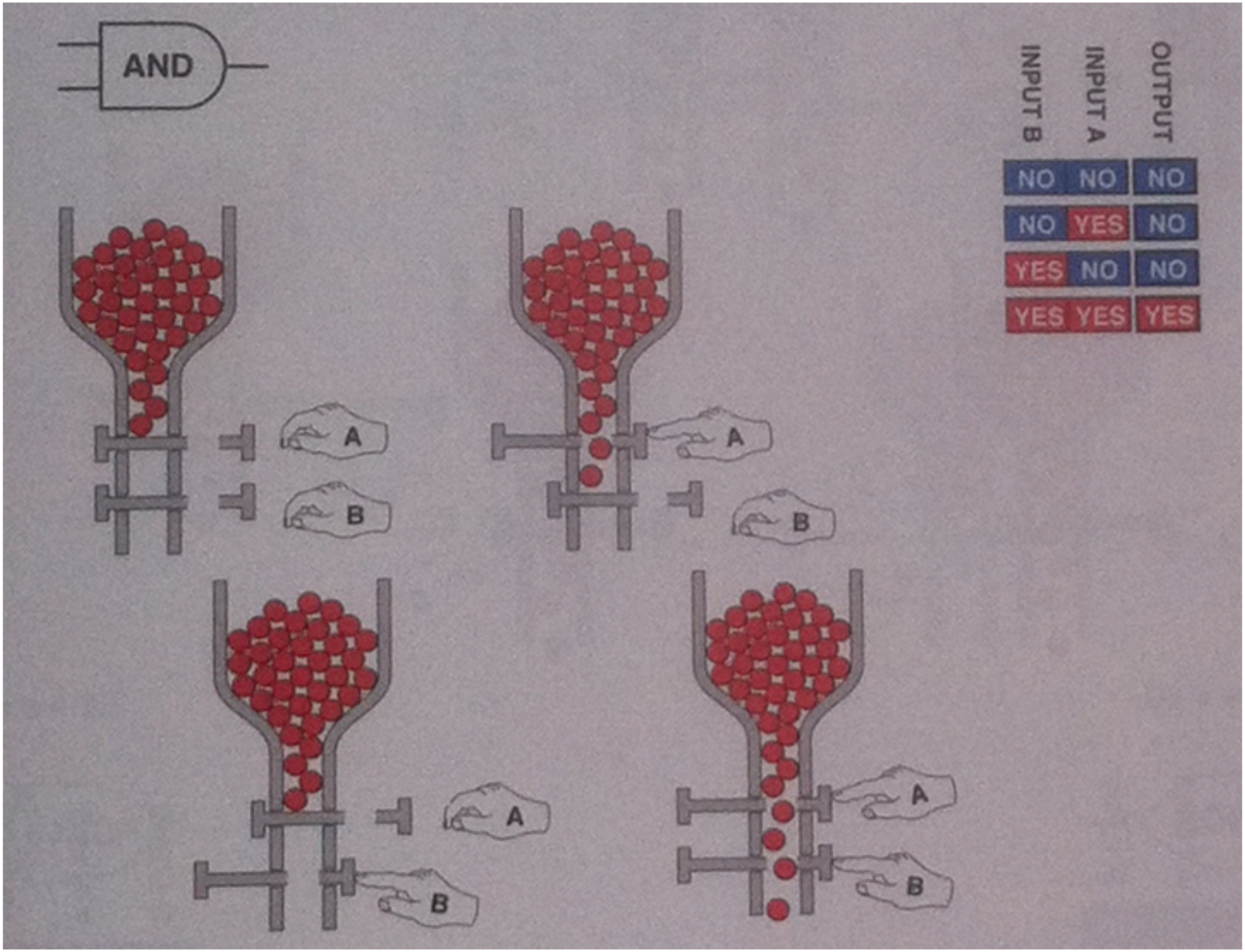
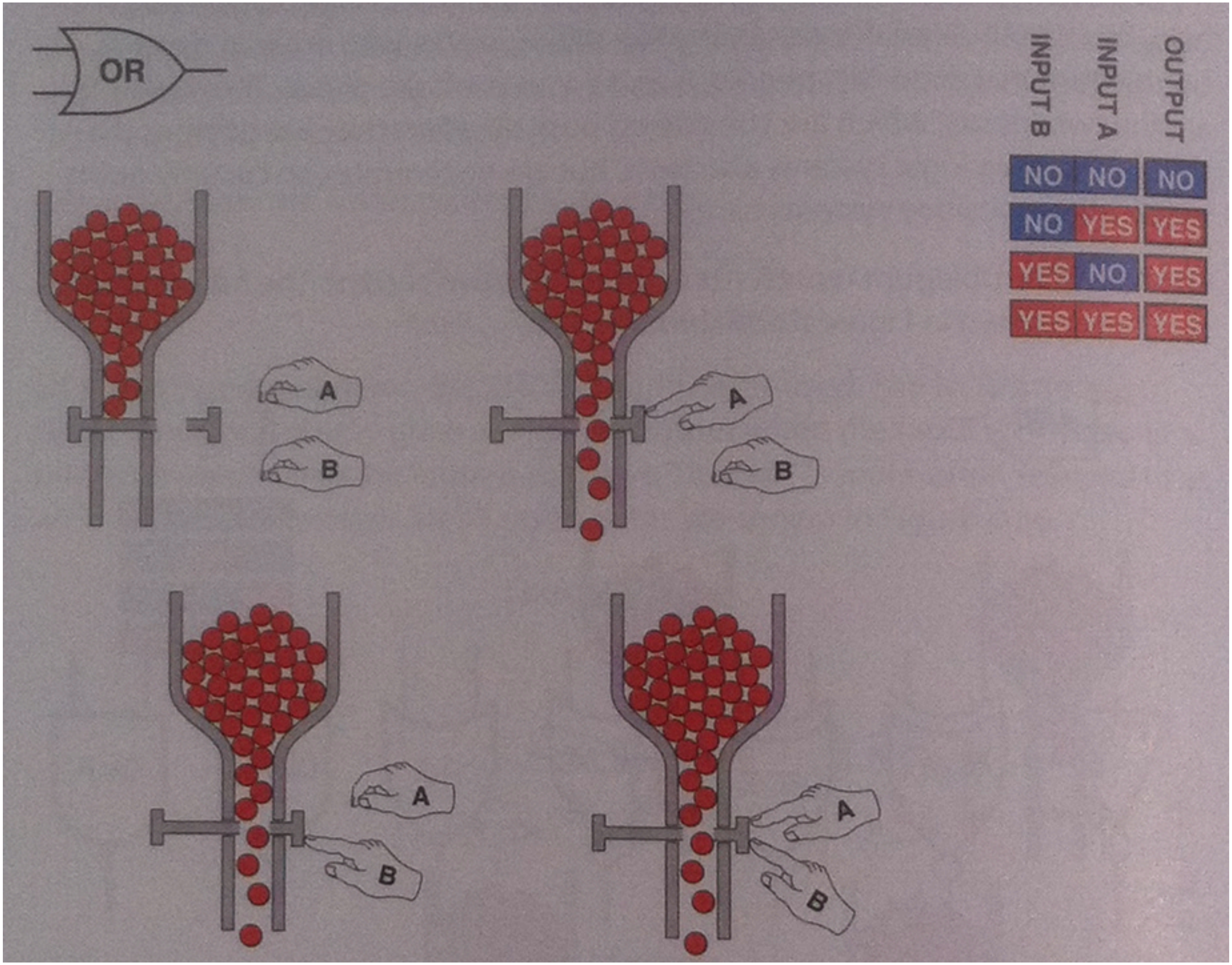


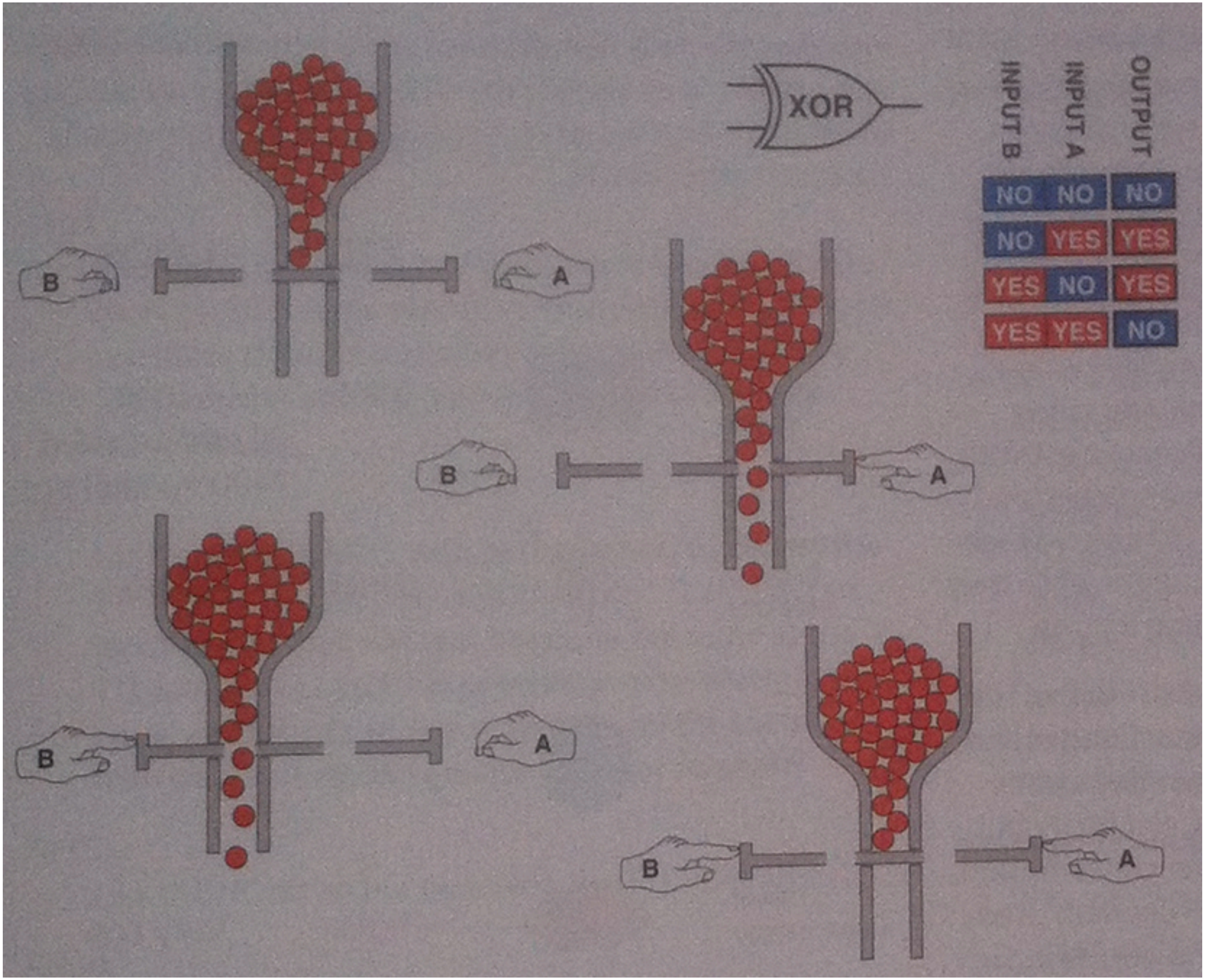
INPUT B	INPUT A	OUTPUT
NO	NO	NO
NO	YES	NO
YES	NO	NO
YES	YES	YES

[Platt 2009]



INPUT B	INPUT A	OUTPUT
NO	NO	NO
NO	YES	YES
YES	NO	YES
YES	YES	YES

[Platt 2009]



INPUT B	INPUT A	OUTPUT
NO	NO	NO
NO	YES	YES
YES	NO	YES
YES	YES	NO

[Platt 2009]

Questions?

THE END