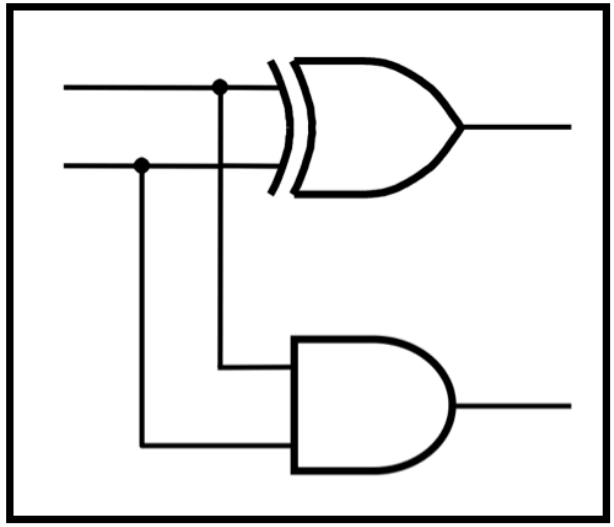


CprE 281: Digital Logic

Instructor: Alexander Stoytchev

http://www.ece.iastate.edu/~alexs/classes/

Intro and Overview

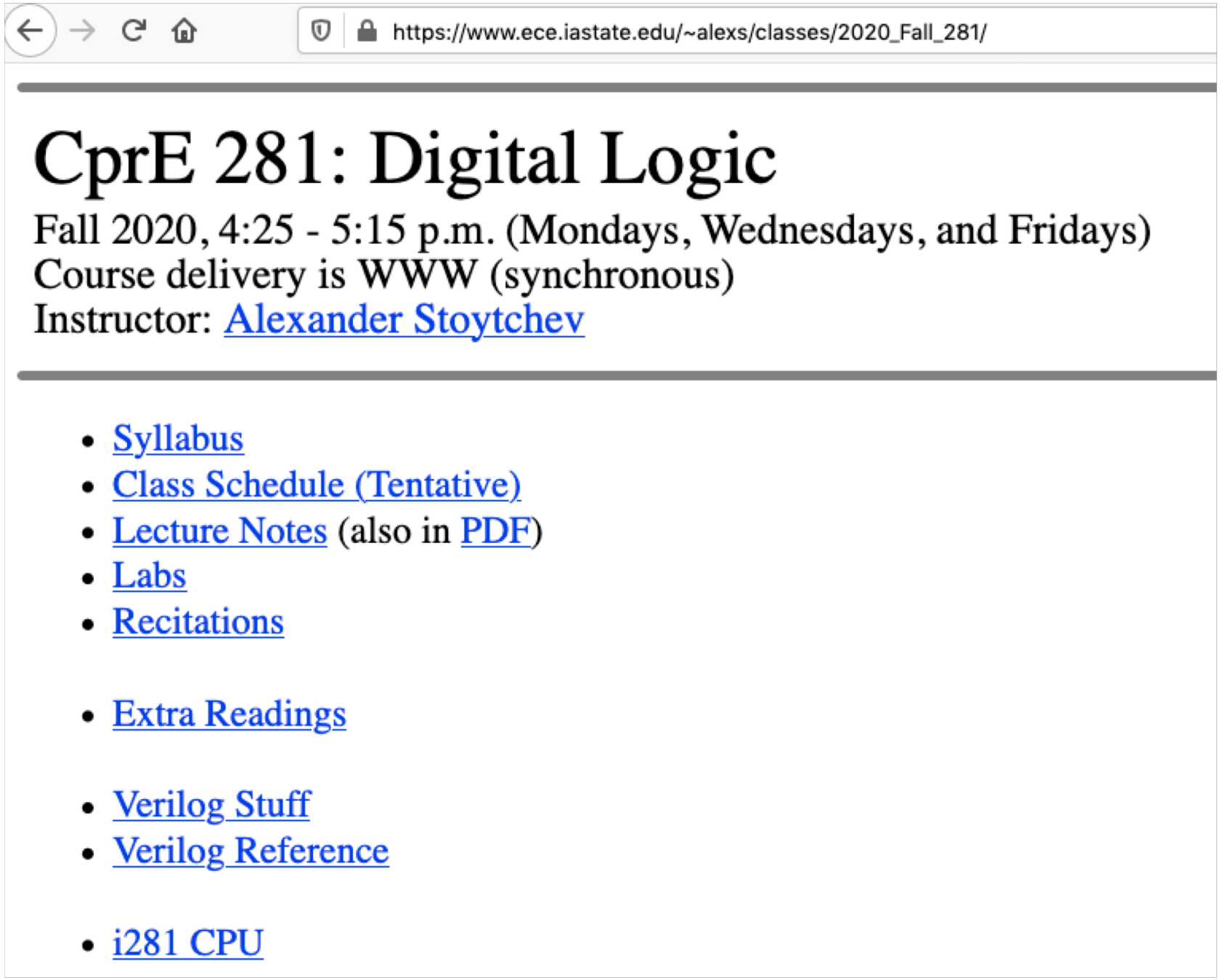
CprE 281: Digital Logic
Iowa State University, Ames, IA

Class Web Page

This is the official class web page:

http://www.ece.iastate.edu/~alexs/classes/2020_Fall_281/

The syllabus and other class materials are posted there.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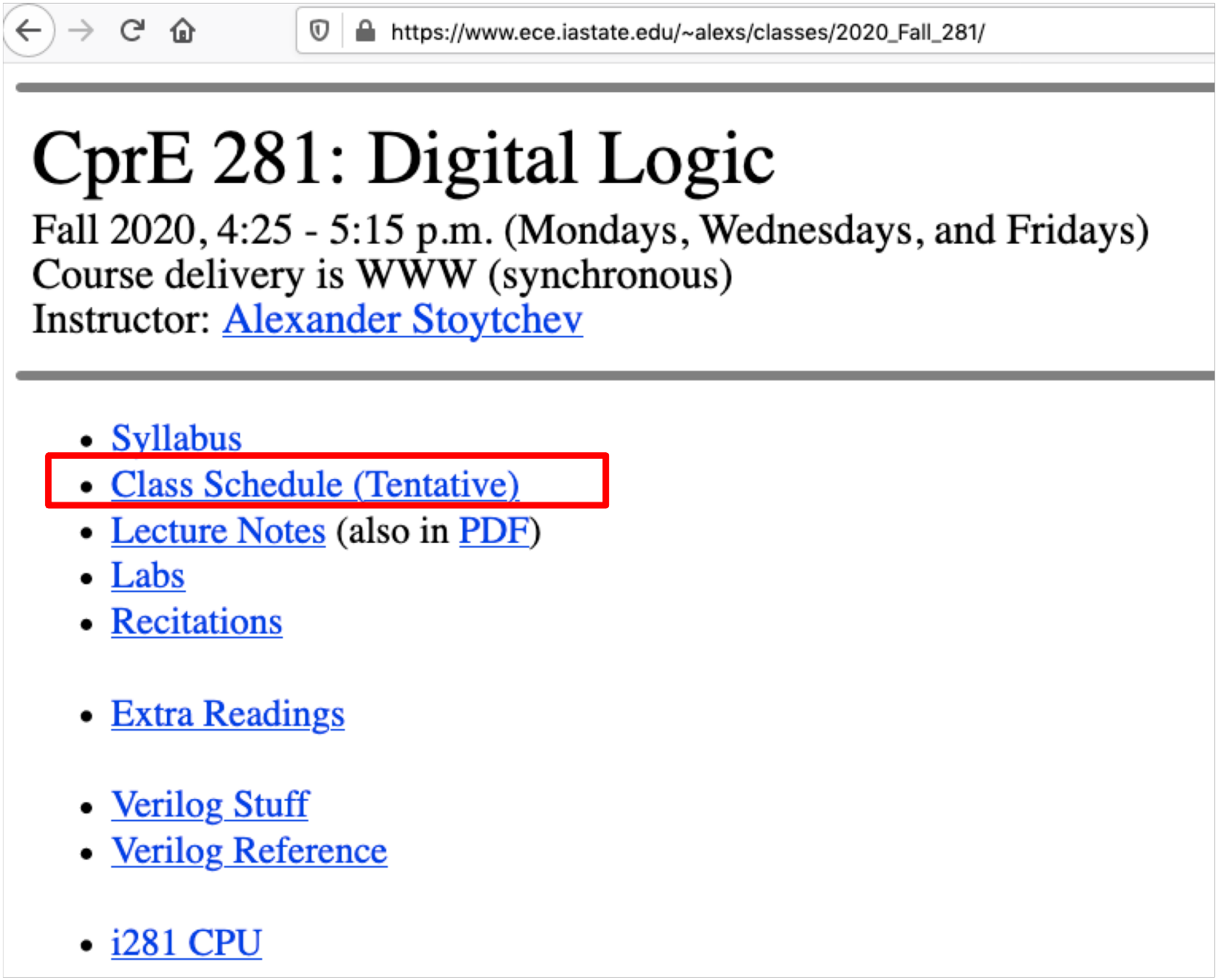
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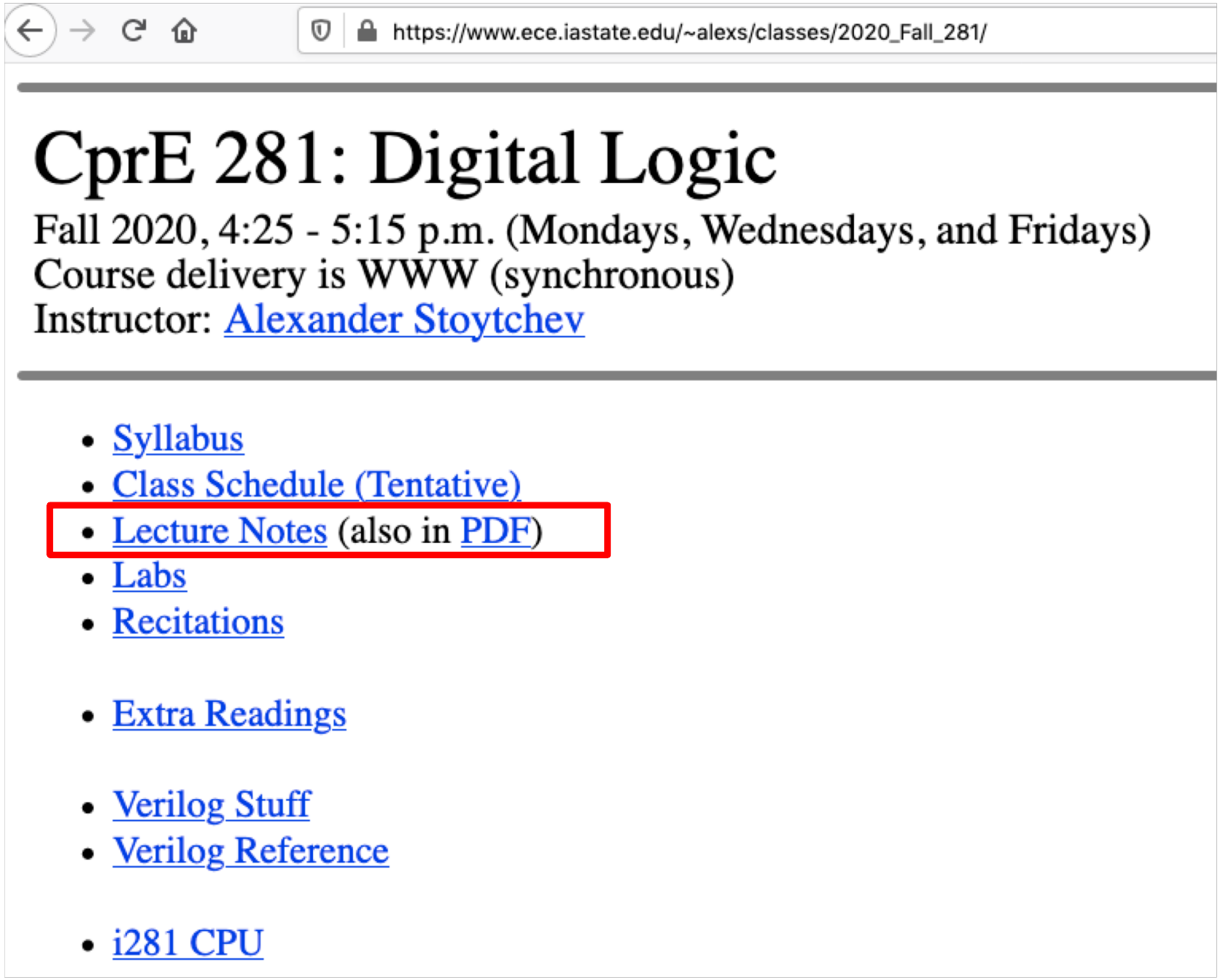
CprE 281: Class Schedule (Fall 2020)

Week	Day/Date		Topic	Readings	Homework	Lab
1	Monday	8/17	Introduction	1.1, 1.2, 1.3, 1.4		No Lab
	Wednesday	8/19	Binary Numbers	1.5, 1.6		
	Friday	8/21	Truth Tables & Logic Gates	2.1, 2.2, 2.3, 2.4		
2	Monday	8/24	Boolean Algebra	2.5	HW 1 due	Lab 1
	Wednesday	8/26	AND, OR, NOT	2.6		
	Friday	8/28	NAND, NOR	2.7		
3	Monday	8/31	Design Examples	2.8	HW 2 due	Lab 2
	Wednesday	9/2	Intro to Verilog	2.9, 2.10		
	Friday	9/4	Karnaugh Maps	2.11		
4	Monday	9/7	Minimization	2.12, 2.13	HW 3 due	Lab 3
	Wednesday	9/9	Functions and Circuits	2.14, 2.15, 2.16		
	Friday	9/11	Examples	2.17		
5	Monday	9/14	Addition of Unsigned Numbers	3.1, 3.2	HW 4 due	Lab 4
	Wednesday	9/16	Signed Numbers	3.3		
	Friday	9/18	Midterm #1			

6	Monday	9/21	Fast Adders	3.4, 3.5	HW 5 due	Lab 5
	Wednesday	9/23	Multiplication	3.6		
	Friday	9/25	Floating Point Numbers	3.7		
7	Monday	9/28	Multiplexers	4.1		Mini
	Wednesday	9/30	Decoders & Encoders	4.2, 4.3		Project
	Friday	10/2	Code Converters	4.4, 4.5		
8	Monday	10/5	Latches	5.1, 5.2, 5.3	HW 6 due	Lab 6
	Wednesday	10/7	D Flip-Flops	5.4		
	Friday	10/9	T Flip-Flops & JK Flip-Flops	5.5, 5.6, 5.7		
	Friday	10/9	* Midterm Grade Reports Due *			
9	Monday	10/12	Registers & Register Files	5.8	HW 7 due	Lab 7
	Wednesday	10/14	Counters	5.9, 5.10		
	Friday	10/16	Examples with Counters	5.11, 5.14, 5.17		

Week	Day/Date		Topic	Readings	Homework	Lab
10	Monday	10/19	Basic Design Steps	6.1	HW 8 due	Lab 8
	Wednesday	10/21	State-Assignment Problem	6.2		
	Friday	10/23	Midterm # 2			
	Friday	10/23	***DROP DEADLINE***			
11	Monday	10/26	Moore & Mealy Machines	6.3, 6.4	HW 9 due	Lab 9
	Wednesday	10/28	Serial Adder & Arbiter Circuit	6.5, 6.8		
	Friday	10/30	State Minimization	6.6		
12	Monday	11/2	Designing a Counter	6.7	HW 10 due	Lab 10
	Wednesday	11/4	Analysis of Syn. Seq. Circuits	6.9		
	Friday	11/6	ASM charts & Examples	6.10 – 6.13		
13	Monday	11/9	Register Machines		HW 11 due	Lab 11
	Wednesday	11/11	The i281 CPU			
	Friday	11/13	i281 Assembly Language			
14	Monday	11/16	Arithmetic Logic Unit & PC		HW 12 due	Lab 12
	Wednesday	11/18	Software-Hardware Interface			
	Friday	11/20	Final Review Session			
14	Saturday	11/21	FINAL EXAM @ 2:15-4:15pm	everything		No Lab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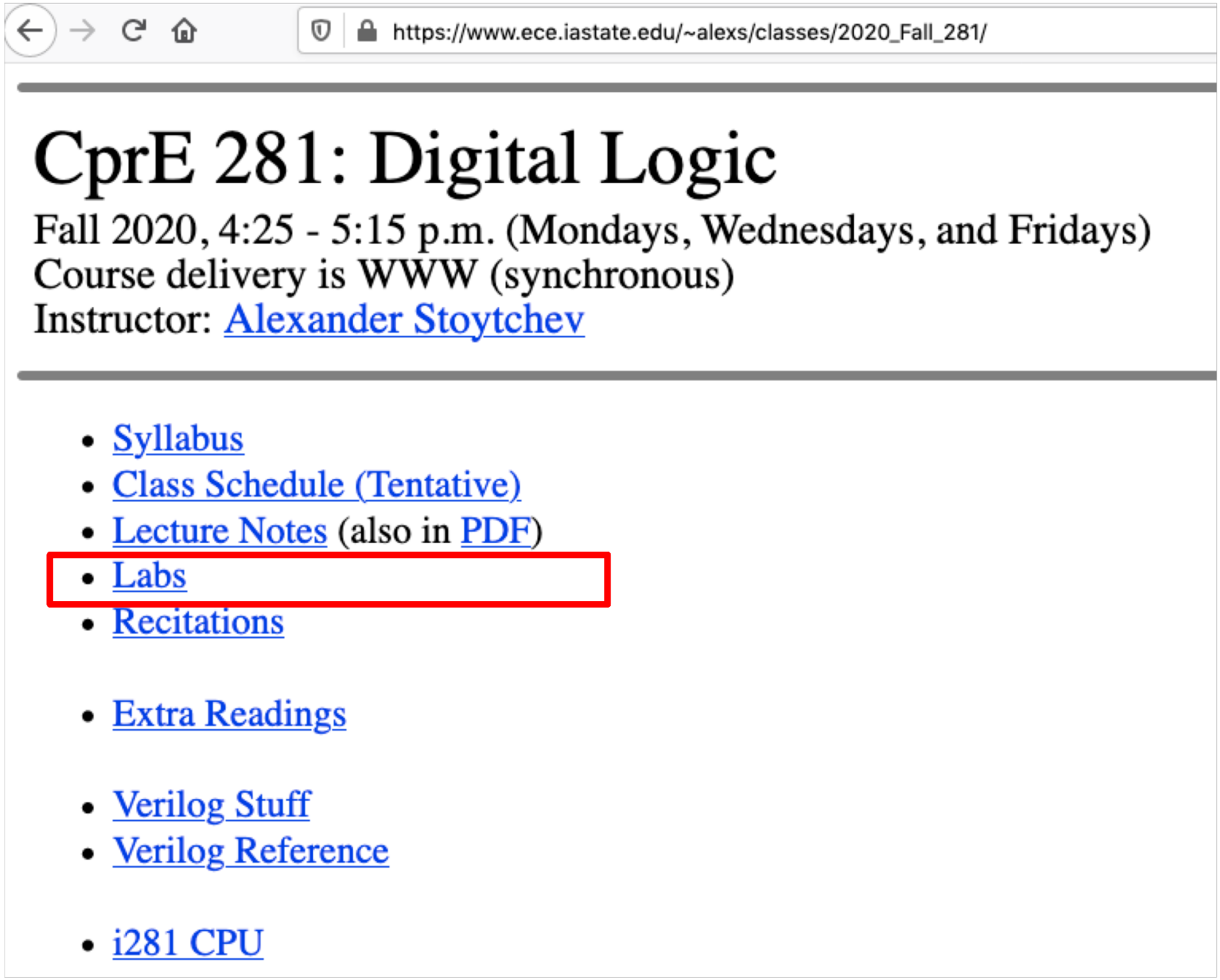
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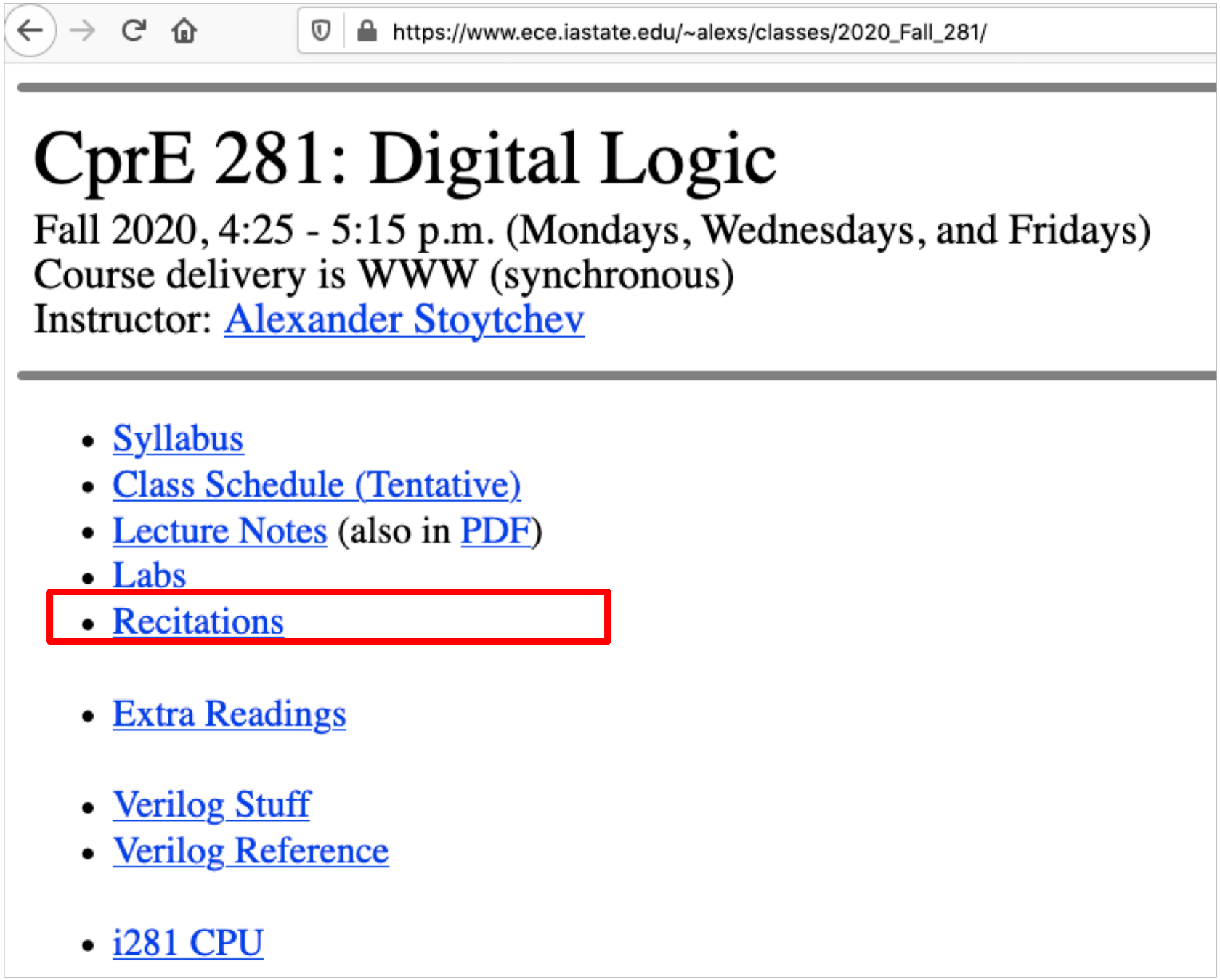
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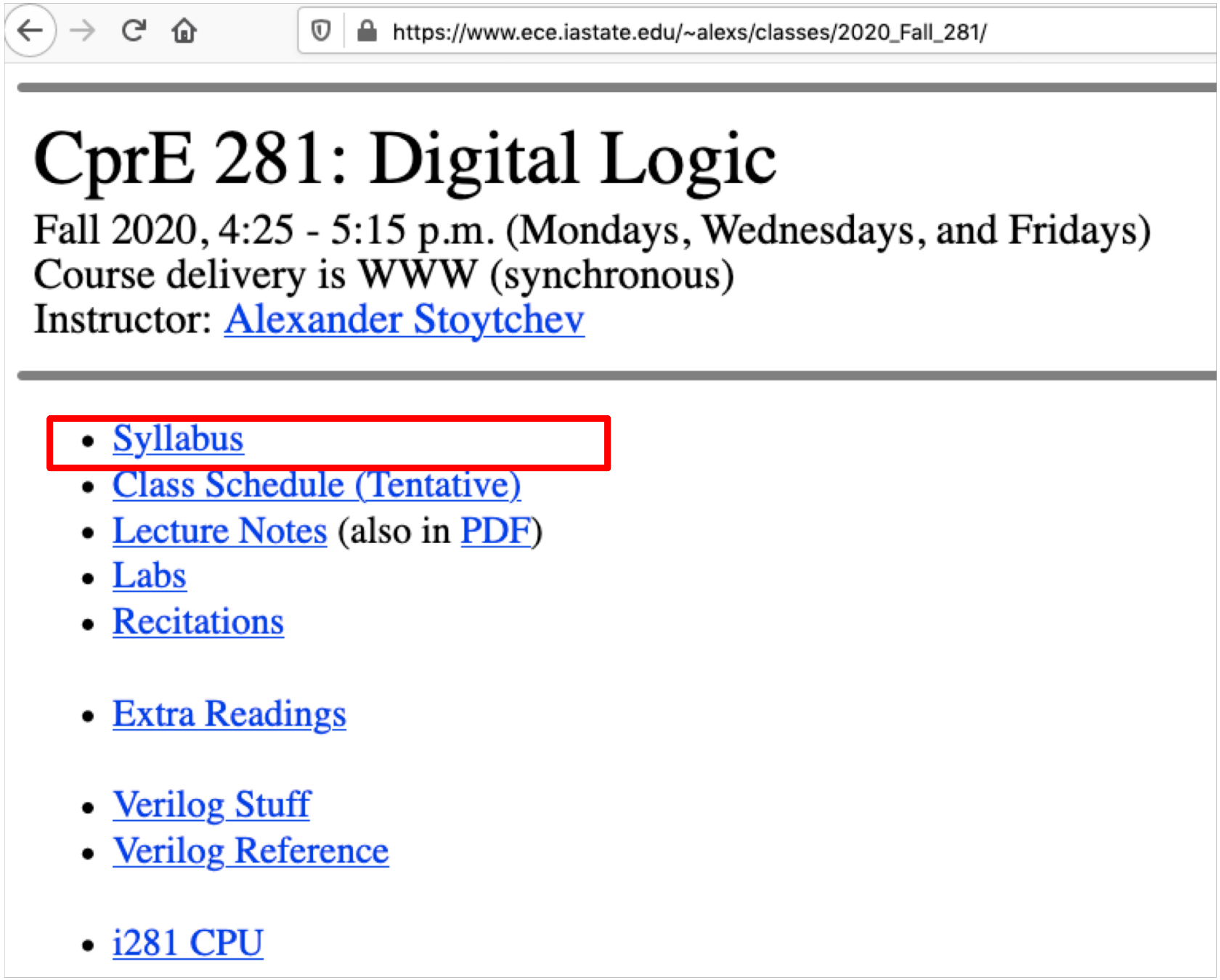
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Course Catalog Description

CprE 281: Digital Logic. Cr. 4. F.S. Prereq: sophomore classification
Number systems and representation. Boolean algebra and logic minimization. Combinational and sequential logic design. Arithmetic circuits and finite state machines. Use of programmable logic devices. Introduction to computer-aided schematic capture systems, simulation tools, and hardware description languages. Design of simple digital systems.

Learning Outcomes

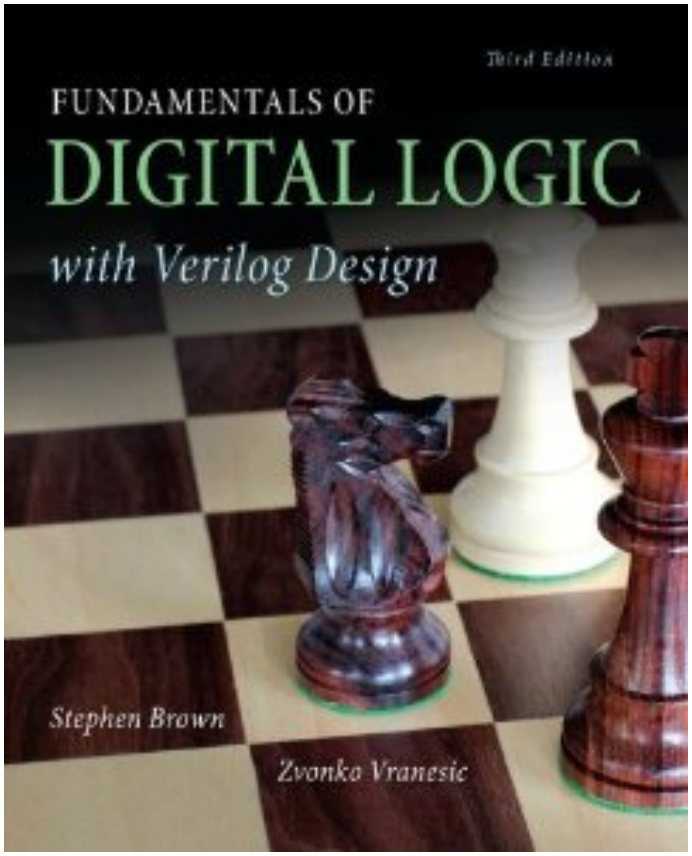
Students who successfully complete CprE 281 Digital Logic will have:

- Understanding of number systems and codes, and digital representation of data.
- Understanding of the general concepts in digital logic design, including logic elements, and their application in combinatorial and sequential logic circuit design quality.
- Familiarity with computer-aided schematic capture systems, simulation tools and hardware description language.
- Familiarity with programmable logic devices.

Learning Objectives

To introduce number systems and codes, digital representation of data, and to teach the general concepts in digital logic design, including logic elements, and their use in combinational and sequential logic circuit design. Students will also be introduced to computer-aided schematic capture systems, simulation tools and hardware description languages, and will use programmable logic devices.

Required Textbook



Title: **Fundamentals of Digital Logic with Verilog Design [3-rd edition]**
Author: **Stephen Brown and Zvonko Vranesic**
Edition: **Copyright 2013, 3-rd edition**
ISBN: **978-0073380544**
Publisher: **McGraw-Hill**

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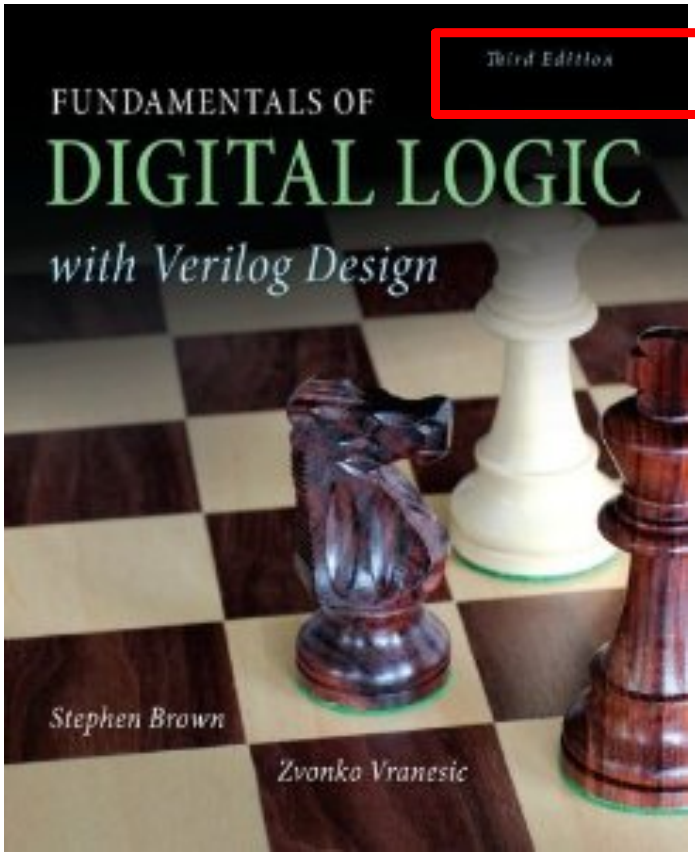

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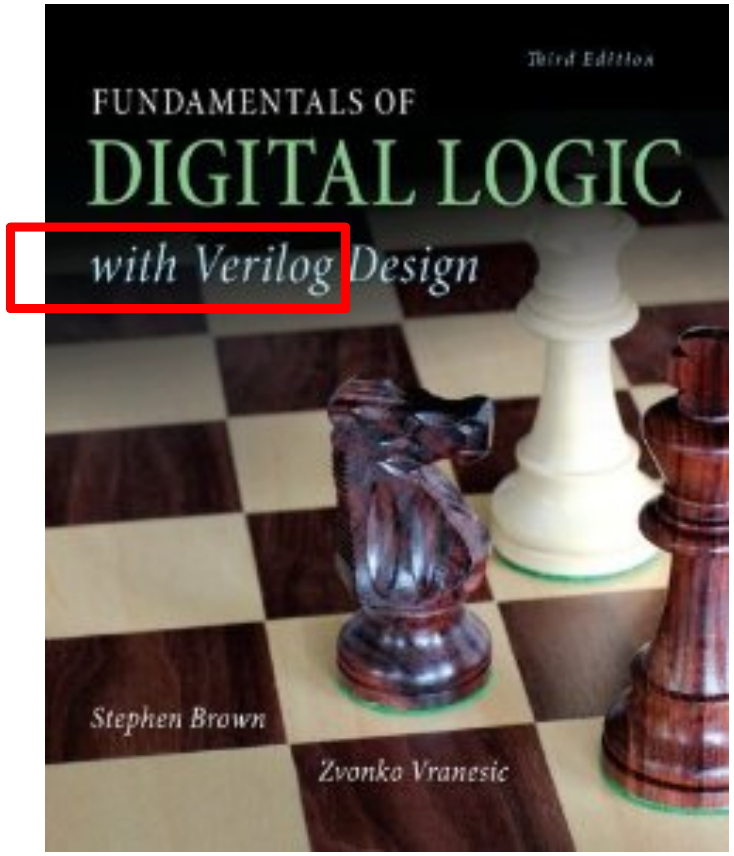

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Textbook (electronic version)

This course is enrolled in the Iowa State University Immediate Access Program. Immediate Access is a collaborative program where the University Book Store, faculty, and publisher have worked together to ensure access to the "Fundamentals of Digital Logic with Verilog" ebook the first day of class at a reduced price compared to the national average.

You can view the ebook after the instructor has published the course in Canvas. To view the ebook:

1. Click on the RedShelf Course Materials link on the Canvas course homepage.

2. Click on "View Course Materials" and follow the instructions to receive access to the ebook. (The ebook may not be available to view until the first day of class).

You will be automatically charged on your u-bill for this digital content. You will see the charge listed as CPR E 281 EBOOK 9781260640281 for $45.00. Students who drop the course within the first 10 days of class will receive a refund on their u-bill (5 days for courses 8 weeks or shorter). YOU DO NOT HAVE TO NOTIFY THE BOOKSTORE IF YOU DROP THE COURSE.

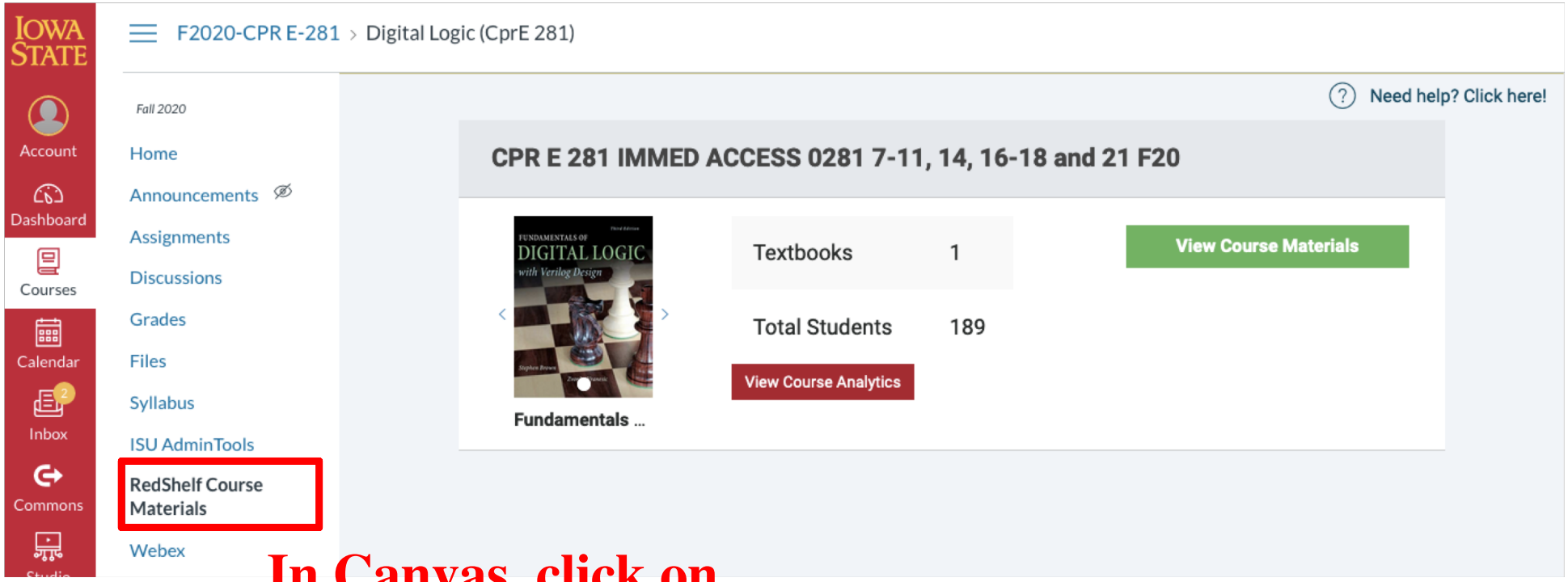
Textbook (electronic version)

Students may also choose to opt out of the program. Opting out does not mean you are dropping the course. It simply means you are choosing not to receive the digital content from the bookstore and you must find another way to acquire it in order to complete required homework assignments. Students have within the first 10 days of class to opt out and receive a refund to their u-bill (5 days for courses 8 weeks or shorter). To opt out, click on the Redshelf Course Materials link on the Canvas course homepage, then click on "View Your Course Materials", go to the bottom of the next page and click on the opt out link. Should you change your mind after opting out there will be an option to opt back in within the first 10 days of class (5 days for courses 8 weeks or shorter).You may not be able to use the opt out feature until your instructor has published this course in Canvas.

A $35.00 optional looseleaf will be available at the bookstore after the first 10 days of class. This looseleaf DOES NOT replace the digital content you receive in Immediate Access and is only available to students who remain opted into Immediate Access after the opt out period has ended.

For further questions about Immediate Access please email immediateaccess@iastate.edu.

Where is the eBook?



In Canvas, click on the RedShelf

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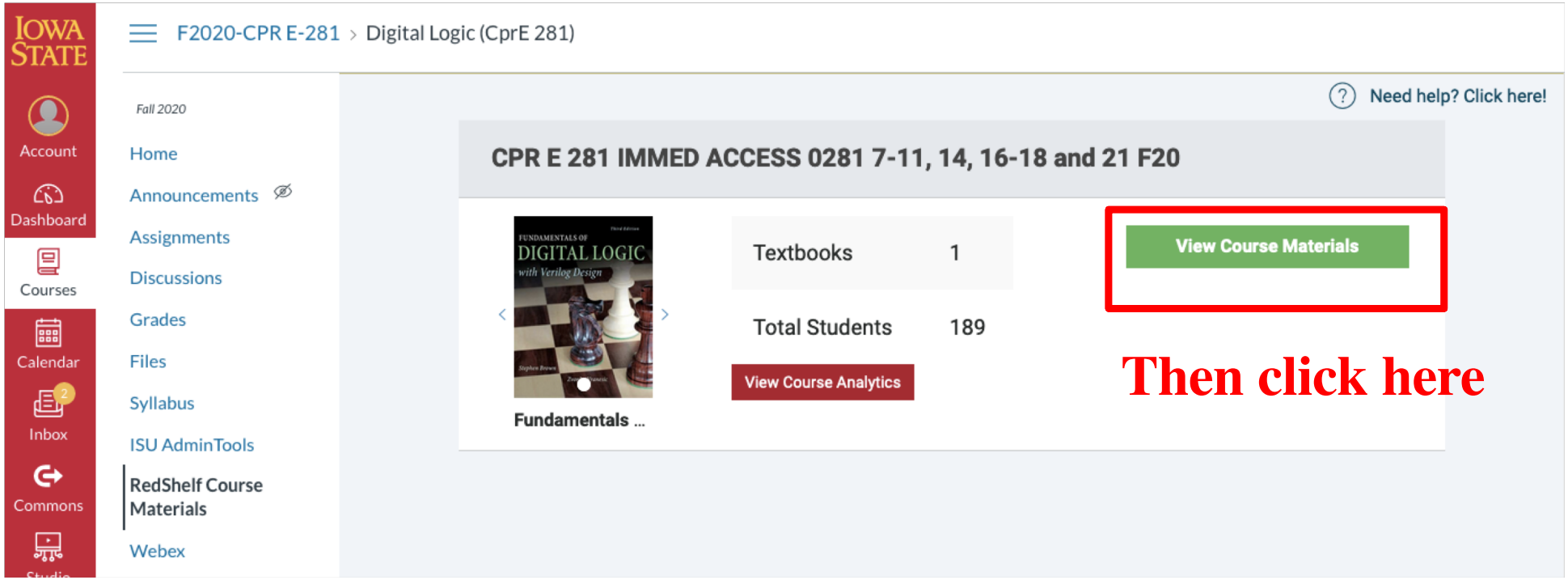
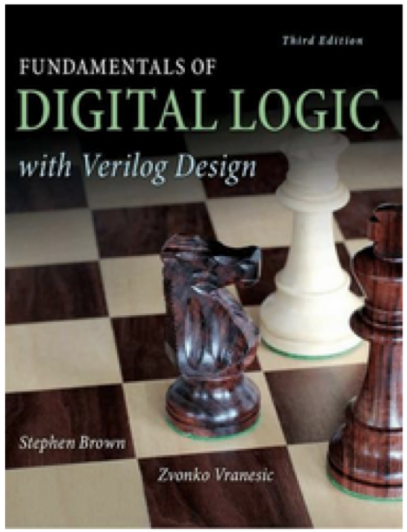


Fundamentals of Digital Logic with Verilog Design



How do eBooks work?

Fundamentals of Digital Logic with Verilog Design

Stephen Brown

Fundamentals of Digital Logic With Verilog Design is intended for an introductory course in digital logic design. The main goals ...

Days Remaining: 1806

Start Reading

And then click here

DRM Restrictions

Offline Access (100%)

Printing (20%)

Digital Book Features

If the course ends before your course materials expire, you will not lose access to your course materials. Visit isubookstore.redshelf.com, log in with your campus email address, and select "My Shelf" from the user menu to access your course materials.

level of the circuit's power supply. As we discuss in Appendix B, typical power-supply voltages in logic circuits range from 1 V DC to 5 V DC.

In general, all information in logic circuits is represented as combinations of 0 and 1 digits. Before beginning our discussion of logic circuits in Chapter 2, it will be helpful to examine how numbers, alphanumeric data (text), and other information can be represented using the digits 0 and 1.

1.5.1 BINARY NUMBERS

In the familiar decimal system, a number consists of digits that have 10 possible values, from 0 to 9, and each digit represents a multiple of a power of 10. For example, the number 8547 represents $8 \times 10^3 + 5 \times 10^2 + 4 \times 10^1 + 7 \times 10^0$. We do not normally write the powers of 10 with the number, because they are implied by the positions of the digits. In general, a decimal integer is expressed by an n-tuple comprising n decimal digits

$$D = d_{n-1}d_{n-2}\cdots d_1 d_0$$

which represents the value

$$V(D) = d_{n-1} \times 10^{n-1} + d_{n-2} \times 10^{n-2} + \cdots + d_1 \times 10^1 + d_0 \times 10^0$$

This is referred to as the *positional number representation*.

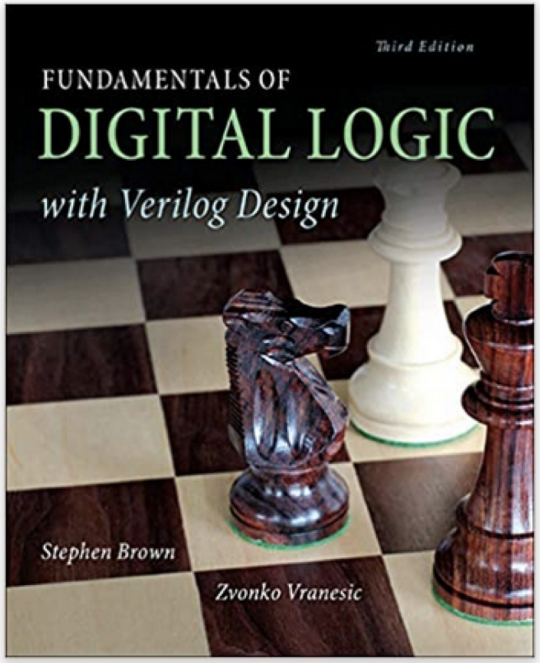
Or you can rent the book from Amazon

Fundamentals of Digital Logic with Verilog Design 3rd Edition

by Stephen Brown (Author), Zvonko Vranesic (Author)

4.0 out of 5 stars 25 ratings

Look inside



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Prerequisites

SOPHOMORE CLASSIFICATION

Star Wars (all episodes), The Matrix (all episodes)

Accessibility Statement

Iowa State University is committed to assuring that all educational activities are free from discrimination and harassment based on disability status. Students requesting accommodations for a documented disability are required to work directly with staff in Student Accessibility Services (SAS) to establish eligibility and learn about related processes before accommodations will be identified. After eligibility is established, SAS staff will create and issue a Notification Letter for each course listing approved reasonable accommodations. This document will be made available to the student and instructor either electronically or in hard-copy every semester. Students and instructors are encouraged to review contents of the Notification Letters as early in the semester as possible to identify a specific, timely plan to deliver/receive the indicated accommodations. Reasonable accommodations are not retroactive in nature and are not intended to be an unfair advantage. Additional information or assistance is available online at www.sas.dso.iastate.edu, by contacting SAS staff by email at accessibility@iastate.edu, or by calling 515-294-7220. Student Accessibility Services is a unit in the Dean of Students Office located at 1076 Student Services Building.

Harassment and Discrimination

Iowa State University strives to maintain our campus as a place of work and study for faculty, staff, and students that is free of all forms of prohibited discrimination and harassment based upon race, ethnicity, sex (including sexual assault), pregnancy, color, religion, national origin, physical or mental disability, age, marital status, sexual orientation, gender identity, genetic information, or status as a U.S. veteran. Any student who has concerns about such behavior should contact his/her instructor, Student Assistance at 515-294-1020 or email dso-sas@iastate.edu, or the Office of Equal Opportunity and Compliance at 515-294-7612.

Religious Accommodation

If an academic or work requirement conflicts with your religious practices and/or observances, you may request reasonable accommodations. Your request must be in writing, and your instructor or supervisor will review the request. You or your instructor may also seek assistance from the Dean of Students Office or the Office of Equal Opportunity and Compliance.

Required Technologies

This course will use Webex for synchronous online interactions. Visit the Webex learning tool guide to view the terms of service, privacy policy, accessibility statement, and steps for getting started with Webex. Some lectures may be recorded.

COVID-19
health and safety requirements

Students are responsible for abiding by the university's COVID-19 health and safety expectations. All students attending this class in-person are required to follow university policy regarding health, safety, and face coverings:

- wear a cloth face covering in all university classrooms, laboratories, studios, and other in-person instructional settings and learning spaces. Cloth face coverings are additionally required to be worn indoors in all university buildings, and outdoors when other people are or may be present where physical distancing of at least 6 feet from others is not possible. Students with a documented health or medical condition that prevents them from wearing a cloth, face covering should consult with Student Accessibility Services in the Dean of Students Office.

- ensure that the cloth face covering completely covers the nose and mouth and fits snugly against the side of the face.

- practice physical distancing to the extent possible.

COVID-19
health and safety requirements

- assist in maintaining a clean and sanitary environment.
- not attend class if you are sick or experiencing symptoms of COVID-19.
- not attend class if you have been told to self-isolate or quarantine by a health official.
- follow the instructor's guidance with respect to these requirements. Failure to comply constitutes disruptive classroom conduct. Faculty and teaching assistants have the authority to deny a non-compliant student entry into a classroom, laboratory, studio, conference room, office, or other learning space.

These requirements extend outside of scheduled class time, including coursework in laboratories, studios, and other learning spaces, and to field trips. These requirements may be revised by the university at any time during the semester.

COVID-19
health and safety requirements

In accordance with university policy, instructors may use a face shield while they are teaching as long as they are able to maintain 8 feet of physical distance between themselves and students during the entire instructional period. Some form of face covering must be worn at all times in learning spaces regardless of the amount of physical distancing.

Faculty may refer matters of non-compliance to the Dean of Students Office for disciplinary action, which can include restrictions on access to, or use of, university facilities; removal from university housing; required transition to remote-only instruction; involuntary disenrollment from one or more in-person courses; and other such measures as necessary to promote the health and safety of campus.

It is important for students to recognize their responsibility in promoting the health and safety of the Iowa State University community, through actions both on-and off-campus. The university's faculty asks that you personally demonstrate a commitment to our Cyclones Care campaign . Iowa State University's faculty support the Cyclones Care campaign and ask you personally to demonstrate a commitment to our campaign. Your dedication and contribution to the campaign will also protect your family, classmates, and friends, as well as their friends and families. Our best opportunity for a successful fall semester with in-person learning and extramural activities requires all of us to collaborate and fully participate in the Cyclones Care campaign.

Homeworks

There will be a total of 12 homework assignments. Each homework is worth 2 percent of your final grade. You will have more than a week to complete each one of them. These assignments will be used to emphasize and clarify important concepts discussed in the lectures.

All homeworks must be submitted in electronic form and uploaded to Canvas BEFORE the start of the lecture period on the day on which they are due.

Also, please write the following three on the first page: 1) your full name; 2) your student ID number; and 3) your lab section letter. If any of these three are missing, then you will lose 10% of your grade for that homework.

IMPORTANT: Due to the large size of this class we cannot and WILL NOT accept late homeworks. Period.

Labs

Unless stated otherwise there will be a 3-hour lab every week. The topics for the labs are posted on the lab schedule. The labs will be graded and they are an essential component of this class. Each lab is worth 2 percent of your final grade. There are 12 labs. You are expected to attend ALL labs.

Seating capacity in the lab is limited so please attend ONLY the section for which you are registered. Switching sections is not allowed.

Lab Sections

- Section 16: Tuesday 11:00 AM - 1:50 PM (Lab delivery is WWW, synchronous)
- Section 11: Tuesday 2:10 PM - 5:00 PM (Lab delivery is WWW, synchronous)
- Section 8: Wednesday 7:45 AM - 10:35 AM (Lab delivery is WWW, synchronous)
- Section 18: Wednesday 11:00 AM - 1:50 PM (Lab delivery is WWW, synchronous)
- Section 14: Thursday 11:00 AM - 1:50 PM (Lab delivery is WWW, synchronous)
- Section 17: Thursday 11:00 AM - 1:50 PM (Lab delivery is WWW, synchronous)
- Section 10: Thursday 2:10 PM - 5:00 PM (Lab delivery is WWW, synchronous)
- Section 7: Friday 11:00 AM - 1:50 PM (Lab delivery is WWW, synchronous)

The Labs Start Next Week

- **Please download and read the lab assignment for next week before you go to your lab section.**

- **You must answer the pre-lab questions before the start of the lab.**

- **The TAs will check your answers at the beginning of the lab.**

The Labs Start Next Week

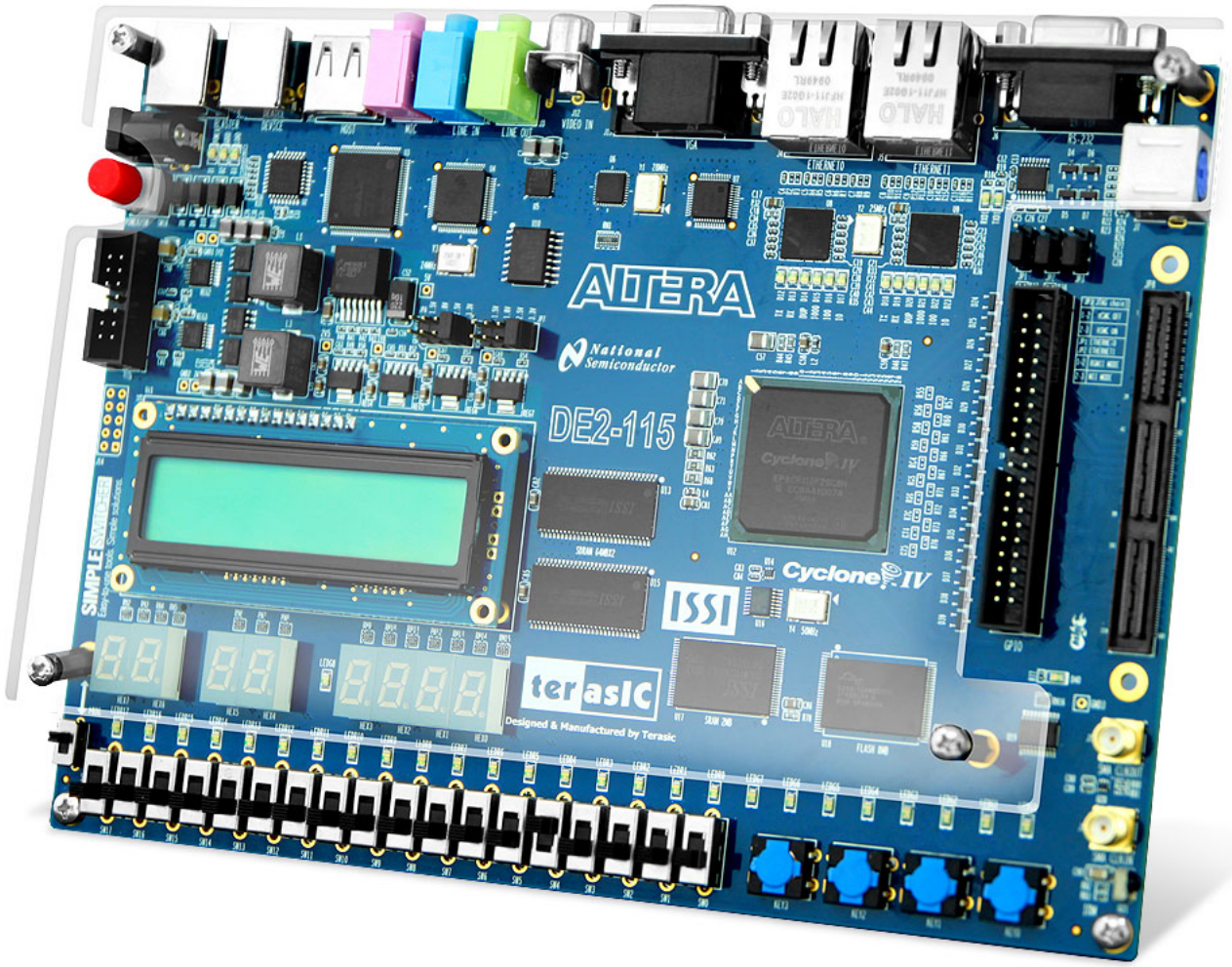

Figure 1.5 in the textbook: An FPGA board.

Midterm Exams

There will be two midterm exams for this class. The midterms are scheduled for:

Midterm 1: Friday Sep 18 from 4:25-5:15pm (during the lecture period)
Midterm 2: Friday Oct 23 from 4:25-5:15pm (during the lecture period)

Both midterms will we closed-book but open-notes (up to 3 letter-sized sheets of paper, typed or hand-written).

You may be required to go to the test center or use a proctoring software while taking each exam.

Final Exam

There will be a final exam during finals week.
The final exam is currently scheduled for Saturday November 21 @ 2:15 - 4:15 pm (tentative).

The exam will we closed-book but open-notes (up to 5 letter-sized sheets of paper, typed or hand-written).

You may be required to go to the test center or use a proctoring software while taking the final exam.

Policy on Collaboration

You are encouraged to form study groups and discuss the reading materials assigned for this class. You are allowed to discuss the homework assignments with your colleagues. However, each student will be expected to write his/her own solutions/code. Sharing of code is not allowed. No collaboration will be allowed during the exams.

IMPORTANT: Cheating, plagiarism, and other academic misconducts will not be tolerated and will be handled according to the ISU's academic dishonesty procedures.

Attendance

You are expected to attend ALL lectures and ALL labs. If you have a valid reason to miss a class (e.g., because you are ill) then it is your responsibility to find out what we have talked about in class, including any announcements that were made during class.

Class Rating

This class is rated PG-13 for some exposure to novel ideas, difficult problems, long and frustrating hours behind the keyboard, 800-page textbook, Muppet violence, the Quartus environment, and some HDL language. Parental involvement is not required and is strongly discouraged.

Appealing a Grade

You will have a two-week window of appeal after each homework/exam is graded and returned. The grade challenge must be in writing and must clearly state the specific problem on the homework/exam in question and the reason for your challenge. The written statement and the original exam must be submitted to the instructor during the two-week window. After two weeks the grade cannot be changed.

Grading Scale

95 - 100	= A
90 - 94	= A-
87 - 89	= B+
83 - 86	= B
80 - 82	= B-
77 - 79	= C+
73 - 76	= C
70 - 72	= C-
67 - 69	= D+
63 - 66	= D
60 - 62	= D-
0 - 59	= F

Grading Percentages

Homeworks:	(12 x 2%)	24%
Labs:	(12 x 2%)	24%
Mini Project:		4%
Midterm Exam 1:		15%
Midterm Exam 2:		15%
Final Exam:		20%
TOTAL:		102%

Small print*

*** The instructor reserves the right to change any and all aspects of this class for whatever reason or no reason at all (a.k.a., academic freedom).**

Questions?

THE END