Cpr E 281 LAB11
ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

Finite State Machines

PRELAB!

Read the entire lab and **complete** the prelab questions (Q1-Q2) on the report template and submit your completed questions on Canvas **before** your lab time. You will submit this report again once you have completed the lab.

1.0 Objectives

In this lab, you will create circuits that function as finite state machines. Read Chapter 6 of your textbook and complete the prelab before you come to the lab.

2.0 A Simple Counting Device

For this step, you are to design a device that simply cycles through six states. It will have four inputs: an input **Clock** for the clock, an input **PRN** connected to the PRN input of each DFF, an input **CLRN** connected to the CLRN input of each DFF, an input ***w*** which will keep the current state if low and advance to the next state if high. The output **Out** will be a bus that represents the present state. The device is a modulo-6 counter. The design method will be similar to that for the modulo-8 counter in Section 6.7 of your textbook.

Fill in the state-assigned table on the report template and use it to design the circuit.

Use D flip-flops for the device's memory. The output needs to be a bus that represents the current count. This is so ModelSim will render the count as a hexadecimal number instead of individual wires. Refer to Lab6 for more information on busses.

Create a ModelSim project for lab11. Then use ModelSim and the **Lab11.do** DO file to verify your design. When you are convinced your design is working correctly, include screenshots of your design and the simulations in the lab report.

3.0 A Simple Counter

You will now design a different kind of counter. Again, modeling this device as a finite state machine, create a counter that repeatedly counts 0, 2, 4, 5, 0, 2, 4, 5, and so on. This device will have the same inputs as the device in section 2.0: an input **Clock** for the clock, an input **PRN** connected to the PRN input of each DFF, an input **CLRN** connected to the CLRN input of each DFF, an input ***w*** which will keep the current state if low and advance to the next state if high. The output **Out** will be a bus that represents the current count.

Fill in the state-assigned table on the report template and use it to design the counter. To simplify the block diagram, we ask you to implement the next state logic and output logic using Verilog, see Figure 1. Use D flip-flops for the device's memory.

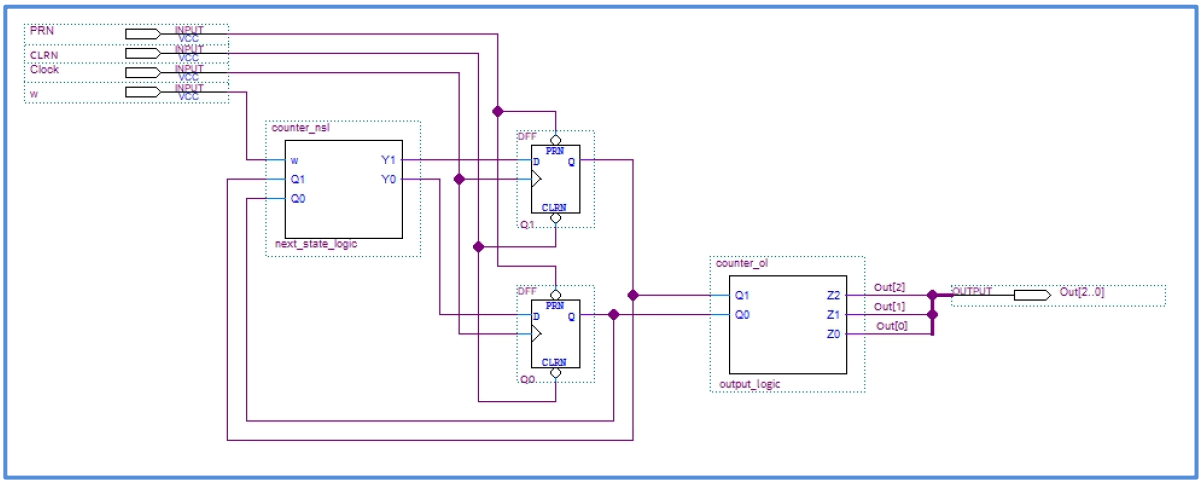

Figure 1: A simple counter

Create a new project and use ModelSim and the **Lab11.do** DO file to verify your design. When you are convinced your design is working correctly, include screenshots of your design and the simulations in the lab report.

4.0 Complete

You are now done with this lab. Close all lab files, exit Quartus Prime, log off the computer and submit your report to Canvas. **Don't forget to include your name and your lab section number**.