Name & Std. No.:\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ Lab Section:\_\_\_\_

Date:\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

**Submission Instructions:**

**Prelab:**

1. **Complete the prelab**
2. **Submit this report with the prelab completed to Canvas before your lab starts**

**Lab:**

1. **Complete the lab according to the instructions**
2. **Take screenshots of your ModelSim waveform (note: to receive points your NetID has to be present in the screenshot) and insert them into this document.**
3. **Include screenshots of any related block design files or Verilog files in the report**
4. **Complete this report and reupload it to Canvas**

**PRELAB:**

*Complete the prelab and make sure you have your designs and circuit diagrams ready before the lab session. You may refer to your text book, Chapter 6.*

**Q1.** Design a simple counting device (Section 2.0).

Number of States: \_\_\_\_\_\_\_\_\_\_

Number of State Variables: \_\_\_\_\_\_\_\_

**State Table: State-Assigned Table:**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Present State | Next State | | Output |  | Present State | Next State | | Output |
| w=0 | w=1 |  | w=0 | w=1 |  |
| A | A | B |  |  | 000 | 000 | 001 | 000 |
| B | B | C |  |  |  |  |  |  |
| C | C | D |  |  |  |  |  |  |
| D | D | E |  |  |  |  |  |  |
| E | E | F |  |  |  |  |  |  |
| F | F | A |  |  |  |  |  |  |

Canonical SOP Expressions for Next State Logic:

Simplified Next State Logic Expressions:

Circuit Diagram:

**Q2.** Design a simple counter (Section 3.0).

Number of States: \_\_\_\_\_\_\_\_\_\_

Number of State Variables: \_\_\_\_\_\_\_\_

**State Table: State-Assigned Table:**

|  |  |  |  |
| --- | --- | --- | --- |
| Present State | Next State | | Output |
| w=0 | w=1 |
| A | A | B | 0 |
| B | B | C | 2 |
| C | C | D | 4 |
| D | D | A | 5 |

|  |  |  |  |
| --- | --- | --- | --- |
| Present State | Next State | | Output |
| w=0 | w=1 |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |

Canonical SOP Expressions for Next State Logic:

Simplified Logic Expressions:

Next State Logic Verilog Code:

module circuit\_nsl(w, Q1, Q0, Y1, Y0);

<<< insert code here >>>

endmodule

Output Logic Verilog Code:

module circuit\_ol(Q1, Q0, Z2, Z1, Z0);

<<< insert code here >>>

endmodule

**LAB:**

**2.0 A Simple Counting Device**

Screenshots:

<<<Insert a screenshot of your module-6 counter BDF here>>>

<<< Insert a screenshot of your waveform for your modulo-6 counter here>>>

**Graphical user interface, application

Description automatically generated**

**3.0 A Simple Counter**

Screenshots:

<<<Insert a screenshot of your simple counter here>>>

<<<Insert a screenshot of your next state logic here>>>

<<<Insert a screenshot of your output logic here>>>

<<< Insert a screenshot of your waveform for your simple counter here>>>

**Graphical user interface, application

Description automatically generated**