Cpr E 281 LAB 09
ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

Designing Latches and Flip-Flops

PRELAB!

Read the entire lab and **complete** the prelab questions (Q1-Q5) on the report template and submit your completed questions on Canvas **before** your lab time. You will submit this report again once you have completed the lab.

1.0 Objectives

In this Lab you will design the following storage elements:

- Basic SR Latch
- D Latch
- D Flip-Flop

The objective is to observe, analyze and understand the working and the timing behavior of these devices. You will do all the designs in this lab using a schematic block diagram. Refer to Sections 5.1 through 5.4, and complete the circuit diagrams before you come to the lab.

2.0 Basic SR Latches

Information on a Basic SR Latch can be found in Section 5.1 of the textbook. For the first step ***lab9step1***, build a Basic SR Latch with NOR gates using a block diagram/schematic file. This circuit is given in Figure 5.4a of your textbook. Name the inputs ***S*** and ***R***; name the outputs ***Q*** and ***Qn***.

Use ModelSim and the **lab9step1.do** DO file to observe the behavior of the latch. Use the results to complete the characteristic table on the report template. When you are convinced that the latch is performing as predicted, take screenshots of your BDF file and the ModelSim waveform to include in your report

Since latches and other memory devices can be built using either NAND or NOR gates, build another SR latch by replacing the NOR gates with NAND gates. Change the ***R*** input to ***S*** and the ***S*** input to ***R***. Place an inverter on each input to create the ~S~R case. Use ModelSim and the **lab9step1.do** DO file again to observe the behavior of the latch. Use the results to complete the characteristic table on the report template. When you are convinced that the latch is performing as predicted, take screenshots of your BDF file and the ModelSim waveform to include in your report

3.0 D Latches

In a new project ***lab9step2*** build a Gated D Latch using NAND gates and a NOT gate. Refer to Section 5.3 for a detailed explanation of D Latches. Figure 5.7a shows how to build a D Latch using NAND gates and a NOT gate. Once you have built the latch, label the inputs ***Clk*** and ***D***, and outputs ***Q*** and ***Qn***. Use ModelSim and the **lab9step2and3.do** DO file to observe the behavior of the latch. When you are convinced that the latch is performing as predicted and you are confident you understand its behavior, complete the timing diagram on the report template. Additionally, take screenshots of your BDF file and the ModelSim waveform to include in your report. Note: you may need to zoom out or take multiple screenshots of the ModelSim waveform due to its length.

Create a **Symbol** for this Latch.

4.0 D Flip-Flops

Refer to Section 5.4 for a detailed explanation of D Flip-Flops.

In a new project, ***lab9step3a,*** use the Gated D Latch you built to design a Negative-Edge-Triggered Master-Slave D Flip-Flop. Section 5.4.1 discusses this design. Refer to Figure 5.9a. Use ModelSim and the **lab9step2and3.do** DO file to observe the behavior of the flip-flop. When you are convinced that the flip-flop is performing as predicted and you are confident you understand its behavior, complete the timing diagram on the report template. Additionally, take screenshots of your BDF file and the ModelSim waveform to include in your report. Note: you may need to zoom out or take multiple screenshots of the ModelSim waveform due to its length.

In a new project (***lab9step3b***) you will design a Positive-Edge-Triggered D Flip-Flop using NAND gates. Section 5.4.2 discusses this design. Please use Figure 5.11a as a guide for this step. Use ModelSim and the **lab9step2and3.do** DO file to observe the behavior of the flip-flop. When you are convinced that the flip-flop is performing as predicted and you are confident you understand its behavior, complete the timing diagram on the report template. Additionally, take screenshots of your BDF file and the ModelSim waveform to include in your report. Note: you may need to zoom out or take multiple screenshots of the ModelSim waveform due to its length.

5.0 Complete

You are now done with this lab. Close all lab files, exit Quartus Prime, log off the computer and submit your report to Canvas. **Don't forget to include your name and your lab section number**.