Cpr E 281 LAB08
ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

Designing Shifters with Multiplexers

PRELAB!

Read the entire lab and **complete** the prelab questions (Q1-Q3) on the report template and submit your completed questions on Canvas **before** your lab time. You will submit this report again once you have completed the lab.

1.0 Objectives

In Lab 4 you designed a multiplexer. In this lab you will learn to design shifters using multiplexers. You will design a 1-bit 4-to-1 Multiplexer in Verilog. Then you will use this multiplexer to build a shifter.

2.0 Multiplexers

2.1 A 4 to 1 Multiplexer (1-bit)

First, start a new project (***mux4to1***) and start a new Verilog file. Save this file as ***mux4to1.v***. The following is the Verilog code for a 1-bit 2 to 1 multiplexer. When the selector is 0 the output f is i0 and when the selector is 1 the output is i1.

```
module mux2to1(W0, W1, S, F);
       input W0, W1, S;
       output F;
       assign F = S ? W1 : W0;
endmodule
```

Modify this code to build a 1-bit 4-to-1 multiplexer. The multiplexer will have the following specification (note that S is a two bit bus, see the following two sections):

- Four 1-bit data inputs, W0, W1, W2 and W3.
- One 2-bit selector input, S [1:0].
- One 1-bit output, F.
- When S [1:0] = 00 the output will be W0.
- When S [1:0] = 01 the output will be W1.
- When S [1:0] = 10 the output will be W2.
- When S [1:0] = 11 the output will be W3.

For a detailed explanation of multiplexers please refer to the textbook. Also, read and understand any code that you may find in your textbook for multiplexers. *Note: It will be easier to reuse this code if you do not use a bus for the W inputs.*

Use ModelSim to test your code using the **mux4to1sim.do** file. When you are confident that your code is correct, take screenshots of the result and include it in your lab report.

IMPORTANT: Once you are done create a default symbol for your mux4to1 so that you can use it in section 3.

2.2 Bus Notation in Schematic Files

To create a bus in a schematic file (i.e. block design files) you will use the following syntax on an input/output input pin:

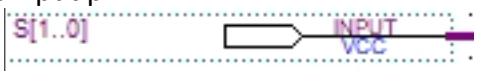


Fig 1. A Schematic Bus

The example above creates a bus input named S that is two bits wide. Note that there are two periods between the numbers in the brackets. This indicates that there is a wire in bus line 1 and a wire in bus line 0. This also indicates that bus line 1 is more significant than bus line 0.

To connect an input/output bus to blocks in a block design file, use the orthogonal bus tool.

2.3 Bus Notation in Verilog Files

To create a bus in a Verilog you have to use the Verilog bus syntax. See the example below:

```
module bus_input (A1, A2, B, Z1, Z2);
        input A1, A2;
        input [1:0] B;
        output Z1, Z2;

        assign Z1 = B[0] & A1;
        assign Z2 = B[1] & A2;
endmodule
```

The Verilog syntax uses a semi-colon to indicate a bus instead of two periods. Note that each bus needs to be defined on its own line which is separate from other busses of different widths and single bit inputs/outputs. To access a certain bus line, use the following syntax:

- `B[index]`

B is the name of the bus and **index** is the index of the bus line you want to access.

3.0 Shifters

3.1 Designing a Shifter

You will now design a device called a shifter. A Shifter is built from multiplexers and shifts the outputs, based on the select signals. For this shifter, you will use the 1-bit 4-to-1 multiplexer from Section 2.1. A shifter has the following inputs and outputs:

X3, X2, X1, X0	Primary Inputs
X_1, X_2, X_3	Cascading Inputs
S[1], S[0]	Shift Count
F3, F2, F1, F0	Fixed Outputs

The shifter outputs the inputs shifted to the left 0, 1, 2, or 3 places as indicated by the 2-bit shift count (select signals). The table below summarizes the behavior:

S[1]	S[0]	F3	F2	F1	F0
0	**0**	X3	X2	X1	X0
0	**1**	X2	X1	X0	X_1
1	**0**	X1	X0	X_1	X_2
1	**1**	X0	X_1	X_2	X_3

Example:

Let the inputs have the values below:

X3	X2	X1	X0	X_1	X_2	X_3
0	1	1	0	1	0	1

If the shift count is 00, the output would be:

F3	F2	F1	F0	X_1	X_2	X_3
0	1	1	0	1	0	1

If we shifted left ONE position – i.e., shift count is 01 then the output would be:

X3	F3	F2	F1	F0	X_2	X_3
0	1	1	0	1	0	1

The result makes it look like the **Shift Count** moves the window for the output!

To develop this Shifter, start with a new block diagram. Name it as your top-entity-file. The default should be ***lab8step1*.bdf**.

Hint:

To complete the shifter design, you will need four 1-bit 4-to-1 multiplexers, one for each output of the shifter. As is evident from the table summarizing the behavior of a shifter, the output bit F3 of the shifter can be X3, X2, X1 or X0 depending on the value of the shift count. A 4-to-1 multiplexer allows choosing from X3, X2, X1 and X0 based on the value of the shift count.

For this circuit you will only place **one output pin** on the block diagram and name it **F[3..0]**. Next create a small node line (orthogonal node tool), one on the output of each mux. Then run a bus line (orthogonal bus tool) to the output pin and connect each node line to the bus line. You should now have the output of each mux connected to the same bus line via a node line. Next you must label each node line to establish its position in the bus. To do this simply right click the node line and give it a name. An example is shown below in **Figure 1**.

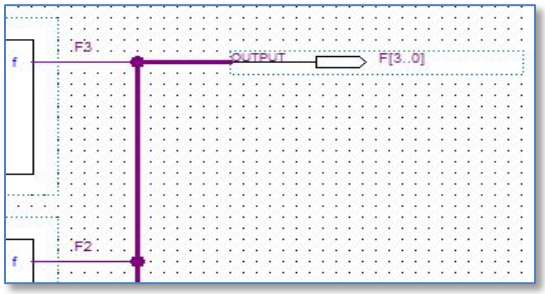
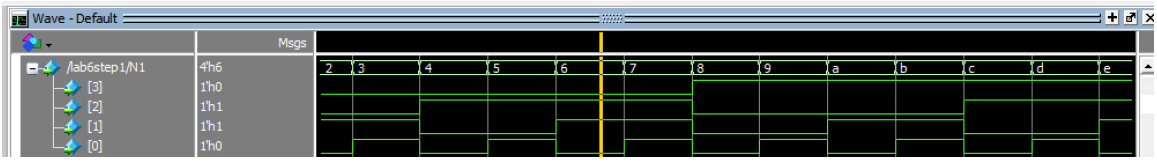


Figure 1: Node Line to Bus Line Connections

3.2 Simulation of the Shifter

Once your circuit is ready, compile it, and then simulate it on ModelSim. Use a DO file to simulate the shifts from the table in **Q3** (See *Using DO files in ModelSim* from Lab03).

Once you verified your circuit, follow the table you filled out for prelab **Q3** and demonstrate the proper operation of your shifter to the TA. Include the DO file and a screenshot of your results in your report. **IMPORTANT:** click on the plus by the output F to show the waveform for each bit. See the example below for a similar output.



4.0 Complete

You are now done with this lab. Close all lab files, exit Quartus Prime, log off the computer and submit your report to Canvas. **Don't forget to include your name and your lab section number**.