# Cpr E 281 LAB5 ELECTRICAL AND COMPUTER ENGINEERING IOWA STATE UNIVERSITY

#### Lab 5 Answer Sheet

Name and Student ID:	Lab Section:
Date:	
Submission Instructions:	
Prelab:	

- 1. Complete the prelab
  - 2. Submit this report with the prelab completed to Canvas before your lab starts

#### Lab:

- 1. Complete the lab according to the instructions
- 2. Take screenshots of your ModelSim waveform (note: to receive points your NetID has to be present in the screenshot) and insert them into this document.
- 3. Include screenshots of any related block design files or Verilog files in the report
- 4. Complete this report and reupload it to Canvas

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#### PRELAB:

**Q1.** Use Figure 1 and the table below to fill in the truth table on the next page.

Display	X <sub>0</sub>	X <sub>1</sub>	X <sub>2</sub>	<b>X</b> <sub>3</sub>
	0	0	0	0
 	1	0	0	0
2	0	1	0	0
3	1	1	0	0
닉	0	0	1	0
5	1	0	1	0
8	0	1	1	0
-	1	1	1	0

<b>X</b> <sub>3</sub>	$X_2$	$X_1$	$X_0$	Display
1	0	0	0	
1	0	0	1	
1	0	1	0	70
1	0	1	1	_Ū
1	1	0	0	الالا
1	1	0	1	-⊡
1	1	1	0	
1	1	1	1	

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Хз	X <sub>2</sub>	<b>X</b> <sub>1</sub>	Χo	Α	В	С	D	E	F	G
0	0	0	0	0	0	0	0	0	0	1
0	0	0	1							
0	0	1	0							
0	0	1	1							
0	1	0	0							
0	1	0	1							
0	1	1	0							
0	1	1	1							
1	0	0	0							
1	0	0	1							
1	0	1	0							
1	0	1	1							
1	1	0	0							
1	1	0	1							
1	1	1	0							
1	1	1	1							

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**Q2.** Write the verilog code for the 7-Segment Display Decoder based on the truth table from Q1. You only need to write the skeleton code (i.e., a code which shows only a rough outline and no unnecessary or repetitive details) below.

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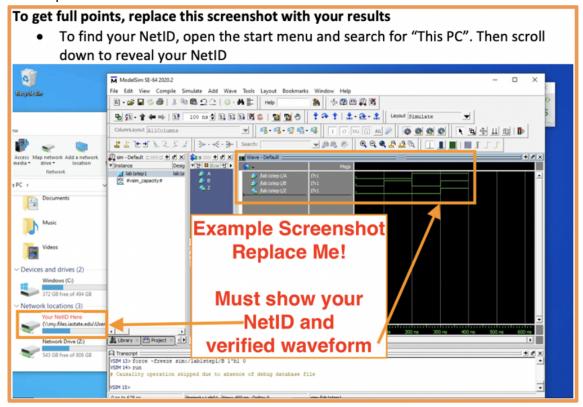
#### LAB:

#### 3.0 Lab5step0

Hardware demonstrates a good circuit.

<<<Insert a screenshot of your Verilog file>>>

#### Lab5step0 Result:



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#### 4.0 Lab5step1

Hardware demonstrates a good circuit.

<<<Insert a screenshot of your BDF file here>>>

#### Lab5step1 results:

