Name and Student ID:\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ Lab Section:\_\_

Date:\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

# Submission Instructions:

## Prelab:

1. Complete the prelab (questions Q1 and Q2)
2. Submit this report with the prelab completed to Canvas **before** your lab starts

## Lab:

1. Complete the lab according to the instructions
2. Take screenshots of your ModelSim waveform (note: to receive points your NetID has to be present in the screenshot) and insert them into this document.
3. Complete this report and reupload it to Canvas

**PRELAB:**

**Q1.** Read section 3.0 and fill in the truth table below for Design 1 (*the farmer’s problem*). Then use it to construct the POS expression.

|  |  |  |  |
| --- | --- | --- | --- |
| **Cabbage** | **Goat** | **Wolf** | **Alarm** |
| 0 | 0 | 0 |  |
| 0 | 0 | 1 |  |
| 0 | 1 | 0 |  |
| 0 | 1 | 1 |  |
| 1 | 0 | 0 |  |
| 1 | 0 | 1 |  |
| 1 | 1 | 0 |  |
| 1 | 1 | 1 |  |

POS Logic Expression: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

**Q2.** Read section 4.0 and fill in the truth table below for Design 2 (*adding the farmer*). Then use it to construct the SOP expressions.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Farmer** | **Cabbage** | **Goat** | **Wolf** | **Alarm** |
| 0 | 0 | 0 | 0 |  |
| 0 | 0 | 0 | 1 |  |
| 0 | 0 | 1 | 0 |  |
| 0 | 0 | 1 | 1 |  |
| 0 | 1 | 0 | 0 |  |
| 0 | 1 | 0 | 1 |  |
| 0 | 1 | 1 | 0 |  |
| 0 | 1 | 1 | 1 |  |
| 1 | 0 | 0 | 0 |  |
| 1 | 0 | 0 | 1 |  |
| 1 | 0 | 1 | 0 |  |
| 1 | 0 | 1 | 1 |  |
| 1 | 1 | 0 | 0 |  |
| 1 | 1 | 0 | 1 |  |
| 1 | 1 | 1 | 0 |  |
| 1 | 1 | 1 | 1 |  |

Canonical SOP Logic Expression: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

Simplified SOP Logic Expression: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

**LAB:**

**3.1** Schematic Capture with Quartus Block Design Files (lab3step0)

Schematic screenshot:

**<<<Insert a screen shot of your lab3step0 BDF file>>>**

Schematic results:



### 3.2 Structural Verilog (lab3step1)

Structural Code:

**<<<Copy and paste your Structural Verilog code here>>>**

Structural Results:



**3.3** Behavioral Verilog (lab3step2)

Behavioral Code:

**<<<Copy and paste your Behavioral Verilog code here>>>**

Behavioral Results:



**4.0** Design 2 (lab3step3)

Design 2 Code:

**<<<Copy and paste your Behavioral Verilog code here>>>**

Design 2 Results:

