ModelSim Guide

CPR E 281: Digital Logic

Introduction

ModelSim is a software for simulating hardware related tasks such as those normally performed on the Altera FPGA Board. Due to the coronavirus pandemic we are not allowed to use these boards this semester, because they cannot be easily disinfected after each use. Therefore, we will use ModelSim to simulate our circuit designs.

Starting ModelSim

VDI provides a virtual Windows 10 or Linux desktop with the same software as our physical computer labs. VDI works both on-campus and off-campus and can be used from almost any computing device (https://etg.ece.iastate.edu/vdi/).

How to Connect to VDI

If you are off campus you no longer need to connect to the VPN before using VDI (unless you want to; instructions for VPN are posted here: https://vpn.iastate.edu/).

1. Download the client for Windows or Mac: https://vlab.ece.iastate.edu/
2. Install the client with all the defaults.
3. Launch the VMware Horizon Client
4. Click the New Server icon on the Horizon Client Home window (the plus button on the top left), enter https://vlab.ece.iastate.edu for the name of the Connection Server, and click Connect.
5. Enter your IASTATE NetID in the form of netid@iastate.edu and password
6. Double click on the Windows Lab VDI icon.

You should now be able to access Quartus Prime remotely, as well as your U: drive. When you are finished using the VDI session, make sure anything that you want to keep saved on your U: drive. Otherwise, it will be deleted after you logout. You can exit the VDI session via several methods:

1. Start Menu > Log off
2. Start Menu > Shut Down
3. Quit the VMware View Client

All sessions are automatically destroyed after 2 hours of inactivity or logoff/shutdown.

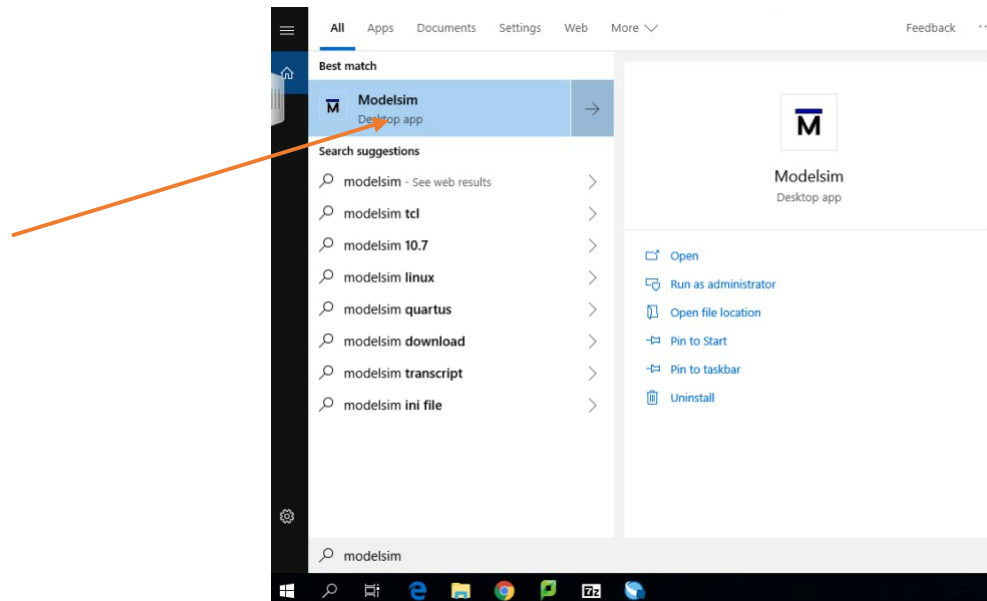To open ModelSim, simply search for ModelSim on the start menu as shown in Figure 1.

Figure 1: Starting ModelSIM from the start menu.

Creating a New Project

After starting ModelSim, click on **File** > **New** > **Project** and select a directory for the project as shown in Figure 2 and Figure 3. This directory will contain all files for the new project.
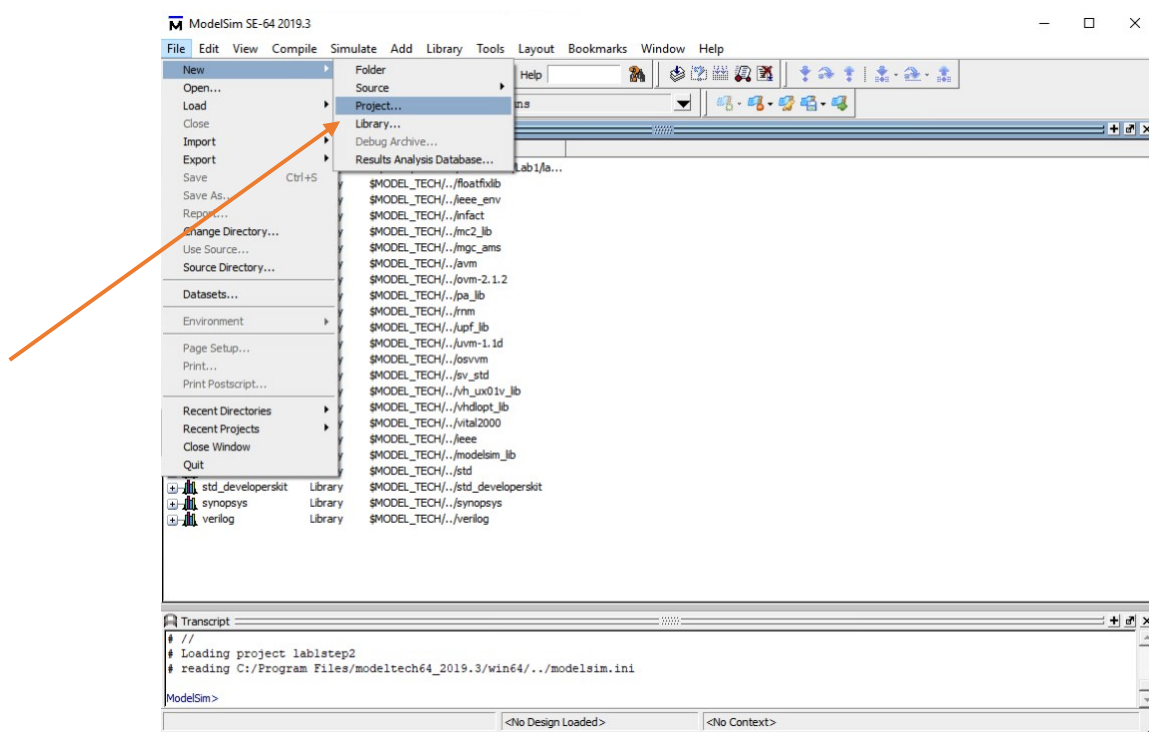

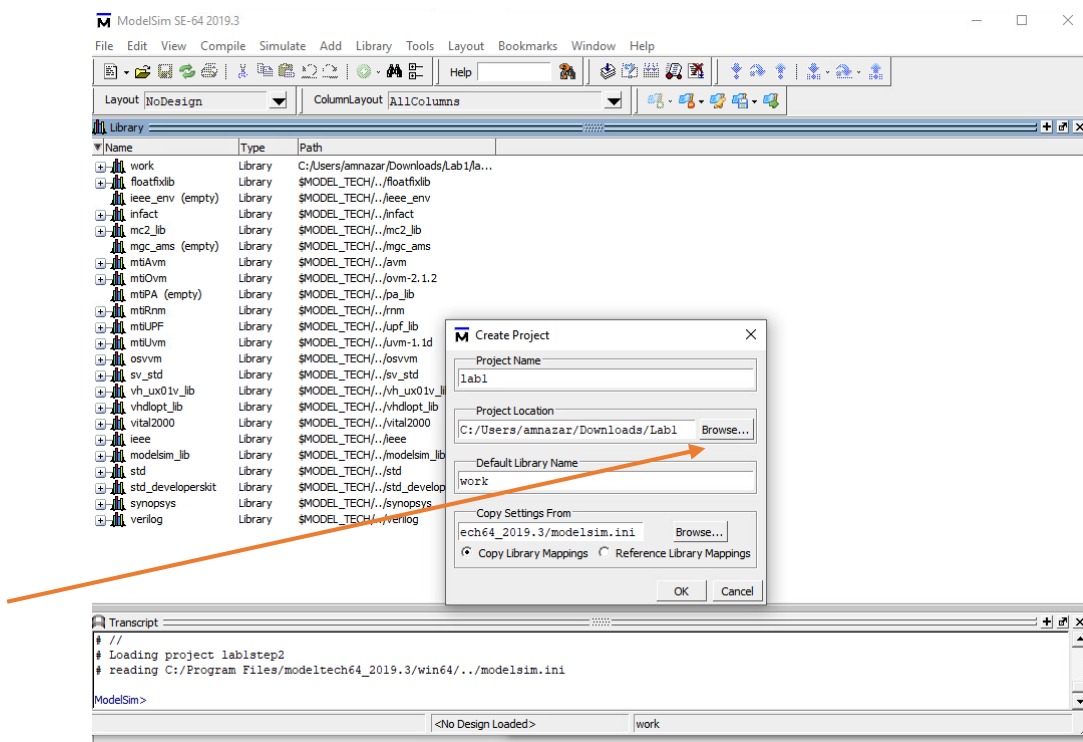Figure 2: Selecting a directory for a new project.

Figure 3: Selecting a directory for a new project.

After completing these steps, ModelSim creates necessary project and preset files to later ease the process of opening projects and view previous simulation logs.

Adding Files to ModelSim

The next step is to add files to the project. There are two options, either to create a new file within ModelSim's built-in text editor or add an existing file from the directory. The choice is made with the pop-up window shown in Figure 4, which should show up automatically after creating a new project. **The files that can be added here are .v files, i.e., Verliog HDL files.**
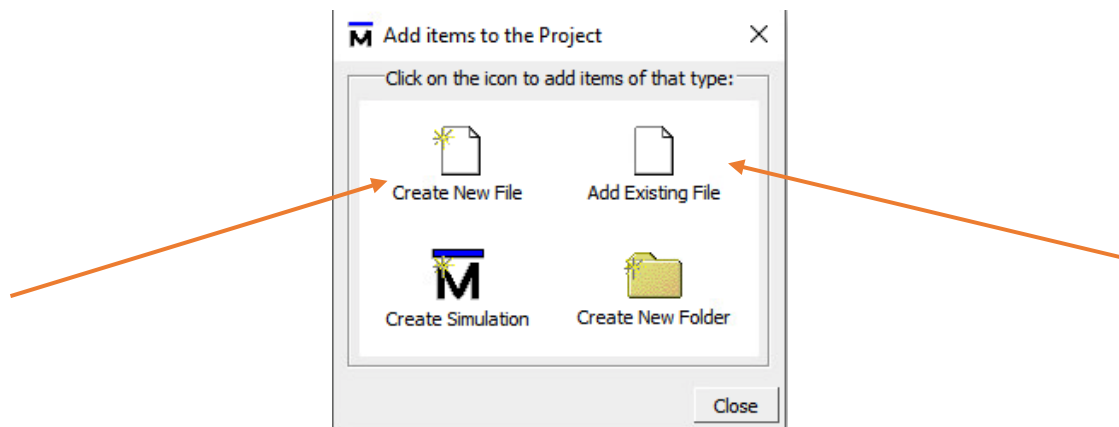

Figure 4: Pop-up window to select file additions.

What Are Verilog HDL (.v) Files?

ModelSim can simulate circuits described using a Hardware Description Language (HDL). In this class we will use a language called Verilog, or sometimes Verilog HDL. There are two ways to create a Verilog (.v) file:

1. Describe the functionality of the circuit directly in Verilog using a text editor.
2. Create a block diagram file (.bdf) for the circuit using a software package called Quartus. Then, convert the .bdf file to a .v file so that it can be simulated with ModelSim.

Using Quartus to Convert a Block Diagram File to a Verilog HDL File

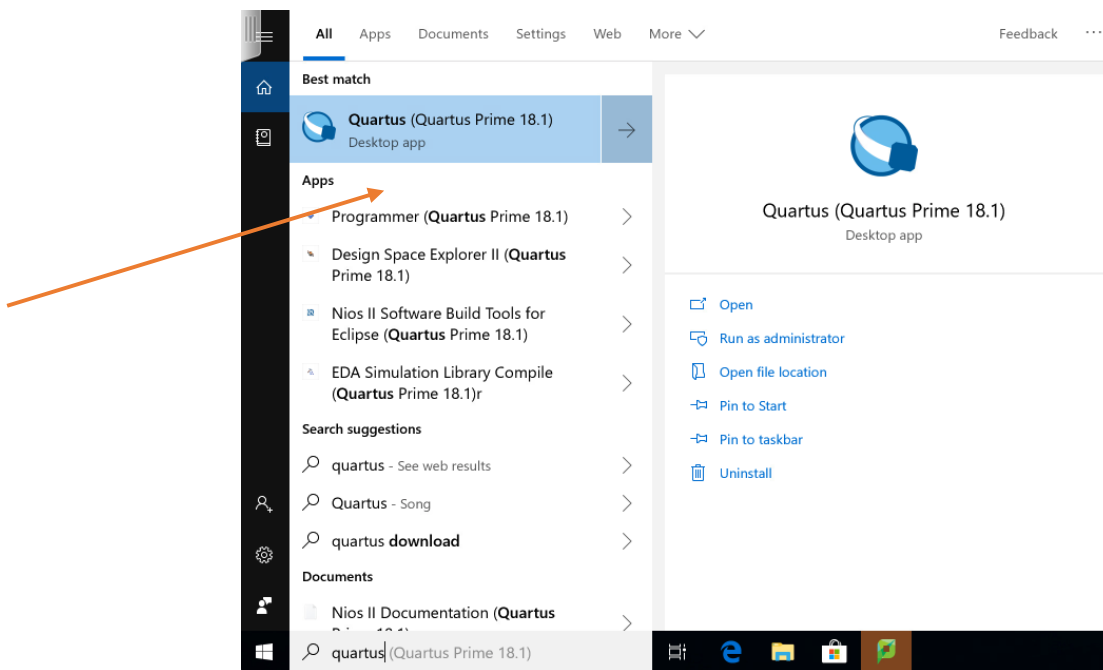Using the start menu, search for Quartus and start the application as shown in Figure 5.

Figure 5: Starting Quartus from the start menu.

Load the desired block diagram file (*.bdf) that you want to convert to a Verilog (*.v) file. Then, go to **File > Create/Update > Create HDL Design from Current File** as shown in Figure 6. A pop-up window will prompt you for the format of the output file. Make sure to select "Verolog HDL" as shown in Figure 7. Click OK and let Quartus do the remaining work. The resulting *.v file is now in the same directory and is ready to be opened by ModelSim.

Note: After converting the file it should be added to a project in ModelSim so that it can be simulated (see the previous page).
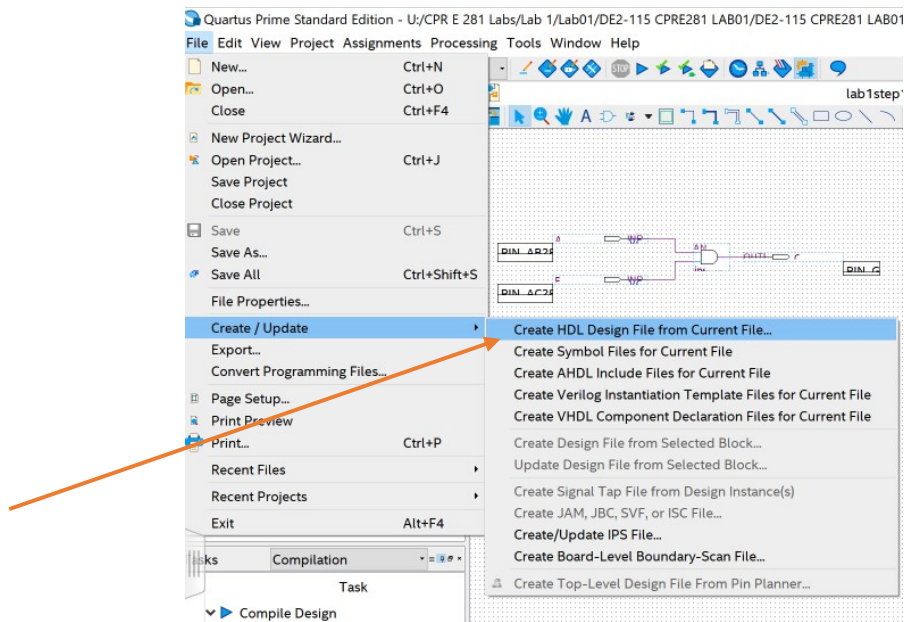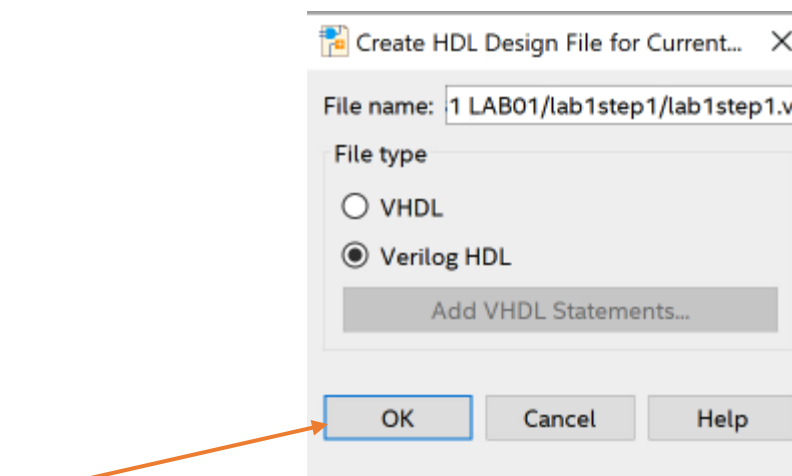
Figure 6: Converting a .bdf file to a .v file.

Figure 7: Prompt for choosing the destination of the converted .v file.

Compiling Files

To compile a file, right click on the file name within the project directory and then **Compile** > **Compile All** (see Figure 8). If the compilation is successful, a green tick mark will appear in the status column for this file.
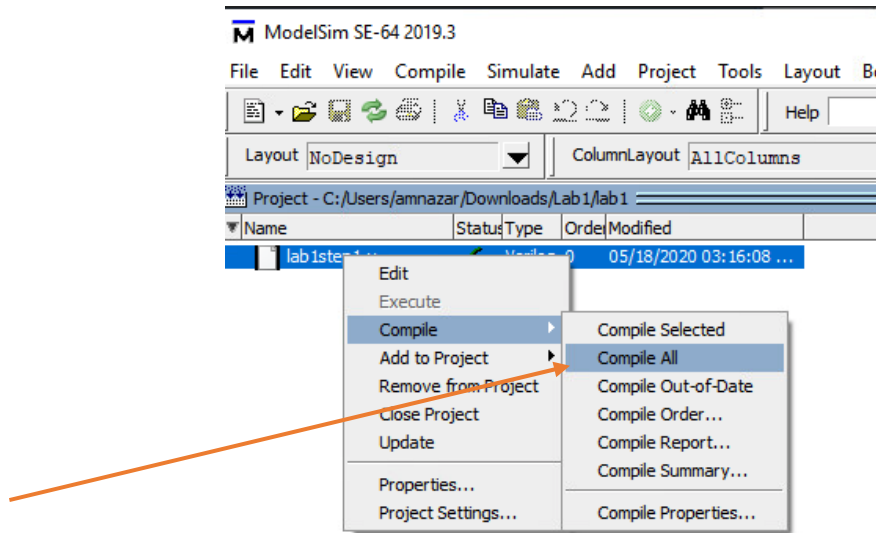

Figure 8: Compiling files in ModelSim.

Starting a Simulation

Before you proceed to this step, make sure that all files in your project are compiled successfully. This is necessary because there could be dependencies between the files.

To run the simulation click **Simulate** > **Start Simulation** as shown in Figure 9. A pop-up window will prompt you to select the file that you want to simulate. In the "Design" tab, look for an item called "work" and then click the "+" button that is immediately to its left (see Figure 10). This will show more files. Click on the file that you want to test and then click OK.
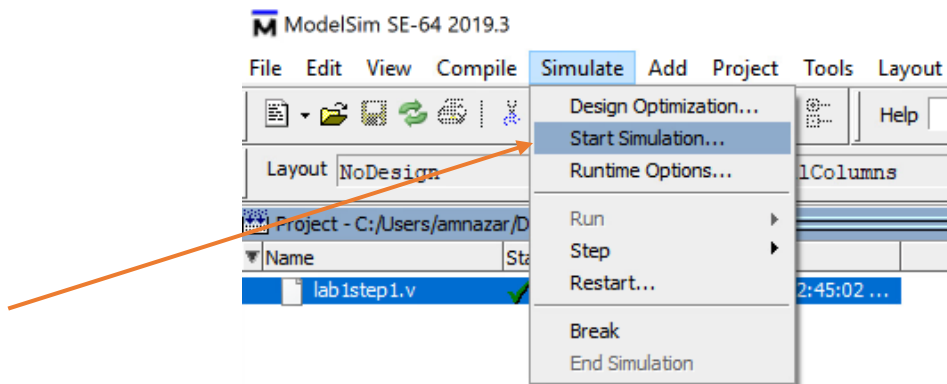

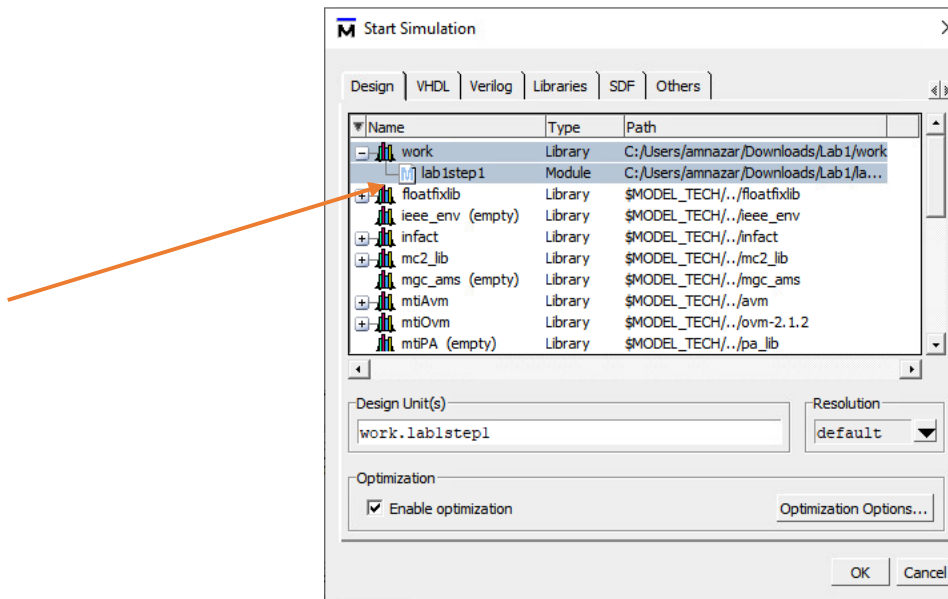Figure 9: Starting a simulation in ModelSim.

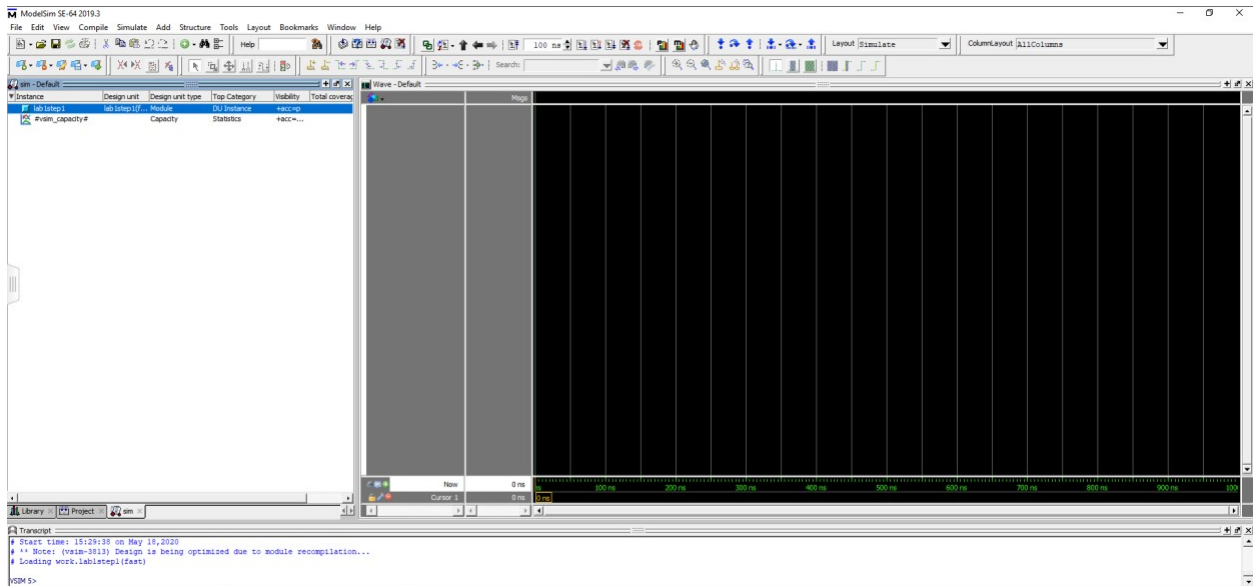Figure 10: Selecting the file to be simulated from the work directory.

Figure 11: Starting a simulation and invoking the wave form diagram.

A simulation window should pop-up as shown in Figure 11. Double click the file name to add all input/signal/output variables to be analyzed. Then click on a variable name that pops up on the right and press "CTRL-W" to add waveforms. No actual wave forms should show up since the variables have no initial value yet. This is shown in Figure 12.
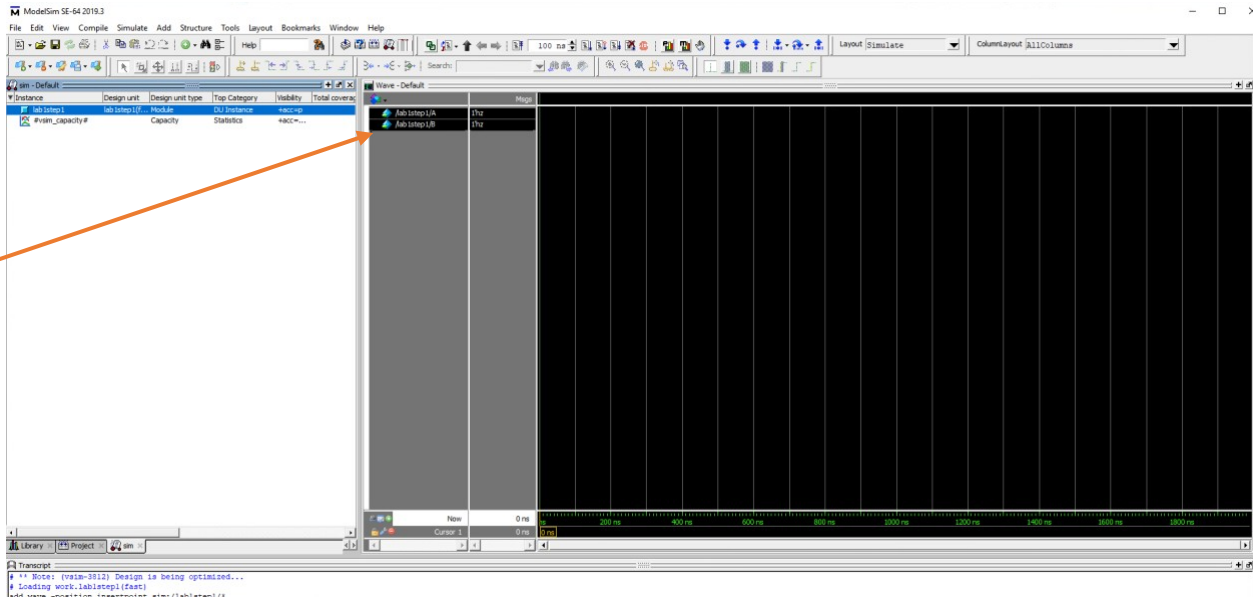
Figure 12: Adding variables and incorporating them into the wave form.

Edge-Case Testing

Now, it's time to finally test the circuit! For this example, we will hard code (or force) the values of the input variables for this circuit. This next step is important! Click on the desired **input variable and not on an output variable**. Then, right click and choose **Force** as shown in Figure 13. This allows you to force a value for that input indefinitely, or at least until it is forced to another value manually.
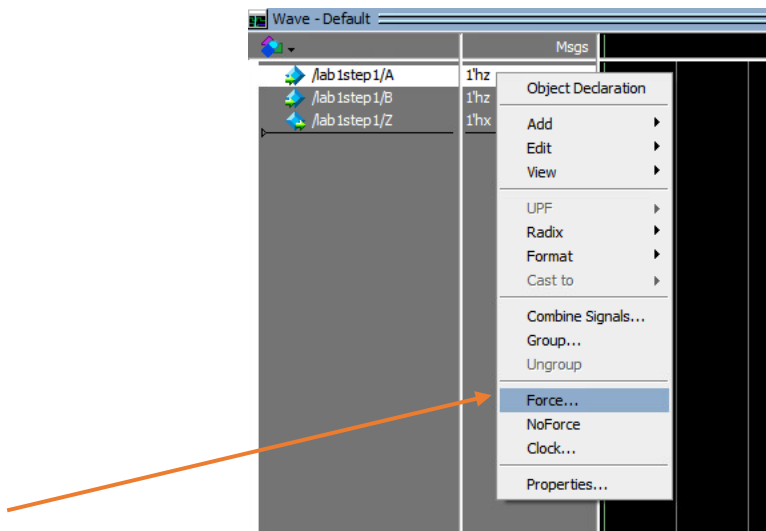

Figure 13: Forcing values for an input.

Another way to test is to create a testbench (if you're interested look up some YouTube tutorials on this subject), but that is out of the scope of this class.

After completing all of these steps, it is time to see some results. There is a command prompt at the bottom that allows for typing in commands in ModelSim syntax.

Using these commands, we can quickly tell ModelSim to complete tasks, instead of looking for them in the dropdown menus. Please ensure that all input variables have a forced value before doing this step. On the command prompt type "run 100", which lets the wave form simulate edge cases for 100 ns. The output variable now shows an expected output. In this case, the output of 0 AND 0 is 0! This is shown in Figure 14.
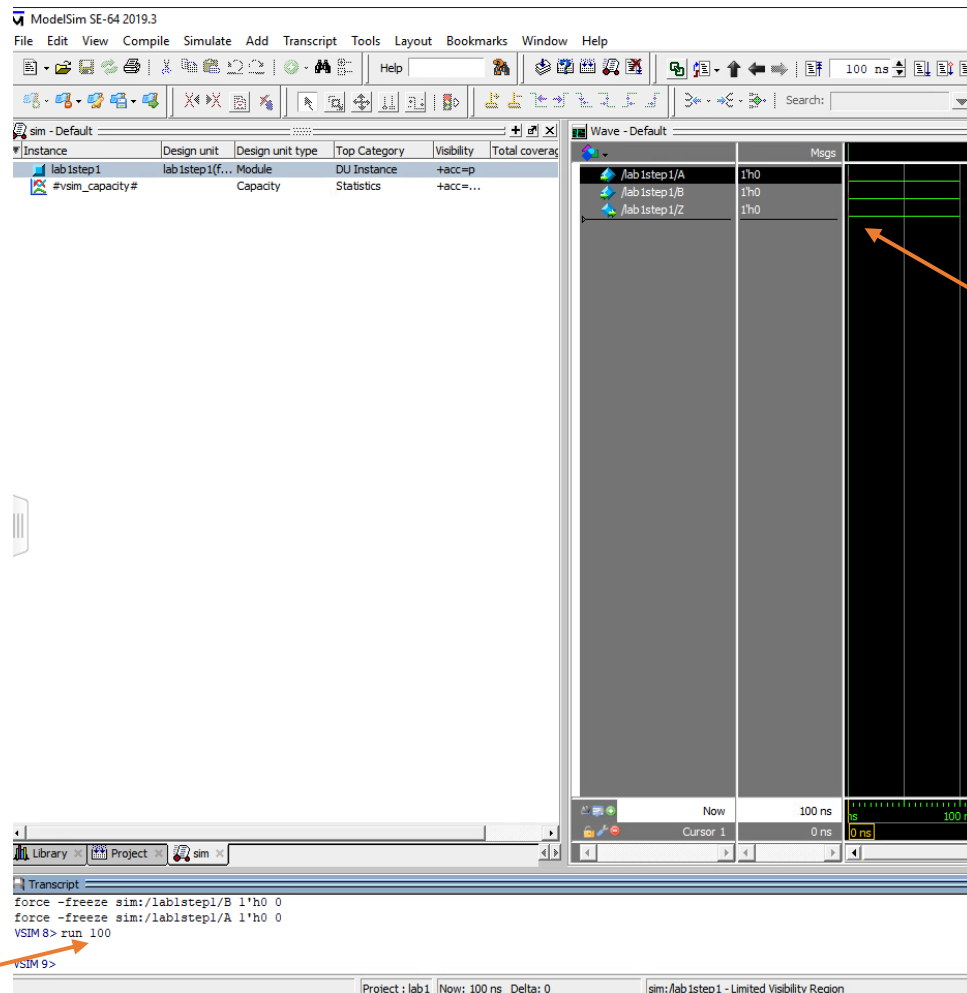

Figure 14: Wave form showing 0 AND 0 for which the output is 0.

Questions

If you have any questions or comments, please email your lab TA for further assistance.