Name and Student ID:\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ Lab Section:\_\_\_

Date:\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

# Submission Instructions:

## Prelab:

1. Complete the prelab (questions Q1 and Q2)
2. Submit this report with the prelab completed to Canvas **before** your lab starts

## Lab:

1. Complete the lab according to the instructions
2. Take screenshots of your ModelSim waveform (note: to receive points your NetID has to be present in the screenshot) and insert them into this document.
3. Complete this report and reupload it to Canvas

# PRELAB:

**Q1.** Read section 3.0 and fill in the truth table below for *lab2step1*. Then use it to construct the SOP expression and draw the resulting circuit using logic gates.

|  |  |  |  |
| --- | --- | --- | --- |
| **A** | **B** | **C** | **F** |
| 0 | 0 | 0 |  |
| 0 | 0 | 1 |  |
| 0 | 1 | 0 |  |
| 0 | 1 | 1 |  |
| 1 | 0 | 0 |  |
| 1 | 0 | 1 |  |
| 1 | 1 | 0 |  |
| 1 | 1 | 1 |  |

SOP Logic Expression: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

Circuit Diagram:

**Q2.** Read section 4.0 and fill in the truth table below for *lab2step2*. Then use it to construct the SOP expression and draw the resulting circuit using logic gates.

|  |  |  |  |
| --- | --- | --- | --- |
| **Cabbage** | **Goat** | **Wolf** | **Alarm** |
| 0 | 0 | 0 |  |
| 0 | 0 | 1 |  |
| 0 | 1 | 0 |  |
| 0 | 1 | 1 |  |
| 1 | 0 | 0 |  |
| 1 | 0 | 1 |  |
| 1 | 1 | 0 |  |
| 1 | 1 | 1 |  |

SOP Logic Expression: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

Circuit Diagram:

**LAB:**

**3.0** ModelSim results demonstrate a correct circuit.



**4.0** ModelSim results demonstrate a correct circuit.

