

PRELAB!

Read the entire lab and **complete** the prelab questions (Q1-Q3) on the answer sheet **before** coming to the laboratory.

1.0 Objectives

In this lab you will get familiar with the concept of using the computer as an experimental tool, to enforce the theory learned in class. You will also have an introduction to the CAD (computer aided design) tool we will be using in this course: **Altera Quartus Prime**. And, you will learn to use truth tables, logic expressions, and circuit design. We will apply the knowledge using modelsim to observe how these concepts relate to each other.

2.0 Setup

The laboratory is equipped to provide software needed to perform the labs. A TA should also be present and is a good resource for questions. The time you spend in lab will be more productive, and you will have a better lab experience if you read, and complete, as much of the lab as possible before you start. You should also have a lab answer sheet. Record your answers to the questions on the answer sheet and then hand it in when the lab is completed (don't forget to write your names).

To begin, create a file folder for CPRE 281 inside your network drive directory (**U:\ Drive**). Each lab will eventually have its own subfolder inside **U:\CPRE281**.

Download zipped lab files from the course webpage on canvas website and **extract the files** into **U:\CPRE281**. Now you should have path **U:\CPRE281\Lab01** for Lab #1 files in your network drive directory. Ask your TA if you need assistance.

You are ready to run **Quartus Prime** software. Click on the Windows Start Button go through **Intel FPGA 18.1.0.625** then click on **Quartus (Quartus Prime 18.1)** to run the software. This is the software we will be using for the rest of the semester.

Open a file in Quartus Prime

- Left-Click on the *Open File* icon from the icon bar (second icon from your left), or select **File>Open Project** from the dropdown menu.
- Click on the downward arrow in the **Address bar** box. Make sure the directory looks like **U:\CPRE281\Lab01\...\lab1step1**; navigate to the file from the U:\ via "This PC" if it does not. It is important that the address begins with U:\ and not "\\my.files.iastate.edu\"; Quartus 16.0 will not compile from filepaths that begin with the latter.
- Select **lab1step1.qpf** (ensure the file extension is **.qpf**, otherwise you will not be able to compile) and click **Open**.

- Click Yes on the Dialog box to upgrade project if it opens up.

A simple AND circuit

- The circuit has already been started for you, and it should have two inputs labeled A and B, and is missing an output. Double-click on the **lab1step1** icon in the **Project Navigator** window to view the **Block Design File (lab1step1.bdf)**.
- In order to create the output pin double click on the blank area to the right of the circuit. This will bring up the **Symbol** dialog. In the **Name** field type “**output**” and then press **OK**. Left-click to place the output pin on the diagram.
- The pin can be renamed by double-clicking on the pin (you may also right click on it select **Properties**). Rename the output pin to C.
- Connect pin C to the output of the AND gate by dragging it over so that the pin touches the output of the AND gate and releasing it. Then you can grab it again and move it away from the AND gate and a wire should appear connecting the two.

Compile the circuit

- Select **Processing>Start Compilation** (save your changes if prompted).
- A warning dialogue box may pop up when the compilation is finished. Ignore the warnings for now and click the *OK* button. If you have any other errors fix them now.

3.0 Simulation Testing – Modelsim

A lab1step1.v file, which is written in Verilog, is provided in the lab01 zip folder (Verilog will be introduced later on in the class). Follow the steps provided in the “...” file in order to run a simulation on Modelsim for testing your design.

4.0 Multi-level Circuits

We will now look at a more complex circuit. Open the (*.qpf) files and follow the instructions. Read the previously outlined steps for opening a file if you are not sure how.

Circuit 1

- **Open** the *lab1step2.qpf* file. Even though this circuit is larger, its behavior can still be shown on a Truth Table. The circuit has multiple logic gates, a single output, and three inputs.

- Compile the design and then program the FPGA with the new circuit. Record the circuit's behavior on your answer sheet.

You can discuss the results with your TA. When you are done, have the TA mark his/her initials next to your answers.

Circuit 2

- **Open** the *lab1step3.qpf* in Quartus Prime. Notice that the Truth Table on the answer sheet for this circuit is blank.
- You need to fill in all possible input and output combinations in the Truth Table.
- Use Modelsim and force-change the inputs, 0 or 1, on the gates to determine how the input combinations affect the output.
- Record each input combination and resulting output.

You can discuss the results with your TA. When you are done, have the TA mark his/her initials next to your answers.

5.0 Complete

You are done with this lab. Ensure that all lab files are closed. Exit Quartus Prime, Modelsim, log off the computer if working remotely, and hand in your answer sheet. **Don't forget to write down your name, student ID and your lab section number.**