Cpr E 281 HW12

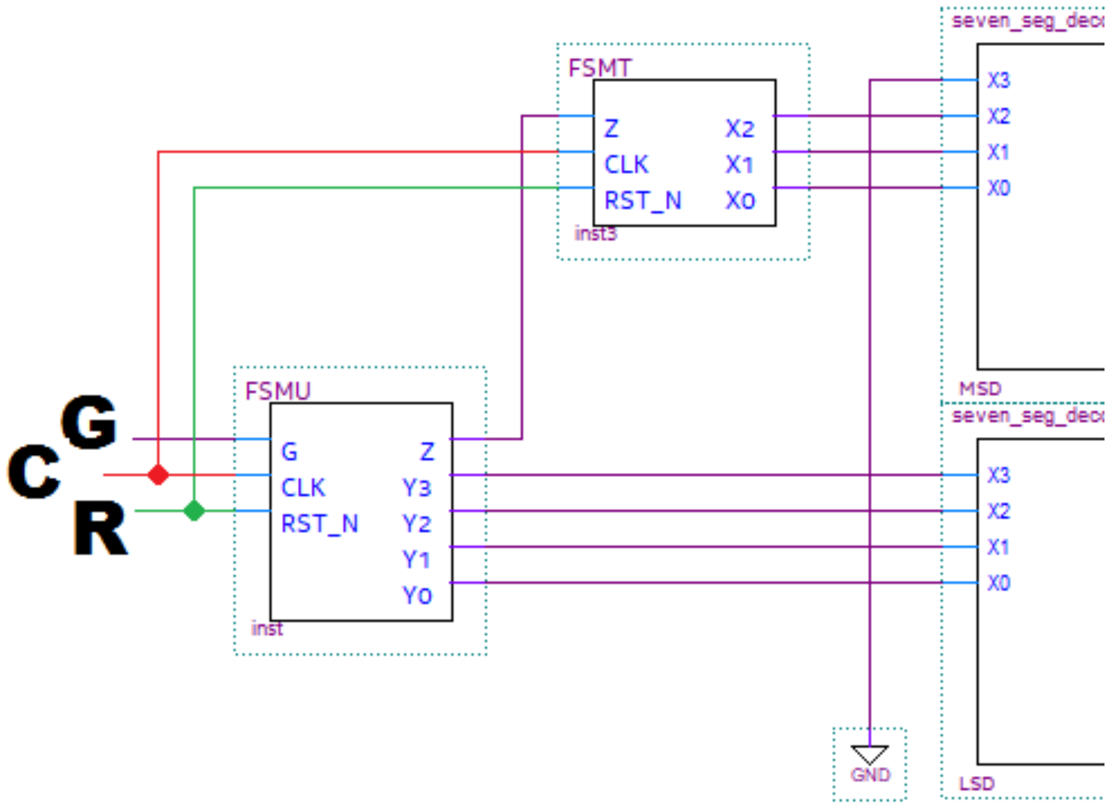
ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

FSMs, ASMs, and Register Machines

Assigned: Week 13

Due Date: Nov. 16, 2020

P1 (20 points): For this problem, you are given two FSMs: FSM T has six states, one-bit input Z, and three-bit output X_2 X_1 X_0. FSM U has ten states, one-bit input G, and five-bit output Z Y_3 Y_2 Y_1 Y_0. These FSMs are connected as shown below:



Each FSM shown here has states determined by a sufficient number of positive-edge-triggered DFFs.

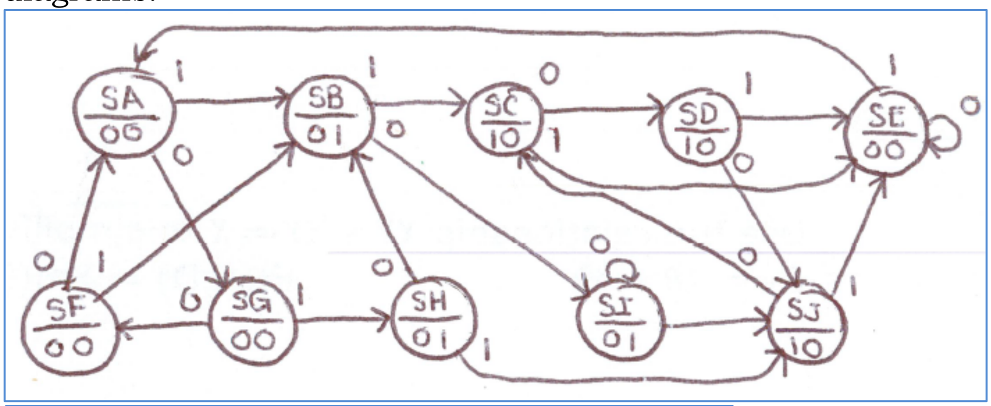
a) Draw the state table for FSM U, a modulo-10 counter that counts *down* when G=1 and holds its value constant when G=0. Upon reset, FSM U should return to a state which outputs Y=9. The output Z=1 if Y=0 and G=1. Make state assignments such that the output Y is equal to the current state (note: the state variable and the output should not have the same name).

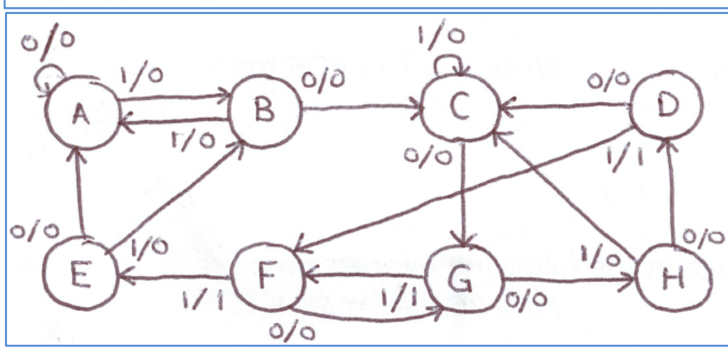
b) FSM U has one input and four state variables, so each expression for the next state is a function of five inputs. To avoid using a 5-variable K-map, we will instead implement FSM U using four 2-to-1 MUXes with G as the select line. Let us assume that G=1. Derive the next state expressions assuming that G=1. Show that the K-maps for the next state variables produce these expressions.

$$For\ G=1\!:\ S_3^{new} = \bar{S}_3\bar{S}_2\bar{S}_1\bar{S}_0 + S_3S_0, S_2^{new} = S_3\bar{S}_0 + S_2S_1 + S_2S_0$$
$$S_1^{new} = S_2\bar{S}_1\bar{S}_0 + S_3\bar{S}_0 + S_1S_0, S_0^{new} = \bar{S}_0$$

c) FSM T is a modulo-6 counter that also counts down when Z=1 and resets to a state which outputs X=5. Draw the state table for FSM T.
d) If both FSMs are treated as a single FSM as shown in the initial diagram, what type of circuit does it create? Please specify the direction, encoding, and modulus.

P2 (15 points): Perform state minimization on the following state diagrams.

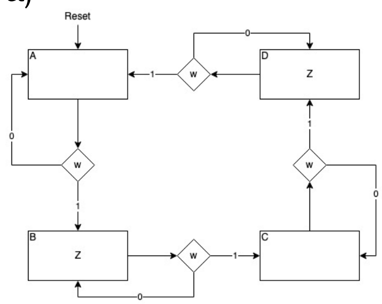




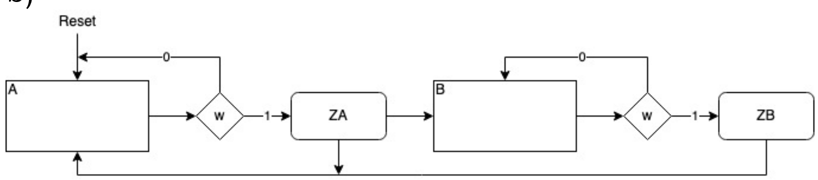
P3 (10 points): Consider a state machine that detects if a number (F) is a multiple of three (3, 6, 9, 12…). Draw the specified ASM chart that will output Z=1 based on the input W. Let F be the number of clock cycles for which the input W has been one. Draw a Moore type ASM chart that outputs Z=1 if F is a multiple of 3.

P4 (10 points): For each of the following, convert each ASM chart to a FSM diagram.

a)



b)



P5 (10 points): Answer the following questions about register machines.

a) How many possible operations can be performed in a register machine? List and explain each operation.
b) How does a register machine perform an if statement? Explain your answer.

P6 (15 points): Consider the following register machine:

Step	Instruction	Register	Go to step	[Branch to step]
1	Deb	1	2	7
2	Deb	2	3	5
3	Inc	0	4	
4	Inc	3	2	
5	Deb	3	6	1
6	Inc	2	5	
7	End			

Syntax note: register 0 is shortened to R0, register 1 is R1, and so on.

a) Let R0 = 0, R1 = 3, R2 = 2, and R3 = 0.
What will be the values stored in R0, R1, R2, and R3 after the machine finishes running?
b) Let R0 = 0, R1 = 0, R2 = 100, and R3 = 0.
What will be the values stored in R0, R1, R2, and R3 after the machine finishes running?

c) Let R0 = 0, R1 = **x**, R2 = **y**, and R3 = 0 where **x** and **y** are two random integers.
Write the value of R0, R1, R2, and R3 in terms of **x**, **y**, and necessary constant numbers. (e.g. R0 = **x**+**y**, R1 = 3, and so on).

P7 (15 points): Consider a register machine with three registers (R0, R1, and R2). Let R0 = **?**, R1 = **x**, and R2 = **y**. The value stored in R0 is unknown, and the values **x** and **y** are two random integers. Write out the instructions for the register machine that will add **x** and **y** and store the sum in R0 (e.g. R0 = **x** + **y**, R1 = 0, R2 = 0).

P8 (5 points): Refer to the lecture slides for ***the i281 CPU*** to answer the following questions about the i281 CPU:

a) How many control signals (number of wires) does the i281 CPU have?
b) What control signal(s) select the ALU operation?
c) What is the name of control signal C17 and what block does it control?
d) How many bits does each instruction have (e.g. how wide is each register in the instruction memory)?
e) How many bits of each instruction go to the OpCode Decoder? Which part of each instruction?