Cpr E 281 HW10
ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

Synchronous Sequential Circuits
Assigned: Week 11
Due Date: Nov. 2, 2020

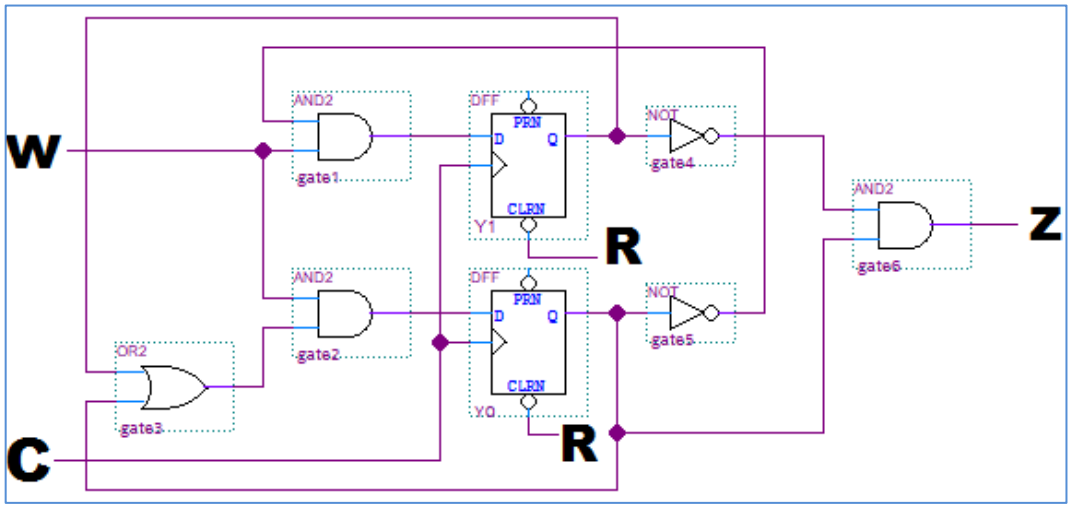
P1 (10 points):
Briefly explain the major difference between a Moore state machine and a Mealy state machine.

P2 (15 points): Design a Moore FSM that has one-bit input A and one-bit output B, where B=1 if the last six bits of A are 100111 (from earliest to latest). Draw the state diagram for this FSM.

P3 (15 points): Design a Mealy FSM that has one-bit input A and one-bit output B, where B=1 if the last six bits of A are 111001 (from earliest to latest). Draw the state diagram for this FSM.

P4 (15 points): Create a Moore FSM for a circuit that outputs z=1 if input w=1 for the last three clock cycles. The states should be as follows: SA=00, SB=10, SC=11, and SD=01. These states encountered in order from reset to completion of the three clock cycles.

a) Draw a state diagram for this FSM.
b) Create a state-assigned table for this FSM.
c) Use K-maps to show that the following circuit implements this FSM. Note the expressions should be in POS form, in accordance with the circuit below.



P5 (10 points): Design a Mealy FSM with the following specifications:

- There is a one-bit input X
- There is a one-bit output Z
- On each cycle, a three-bit value stored in the FSM (V) is shifted left and X replaces the least significant bit of V
  - e.g. if X=0 and V=101_2 then $V^{new}=010_2$
- The output Z=1 if V is greater than 4.

Draw the state table for this Mealy FSM.

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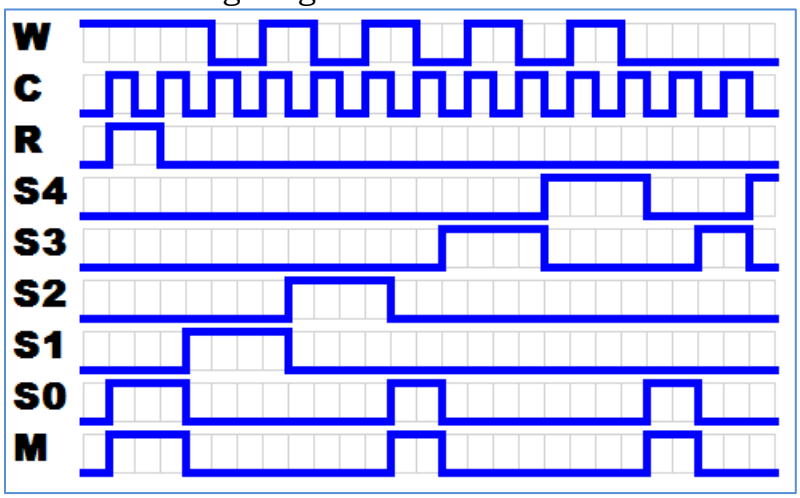
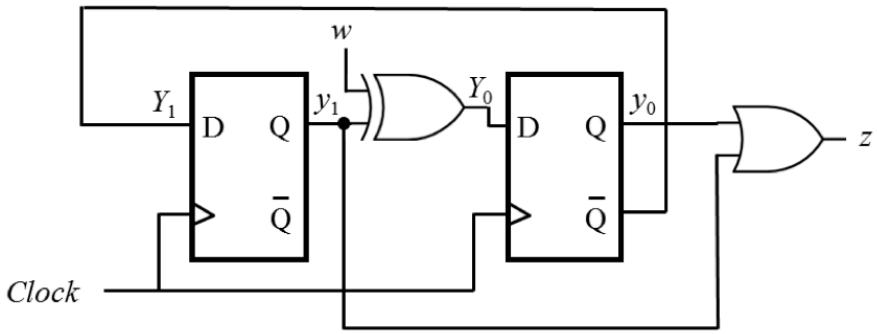
P6 (20 points): A FSM has five states, five state variables, one-bit input W, one-bit reset R, and one-bit output M. The FSM has an output that corresponds with the timing diagram shown below. Answer the following questions.



a) The five states encountered in this timing diagram, in order, are A, B, C, D, and then E. What are the state encodings for these states?
b) Draw a state diagram for this FSM.
c) Draw a state-assigned table for this FSM.
d) This circuit is implemented using five DFFs. Derive expressions for the next state variables and the output M.
e) Explain why this particular circuit has the same number of states as it does state variables and why this isn't necessarily true of other circuits?

P7 (15 points):
A FSM has two D flip-flops, an input w, and an output z. The circuit diagram is shown below.



a) (5 points) Find the logic expressions of Y_1, Y_0, and the output z.
b) (5 points) Show the state-assigned table of the FSM.
c) (5 points) Draw the state diagram of the FSM.