Cpr E 281 HW03
ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

NAND/NOR Gates with Synthesis
Assigned: Week 3
Due Date: Sep. 7, 2020

P1 (5 x 2pts = 10 points): Answer the following true/false questions.

a. In Verilog, the symbol for OR is the plus sign ("+") True/False

b. $x + y = \overline{x \cdot y}$ True/False

c. In Verilog, the symbol for XOR is the caret ("^") True/False

d. A NAND gate can implement a NOT gate True/False

e. $\overline{(x \cdot y) + (\bar{x} \cdot \bar{y})} = (\bar{x} + \bar{y}) \cdot (x + y)$ True/False

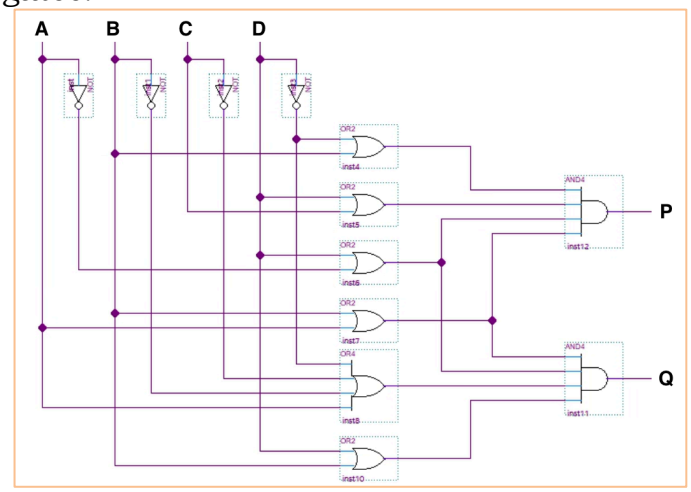
P2 (15 points): Given the expression $F(a,b,c,d) = \prod M(0,2,4,9,11,12)$, perform the following:

a. Write the expression for F as a shorthand SOP expression.
b. Write the expression for F as a simplified POS expression.
c. Show how the expression for F can be implemented as a digital circuit using exactly three NOT gates, three OR gates, and one AND gate.

P3 (15 points): Show how to implement the following:

a. Implement a 4-input AND gate using three 2-input AND gates.
b. Implement a 4-input NAND gate using five 2-input NAND gates.
c. Implement a 2-input AND gate using any number of OR and NOT gates. Hint: remember how DeMorgan's Theorem can be used to change between AND and OR operations.

P4 (15 points): Convert the following circuit into a circuit that only uses NOR gates and NOT gates. Your circuit should use no more than 8 NOR gates.



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P5 (15 points = 3p+3p+3p+4p): A **Full Adder** is a circuit that adds three bits (X, Y, and Z) together and returns two bits (C and S) to represent the total as a 2-bit binary number, where the carry bit C is the most significant bit (MSB) and the sum bit S is the least significant bit (LSB). For example, let X=1, Y=0, and Z=1. Here, the total should be $2_{10} = 10_2$, and the outputs are C=1 and S=0.

a. Derive the truth tables for C and S. (3p)
b. Write the Boolean functions for C and S in shorthand notation using minterms. (3p)
c. Repeat part b) but use maxterms instead. (3p)
d. Obtain the simplest SOP expressions for the functions C and S and draw a circuit that implements the **Full Adder**. (4p)

P6 (16 points): Given the expression $G(A,B,C) = \sum m(2,5,6,7)$, perform the following:

a. Write the expression for G as a simplified SOP expression.
b. Write the expression for G as a simplified POS expression.
c. Implement G using exactly four NOR gates and no other gates.
d. Did you use the SOP expression or the POS expression to implement the circuit? Why?

P7 (14 points): Consider the expression $H(W,X,Y,Z) = \sum m(0,2,8,10,11)$

a. Write H as a simplified SOP expression
b. Implement H using Verilog

```
module p7 (W,X,Y,Z,H);
     input W,X,Y,Z;
     output H;

     //write your code here









endmodule
```