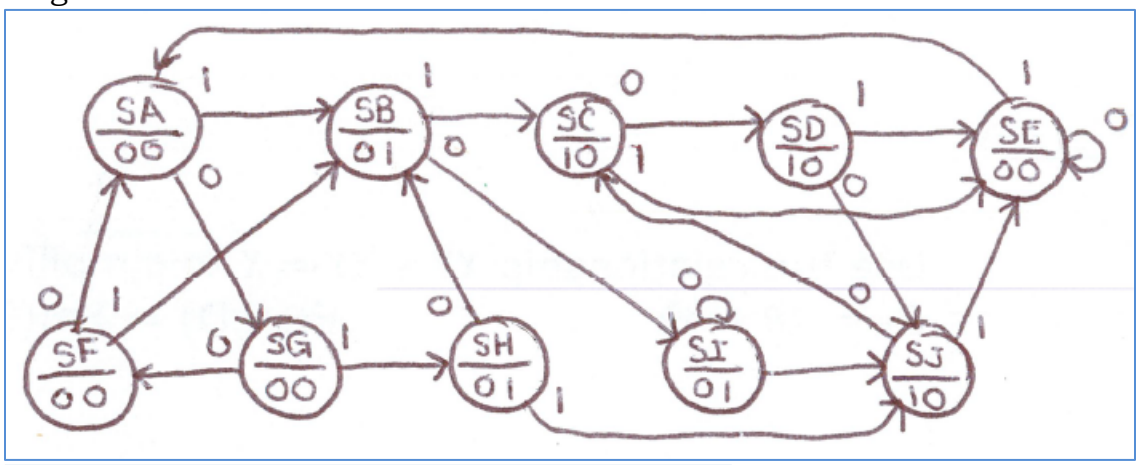
Cpr E 281 HW12

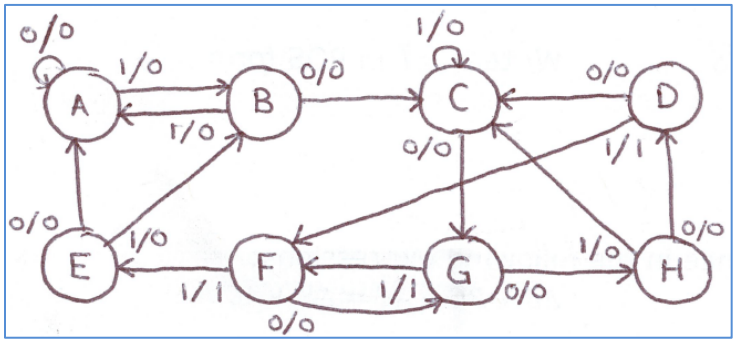
ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

Synchronous Sequential Circuits
Assigned: Week 13
Due Date: Dec. 2, 2019

P1 (15 points): The following all concern state machines that detect if a number is a multiple of three (3, 6, 9, 12…). Draw the specified state diagrams that will output Z=1 based on the input W.
A: Let F be the number of clock cycles for which the input W has been one. Draw a state diagram for a Moore FSM that outputs Z=1 if F is a multiple of 3.
B: Let G be the three-bit binary representation of the last three values of W, with the most significant bit as the earliest observed value of W. Assume that G is initially zero. Draw a state diagram for a Mealy FSM that outputs Z=1 if G is a multiple of 3.
C: For every clock cycle, let the new value of H be twice its previous value plus the value of W ($H^* = 2H_0 + W$). This means that H is the binary representation of all values observed on W (a bit string of unlimited length). Assume that H is initially zero. Draw a state diagram for a Moore FSM that outputs Z=1 if H is a multiple of 3.

P2 (15 points): Perform state minimization on the following state diagrams.





P3 (10 points): The circuit below looks like a counter. Draw a state diagram which illustrates its counting sequence.

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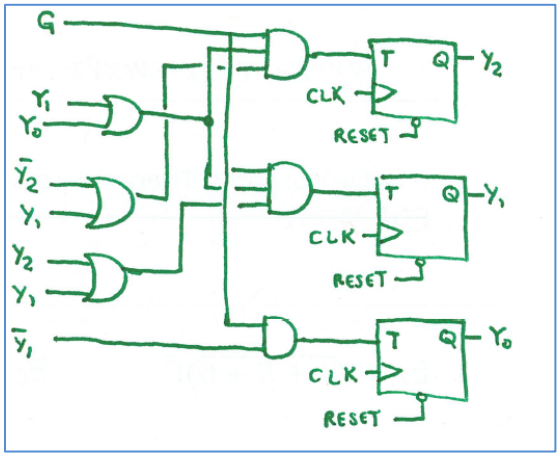
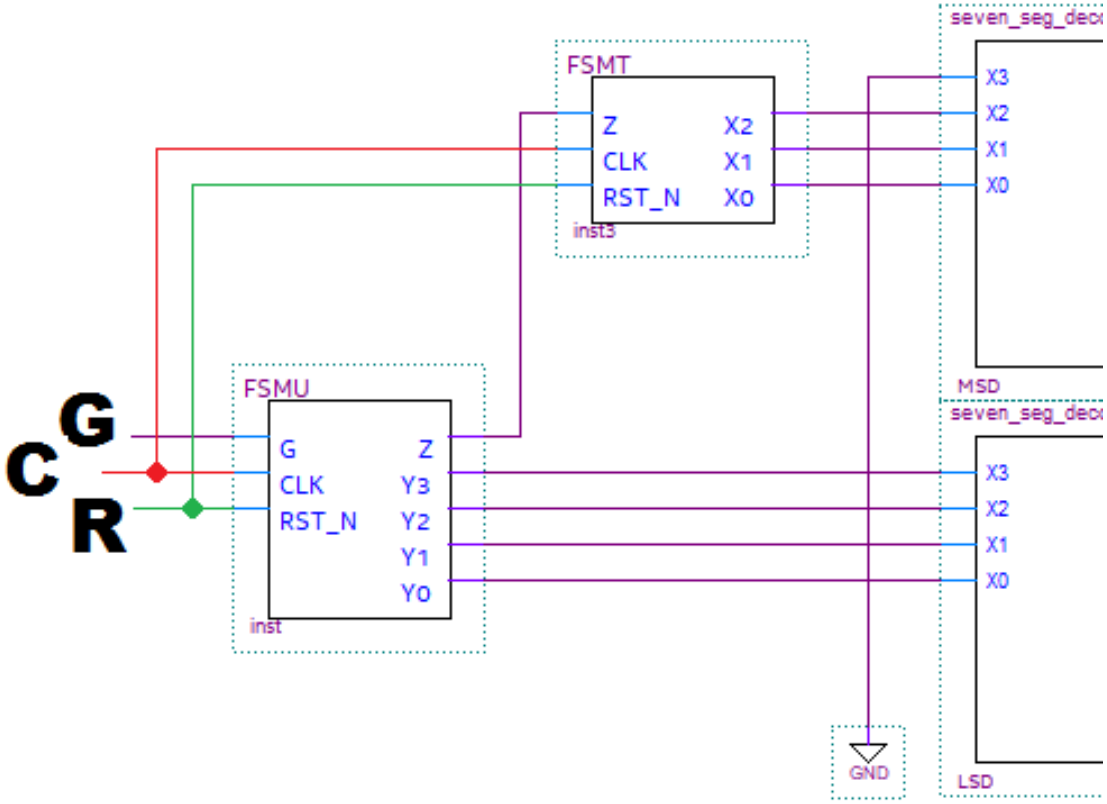


P4 (20 points): For this problem, you are given two FSMs: FSM T has six states, one bit input Z, and three bit output X_2 X_1 X_0. FSM U has ten states, one bit input G, and five bit output Z Y_3 Y_2 Y_1 Y_0. These FSMs are connected as shown below:



Each FSM shown here has states determined by a sufficient number of positive-edge-triggered DFFs.

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A: Draw the state table for FSM U, a modulo-10 counter that counts *down* when G=1 and holds its value constant when G=0. Upon reset, FSM U should return to a state which outputs Y=9. The output Z=1 if Y=0 and G=1. Make state assignments such that the output Y is equal to the current state (note: the state variable and the output should not have the same name).
B: FSM U has one input and four state variables, so each expression for the next state is a function of five inputs. To avoid using a 5-variable K-map, we will instead implement FSM U using four 2-to-1 MUXes with G as the select line. Let us assume that G=1. Derive the next state expressions assuming that G=1. Show that the K-maps for the next state variables produce these expressions.

$$For\ G = 1:\ S_3^{new} = \bar{S}_3\bar{S}_2\bar{S}_1\bar{S}_0 + S_3S_0, S_2^{new} = S_3\bar{S}_0 + S_2S_1 + S_2S_0$$
$$S_1^{new} = S_2\bar{S}_1\bar{S}_0 + S_3\bar{S}_0 + S_1S_0, S_0^{new} = \bar{S}_0$$

C: FSM T is a modulo-6 counter that also counts down when Z=1 and resets to a state which outputs X=5. Draw the state table for FSM T.
D: If both FSMs are treated as a single FSM as shown in the initial diagram, what type of circuit does it create? Please specify the direction, encoding, and modulus.

P5 (20 points): The following Moore FSM state table is incomplete. The clock for this FSM (FSM 1) has a period of 100 microseconds such that the button for the input X, controlled by the user, cannot be pressed for only one clock cycle. In addition, button X, when pressed, will output X=0.

Current State	Next State		Output
	X=0	X=1	W
A (reset)	B	A	0
B	B	C	0
C	D	C	0
D	E	--	1
E	F	--	1
F	G	--	1
G	G	A	0

I: Draw a state diagram for this state table.
II: How many full button press cycles (push and release) will cause this FSM to pass through all seven states and return to state A?
III: Use the following state assignments: A=000, B=001, C=010, D=100, E=101, F=110, G=111. Use a K-map to show that the next state expressions for FSM 1 are:
$Y_2^{new} = (\bar{X})(Y_2 + Y_1), Y_1^{new} = (Y_1 + Y_0)(X + Y_2)(\bar{X} + \bar{Y_2}), Y_0^{new} = (\bar{X})(\bar{Y_2} + Y_1 + \bar{Y_0})(Y_2 + \bar{Y_1})$
Assume that DFFs are used to hold the state values.

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P6 (20 points): Design a FSM with no inputs (other than CLK and RESETN) and four-bit output Z such that the FSM outputs the sequence 2, 3, 4, 5, 9, 13. The state assignments should be equal to the output and your circuit should use four positive-edge-triggered JKFFs and a minimal number of other gates.

A: Draw a state diagram. Don't forget the reset signal.

B: Draw the state-assigned table. This table should also include the excitation for the JKFFs (the values for J and K along with the next state values).

C: Draw K-maps to show that the inputs to the JK FF are as follows:

$$J_3 = s_2 s_0, K_3 = s_2, J_2 = s_0, K_2 = s_0, J_1 = s_3 s_2, K_1 = s_0, J_0 = 1, K_0 = s_3 s_2 + s_1$$

D: How might JKFF 2 be simplified given that both of its inputs are the same?