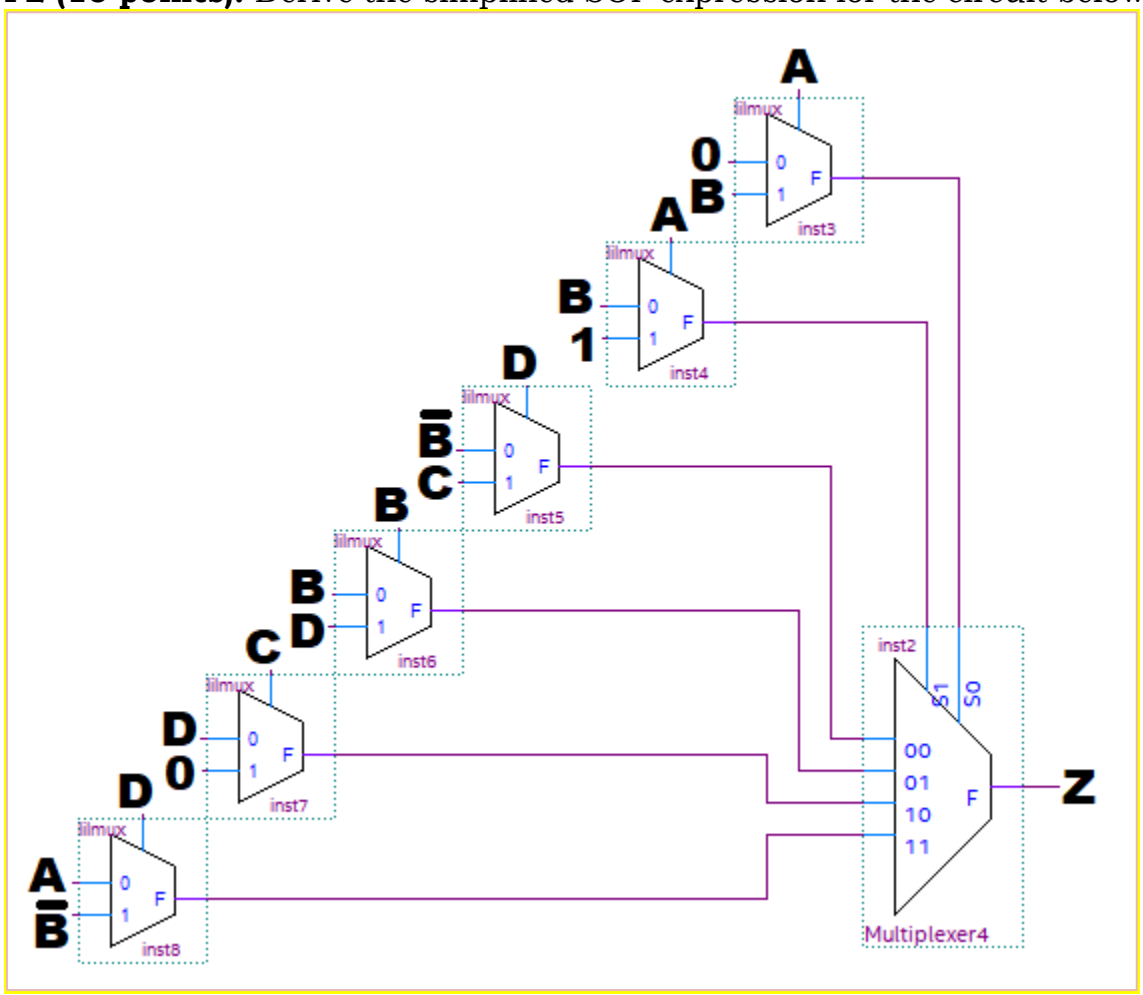
Cpr E 281 HW07
ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

Representation and Arithmetic
Assigned: Week 8
Due Date: Oct. 21, 2019

P1 (8 points): Perform the following number representation conversions and indicate the value of the number in decimal:
A: Convert 100101 from 1's complement to Sign-and-Magnitude
B: Convert 100101 from Sign-and-Magnitude to 2's complement
C: Convert 100101 from 2's complement to 1's complement
D: Convert 011101 from 1's complement to Sign-and-Magnitude

P2 (10 points): Derive the simplified SOP expression for the circuit below.



P3 (20 points): Design the circuits below.
A: Using only three full adders (and other gates as necessary), design a circuit that takes two 3-bit unsigned integers A and B and produces a one-bit output Y=1 if A>B. Hint: C_{out} will have to be used at some point.
B: Using the circuit you designed in part A (along with some 2-to-1 MUXes), design a circuit that takes two 3-bit unsigned integers A and B and produces a 3-bit output L such that L = max(A, B); that is, the output

integer is the larger of the two input integers.

P4 (20 points): Given $P(A,B,C,D) = BCD + A\bar{B}C + \overline{(A+C+D)(B+D)}$
A: Implement this function using one 16-to-1 MUX.
B: Implement this function using one 8-to-1 MUX and NOT gates.
C: Implement this function using one 4-to-1 MUX with A and B as the select lines and a minimal number of AND/OR/NOT gates.
D: Implement this function using one 2-to-1 MUX with C as the select line and some AND/OR/NOT gates. Do not implement P separately with gates and place the MUX in a trivial connection with the rest of the circuit.
E: Implement this function using one 4-to-1 MUX with B and C as the select lines.

P5 (15 points): Using the specified decoder(s), implement the following:
A: One NOT gate using only one 1-2 decoder.
B: One **3**-input AND gate using only two 1-2 decoders.
C: One 2-input OR gate using only four 1-2 decoders.
D: One 2-input NOR gate using only one 2-4 decoder.

P6 (12 points): Answer the following questions about MUXes and decoders.
A: How many 1-bit 2-to-1 MUXes are necessary to create an 8-bit 2-to-1 MUX?
B: How many 1-bit 2-to-1 MUXes are necessary to create a 2-bit 4-to-1 MUX?
C: How many 1-bit 2-to-1 MUXes are necessary to create a 1-bit 8-to-1 MUX?
D: How many 2-to-4 decoders are necessary to create a 4-to-16 decoder?
E: How many 1-to-2 decoders are necessary to create a 2-to-4 decoder?
F: How many 3-to-8 decoders are necessary to create a 6-to-64 decoder?

P7 (15 points): Implement the function $G(w,x,y,z) = \sum m(2,6,8,10,13,14,15)$ as follows:
A: Use a K-map to show that G can be written as $G = w\bar{x}\bar{y}\bar{z} + y\bar{z} + wxz$
B: Implement G using only a minimal number (4) of 2-to-1 MUXes and no other gates (NOT gates are not allowed, either). Hint: Use Shannon's Expansion Theorem a few times.