Cpr E 281 HW05 ELECTRICAL AND COMPUTER ENGINEERING IOWA STATE UNIVERSITY	Karnaugh Maps Assigned: Week 5 Due Date: Sep. 30, 2019

P1 (15 points): Given the two functions $F = \bar{b}\bar{c}d$ and $G = \bar{a}bc + ab\bar{d} + \bar{b}\bar{c}d$:
a) Create a minimal cost circuit that implements both F and G using only NOT, AND, and OR gates. Show that the minimal cost circuit has a cost of 24.
b) Implement the circuit that you made in part a using only (a minimal number of) NAND gates. Your circuit should only use 9 NAND gates.

P2 (10 points): Derive the simplest SOP expressions for the given shorthand shorthand expressions.
a) $F_1(X,Y,Z) = \sum m(0,1,3) + D(2,5)$
b) $F_2(W,X,Y,Z) = \sum m(3,7) + D(0,1,2,4,5,6,11,15)$
c) $F_3(W,X,Y,Z) = \sum m(1,2,4,6,9,11,12,14) + D(0,3,5,7,8,10,13,15)$

P3 (10 points): Derive the simplest POS expressions for the given shorthand POS expressions.
a) $G_1(x,y,z) = M_4 + D(0,2,3,5,6)$
b) $G_2(w,x,y,z) = \prod M(7,9) + D(1,3,5,6,8,13)$
c) $G_3(w,x,y,z) = \prod M(1,2,3,5,10,12,13,14) + D(0,4,6,7,8,9,11,15)$

P4 (15 points): Given the function $P(a,b,c,d) = \sum m(2,8,11,13) + D(1,4,5,6,7,10,14,15)$:
a) Derive a simplest SOP expression for P.
b) Derive a simplest POS expression for P.
c) Draw a circuit which implements P but uses only NAND gates.

P5 (10 points): Implement the function $Q(A,B,C) = m_1 + m_6 + D(0,3)$ using only the following: one OR gate, two AND gates, and two NOT gates.

P6 (20 points): Implement the functions $F(w,x,y,z) = \sum m(2,4,5,6,7,10,14,15)$ and $G(w,x,y,z) = \sum m(0,1,2,5,6,9,10,13,14)$ using only AND, OR, and NOT gates. Your solution should have a cost less than 33.

P7 (20 points): A given circuit receives a four-bit number B (b_3, b_2, b_1, b_0) and produces two outputs: output T will be 1 if B is a multiple of 2 or a multiple of 3, whereas output C will be 1 if B is a composite number (4, 6, 8, 9, etc.) Recall that a composite number is a positive integer that has at least one multiple other than 1 and itself. Also, 0 is not a positive integer!
I: Draw the truth table for C and T.
II: Show that C and T can be implemented using 5 OR gates and 2 AND gates. Assume that the complemented inputs are available; that is, you do not need NOT gates to produce $\bar{b}_3, \bar{b}_2, \bar{b}_1, \bar{b}_0$ since these are also usable as external inputs to your circuit.