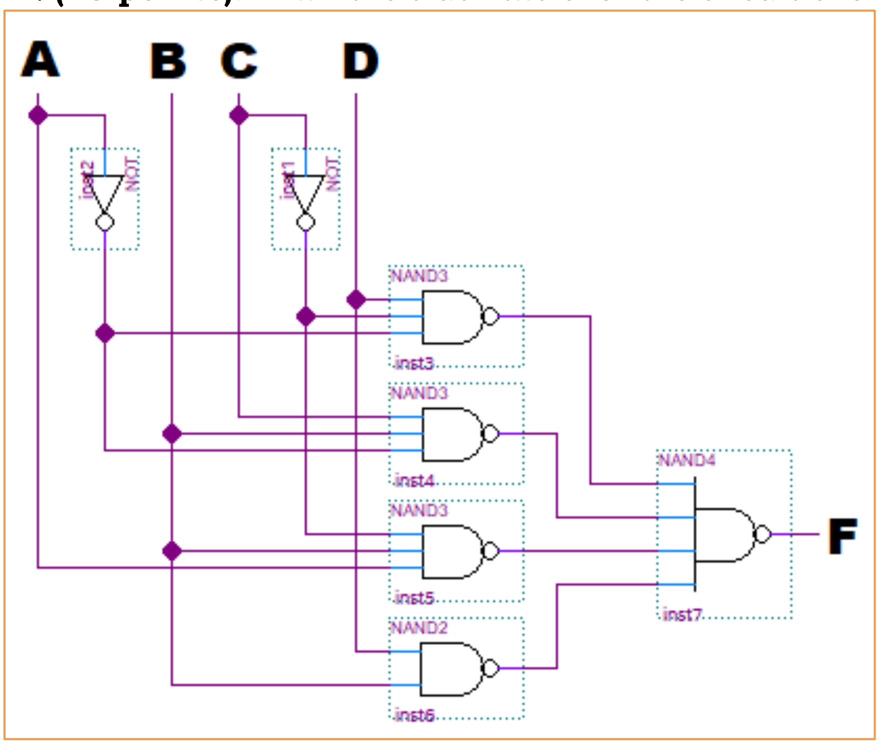
Cpr E 281 HW03
ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

NAND/NOR Gates with Synthesis
Assigned: Week 3
Due Date: Sep. 16, 2019

P1 (10 points): Given the expression $F(a,b,c,d) = \prod M(0,1,5,6,13,14)$, perform the following:

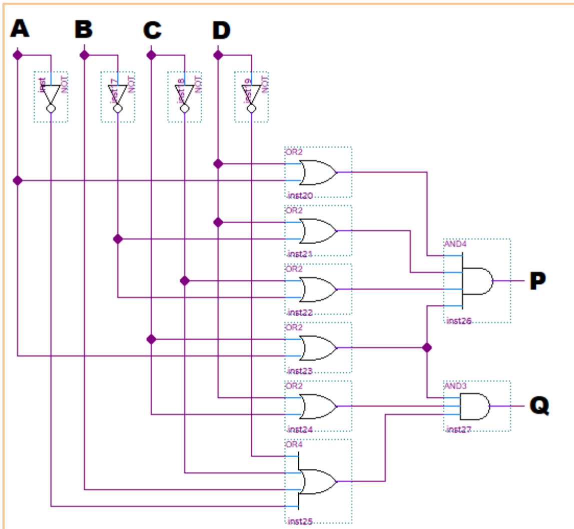
a. Write the expression for F as a shorthand SOP expression.
b. Write the expression for F as a simplified POS expression.
c. Show how the expression for F can be implemented as a digital circuit using exactly three NOT gates, three OR gates, and one AND gate.

P2 (10 points): Draw the truth table for the circuit shown below.



P3 (10 points): Given the expression $G(W,X,Y,Z) = \sum m(0,1,3,7,8,15)$, implement this function using no more than 8 NAND gates. The NAND gates that you use may have any number of inputs. You may not use NOT gates to create this circuit.

P4 (10 points): Convert the following circuit into a circuit that only uses NOR gates and NOT gates. Your circuit should use no more than 8 NOR gates.



P5 (16 points): Given the expression $H(A, B, C) = \sum m(0, 1, 5, 7)$, perform the following:

a. Write the expression for H as a simplified SOP expression.
b. Write the expression for H as a simplified POS expression.
c. Implement H using exactly five NOR gates and no other gates.
d. Did you use the SOP expression or the POS expression to implement the circuit? Why?

P6 (24 points): Show how to implement the following:

a. Implement a 4-input AND gate using three 2-input AND gates.
b. Implement a 4-input NAND gate using five 2-input NAND gates.
c. Implement a 2-input AND gate using any number of OR and NOT gates. Hint: remember how DeMorgan's Theorem can be used to change between AND and OR operations.
d. Implement a 2-to-1 multiplexer (MUX) using only 2-input NAND gates. Hint: use the expression that describes the output of a MUX.

P7 (20 points): A **Full Adder** is a circuit that adds three bits (X, Y, and Z) together and returns two bits (C and S) to represent the total as a 2-bit binary number, where C is the most significant bit (MSB) and S is the least significant bit (LSB). For example, let X=1, Y=0, and Z=1. Here, the total should be $2_{10} = 10_2$, and the outputs are, correspondingly, C=1 and S=0.
A: Derive the truth tables for C and S.
B: Write the functions C and S in shorthand notation using minterms.
C: Repeat part B but use maxterms instead.
D: Obtain the simplest SOP expressions for the functions C and S and draw a circuit which implements the **Full Adder**.