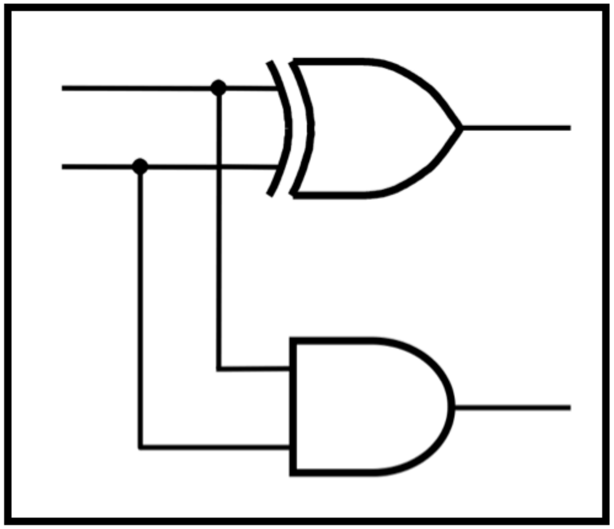


CprE 281: Digital Logic

Instructor: Alexander Stoytchev

http://www.ece.iastate.edu/~alexs/classes/

Logic Gates

CprE 281: Digital Logic
Iowa State University, Ames, IA

Administrative Stuff

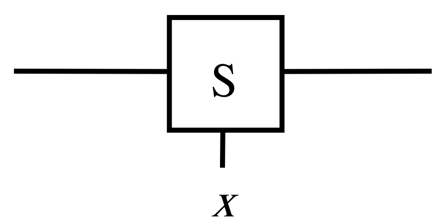
- HW1 is out
- It is due on Monday Aug 27 @ 4pm.
- Submit it on paper before the start of the lecture
- No late homeworks will be accepted.
- Staple all of your pages
- Please write clearly on the first page:
  - your name
  - student ID
  - lab section letter

Labs Next Week

- **Please download and read the lab assignment for next week before you go to your lab section.**
- **You must print the answer sheet and do the prelab before you go to the lab.**
- **The TAs will check your prelab answers at the beginning of the recitation. If you don't have it done you'll lose 20% of the lab grade for that lab.**

A Binary Switch

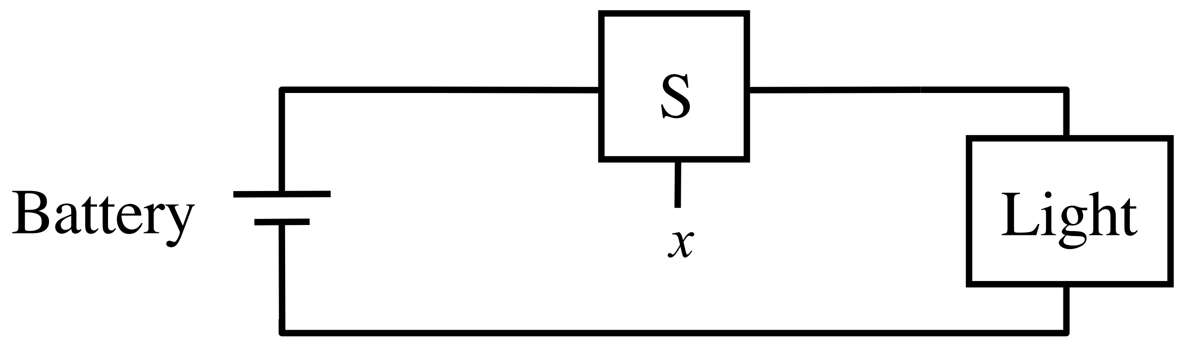
(a) Two states of a switch



(b) Symbol for a switch

[Figure 2.1 from the textbook]

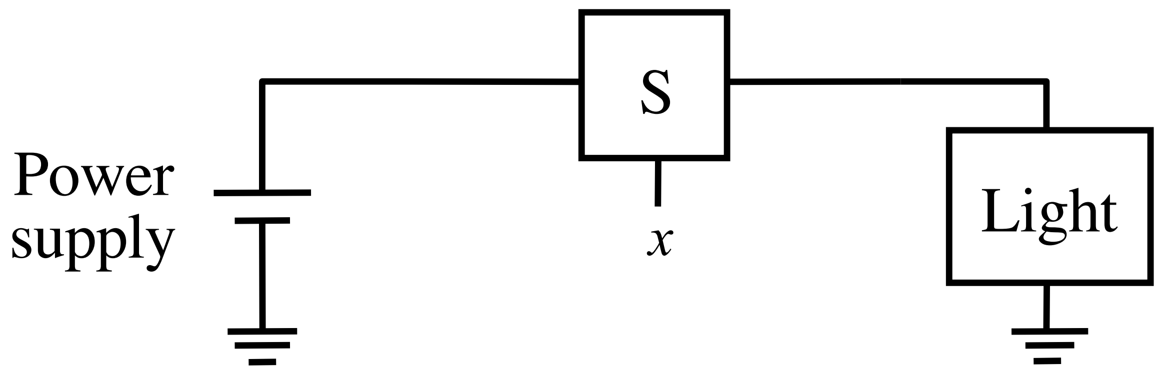
A Light Controlled by a Switch



(a) Simple connection to a battery

[Figure 2.2a from the textbook]

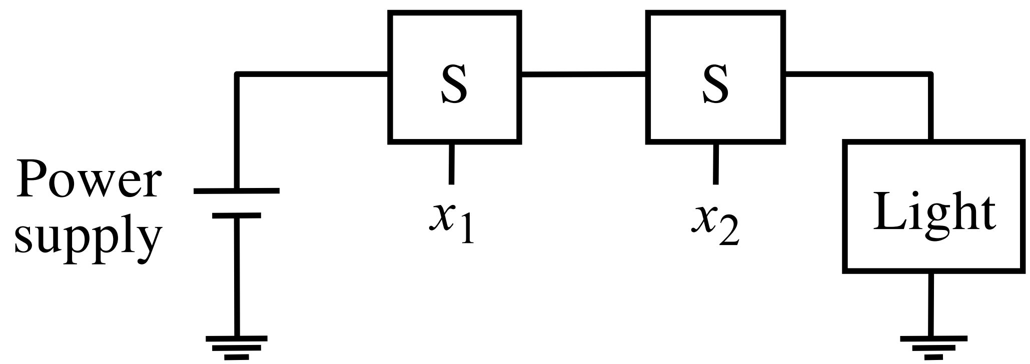
A Light Controlled by a Switch



(b) Using a ground connection as the return path

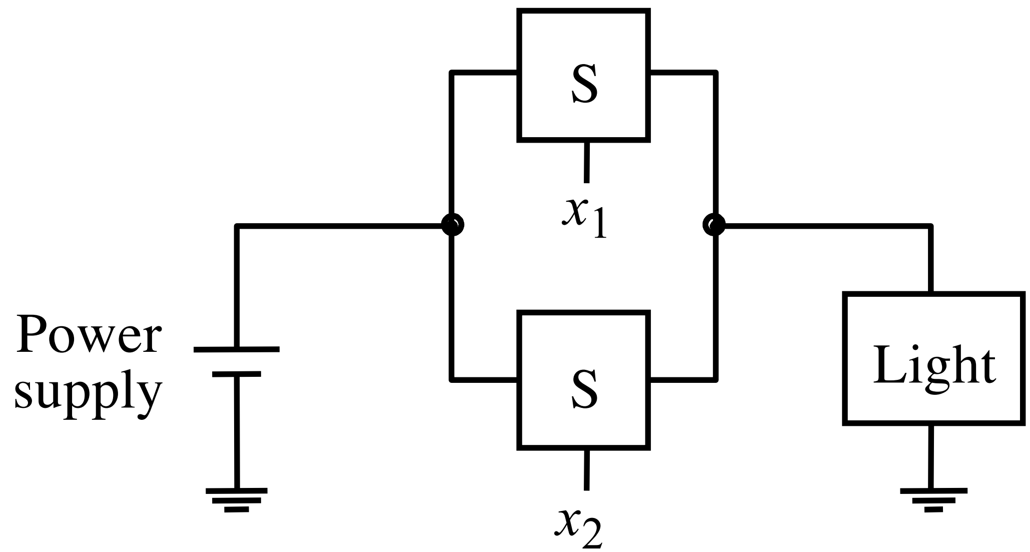
[Figure 2.2b from the textbook]

The Logical AND function
(series connection of the switches)



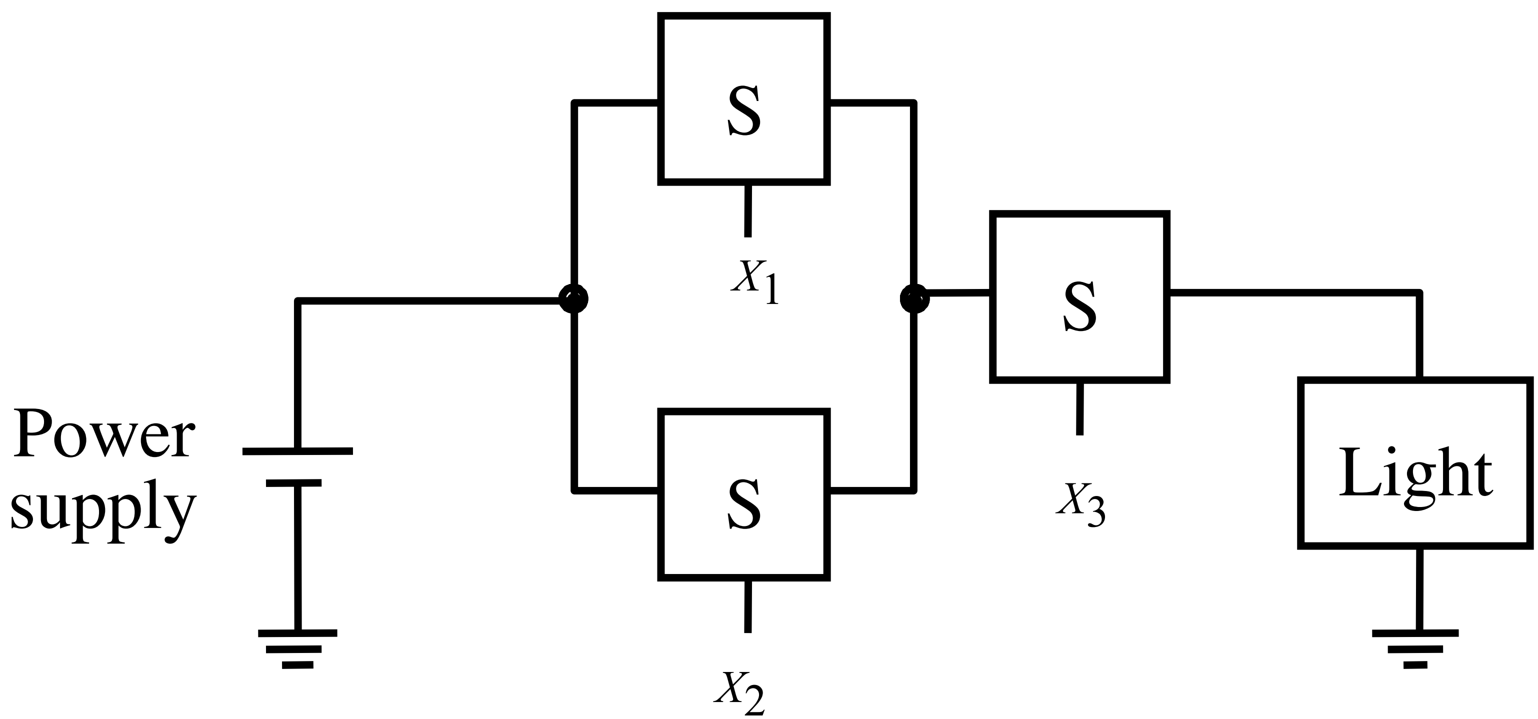
[Figure 2.3a from the textbook]

The Logical OR function
(parallel connection of the switches)



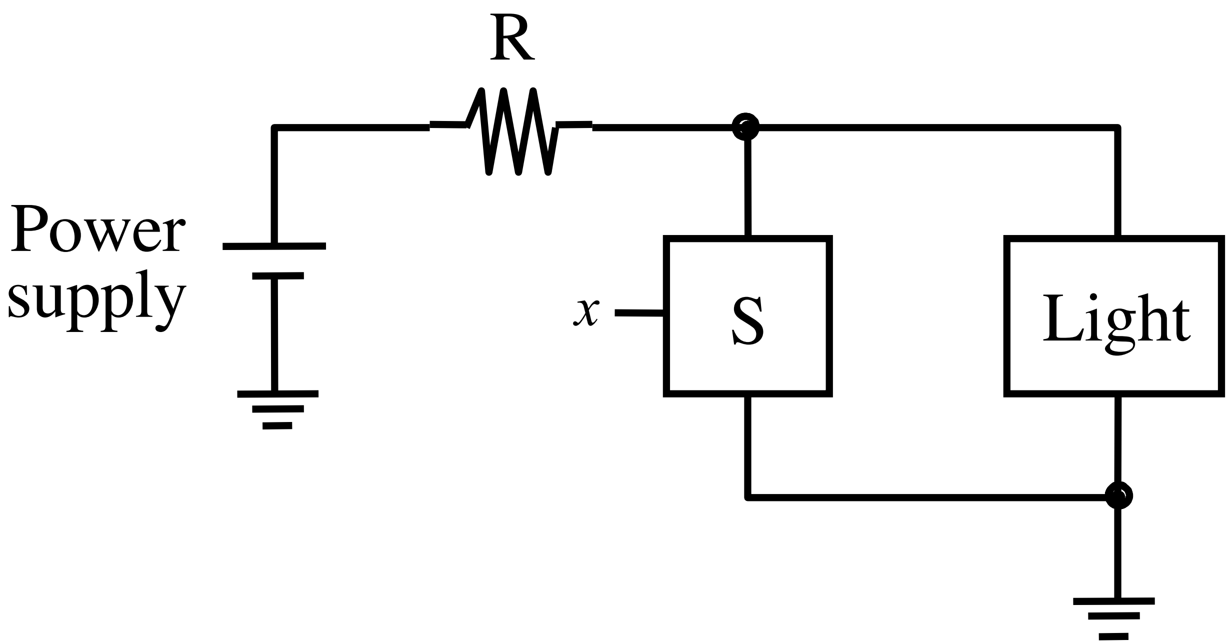
[Figure 2.3b from the textbook]

A series-parallel connection of the switches



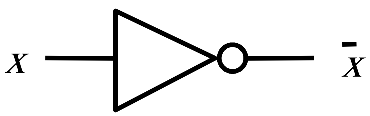
[Figure 2.4 from the textbook]

An Inverting Circuit

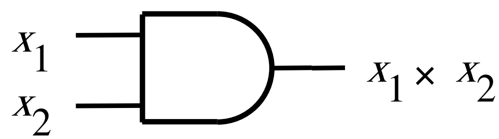


[Figure 2.5 from the textbook]

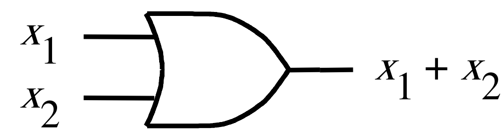
The Three Basic Logic Gates



NOT gate



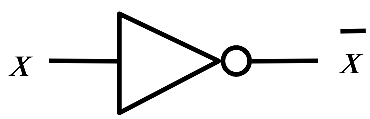
AND gate



OR gate

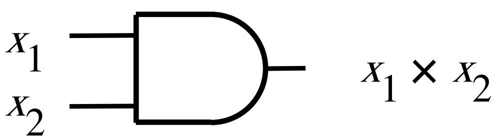
[Figure 2.8 from the textbook]

Truth Table for NOT



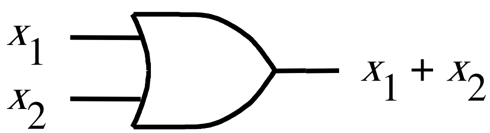
x	$\overline{x}$
0	1
1	0

Truth Table for AND



x_1	x_2	$x_1 \cdot x_2$
0	0	0
0	1	0
1	0	0
1	1	1

Truth Table for OR



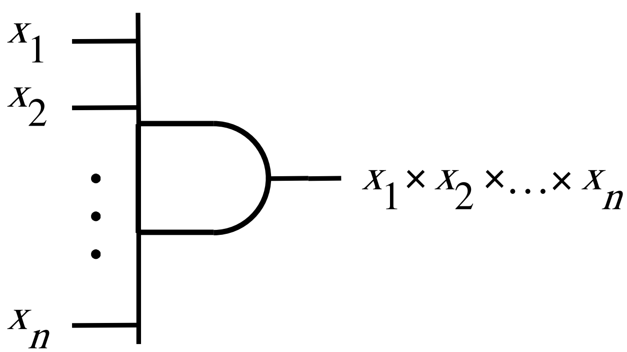
x_1	x_2	$x_1 + x_2$
0	0	0
0	1	1
1	0	1
1	1	1

Truth Tables for AND and OR

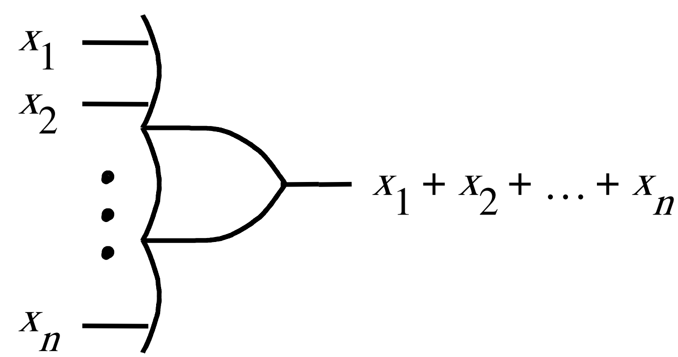
x_1	x_2	$x_1 \cdot x_2$	$x_1 + x_2$
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	1
		AND	OR

[Figure 2.6b from the textbook]

Logic Gates with n Inputs



AND gate



OR gate

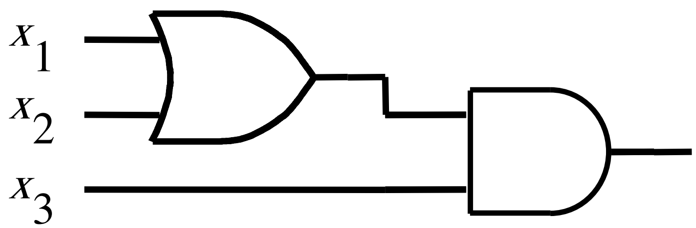
[Figure 2.8 from the textbook]

Truth Table for 3-input AND and OR

x_1	x_2	x_3	$x_1 \cdot x_2 \cdot x_3$	$x_1 + x_2 + x_3$
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	0	1
1	0	0	0	1
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

[Figure 2.7 from the textbook]

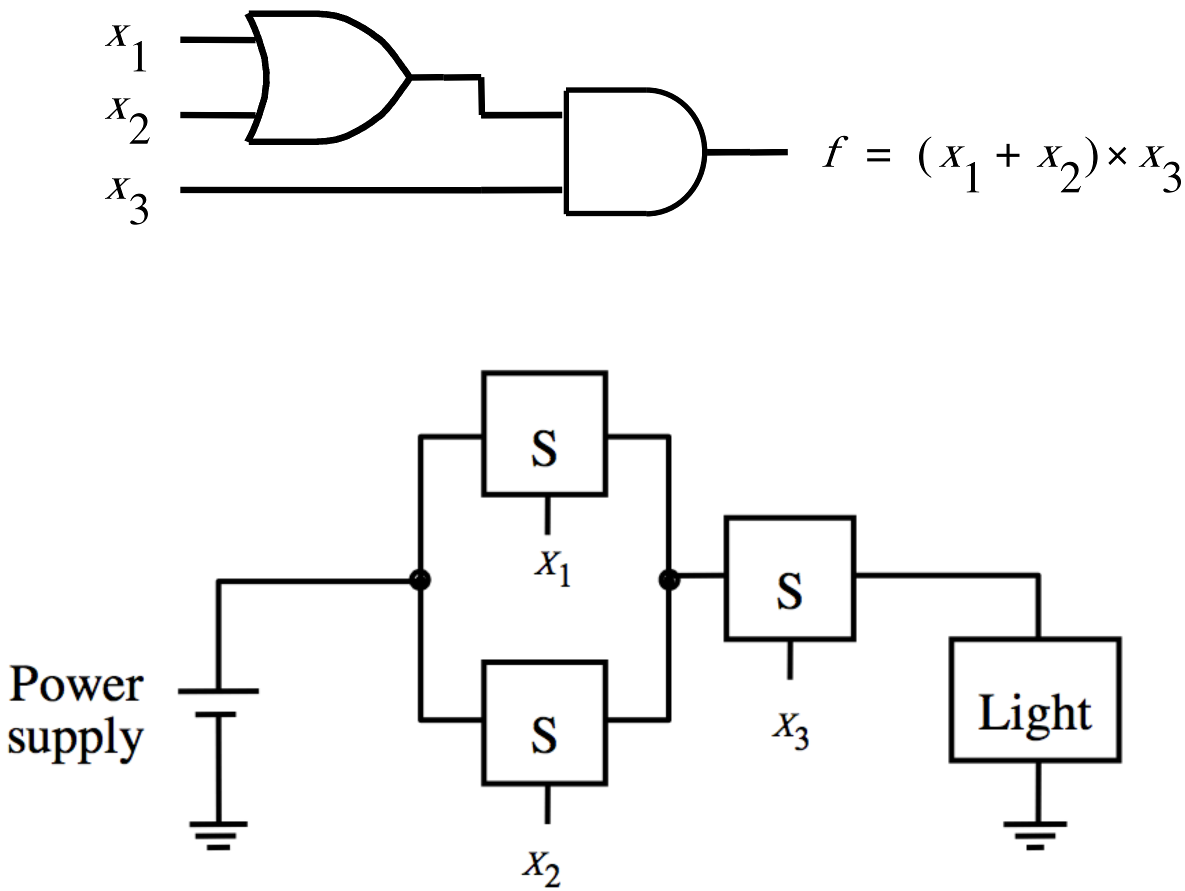
Example of a Logic Circuit Implemented with Logic Gates



$f = (x_1 + x_2) \times x_3$

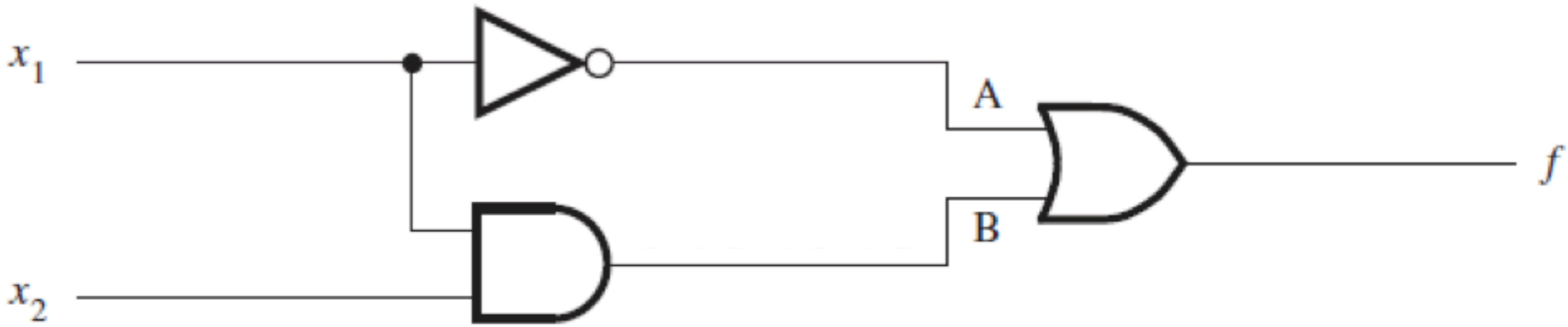
[Figure 2.8 from the textbook]

Example of a Logic Circuit Implemented with Logic Gates



[Figure 2.8 from the textbook]

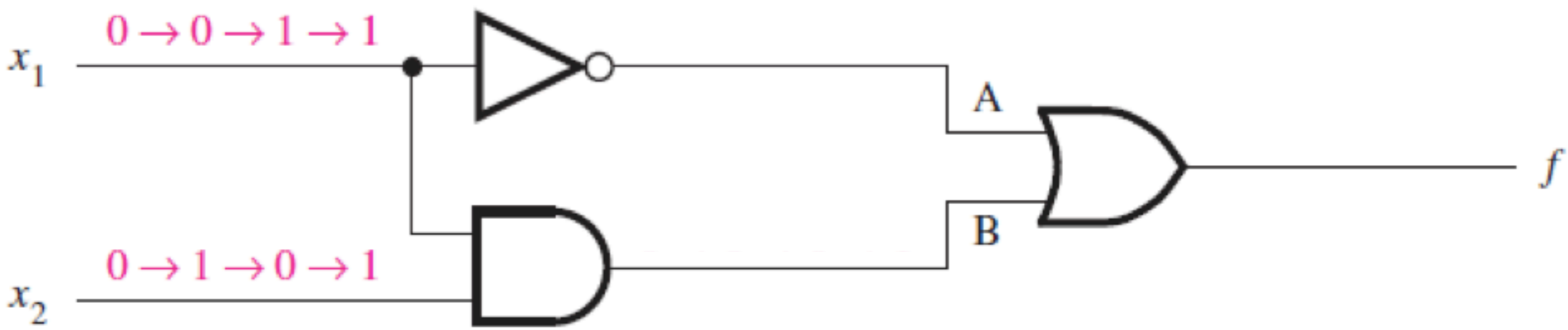
Network Analysis



(a) Network that implements $f = \bar{x}_1 + x_1 \cdot x_2$

[Figure 2.10 from the textbook]

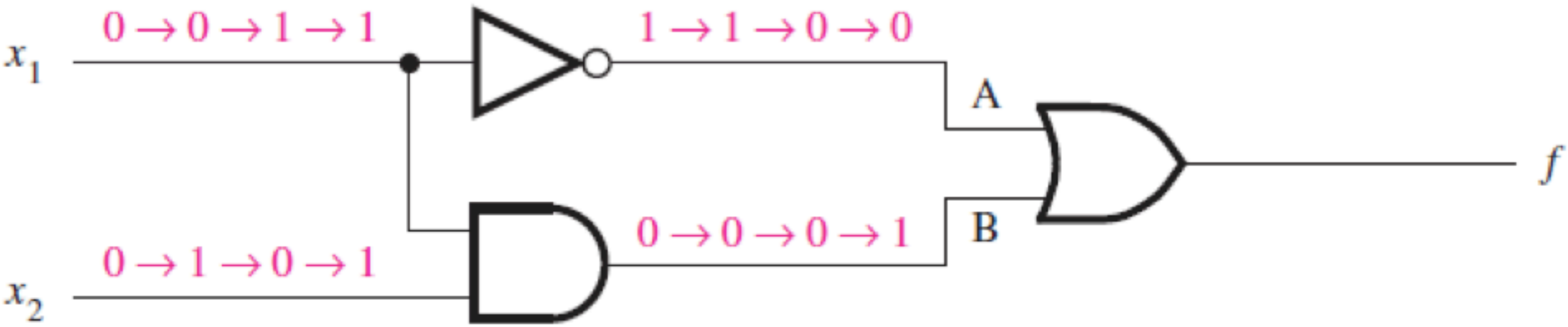
Network Analysis



(a) Network that implements $f = \bar{x}_1 + x_1 \cdot x_2$

[Figure 2.10 from the textbook]

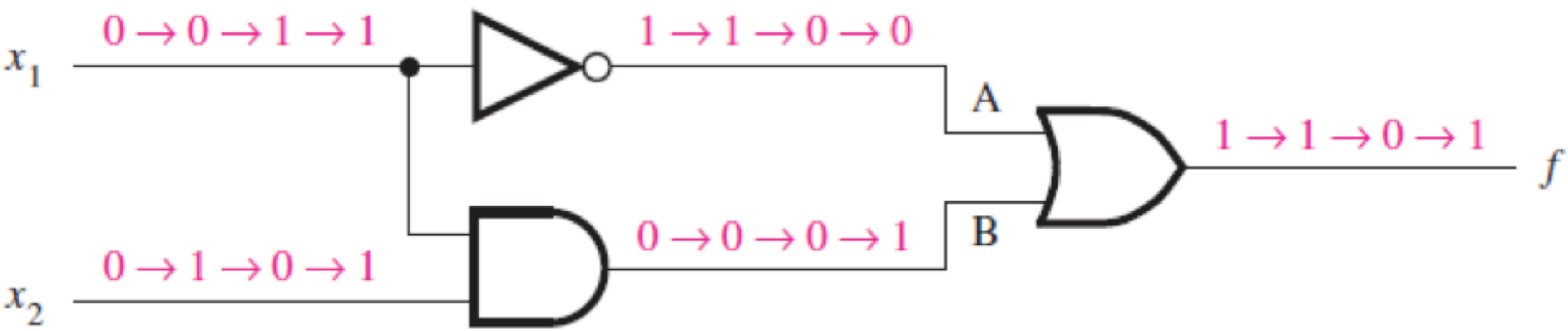
Network Analysis



(a) Network that implements $f = \bar{x}_1 + x_1 \cdot x_2$

[Figure 2.10 from the textbook]

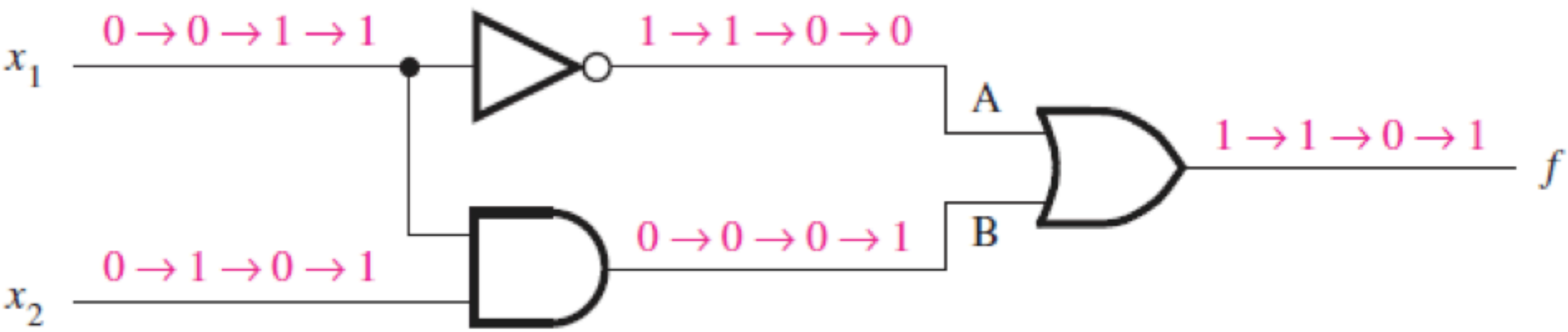
Network Analysis



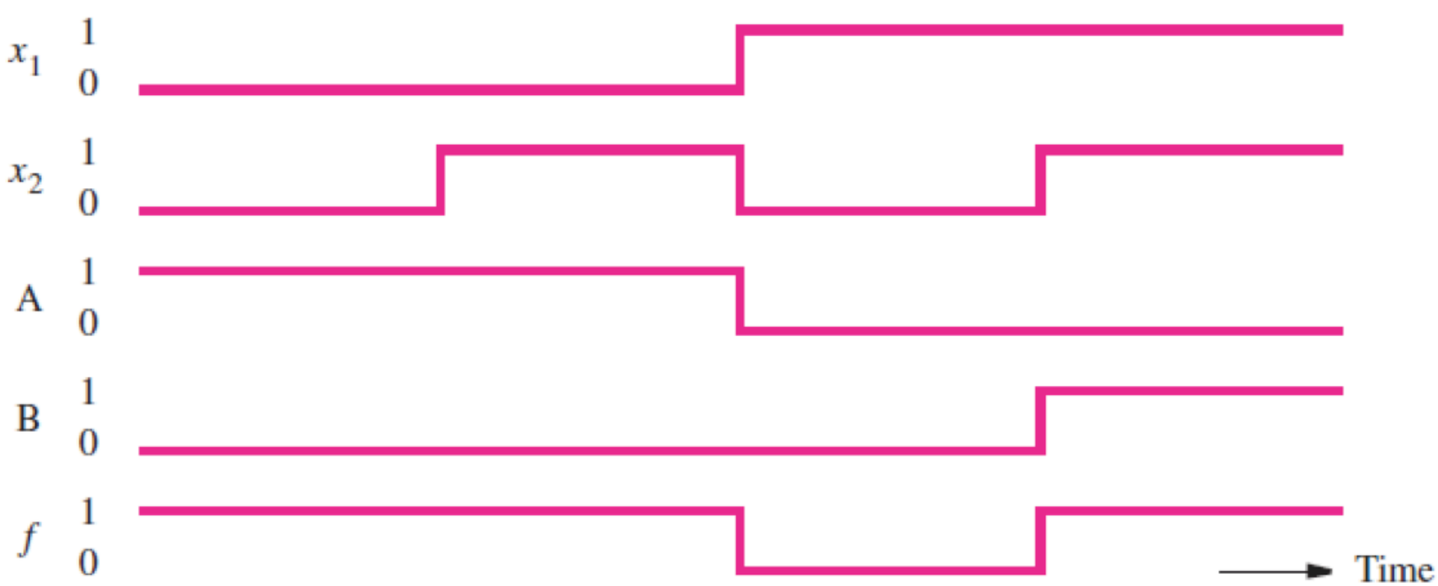
(a) Network that implements $f = \bar{x}_1 + x_1 \cdot x_2$

[Figure 2.10 from the textbook]

Network Analysis

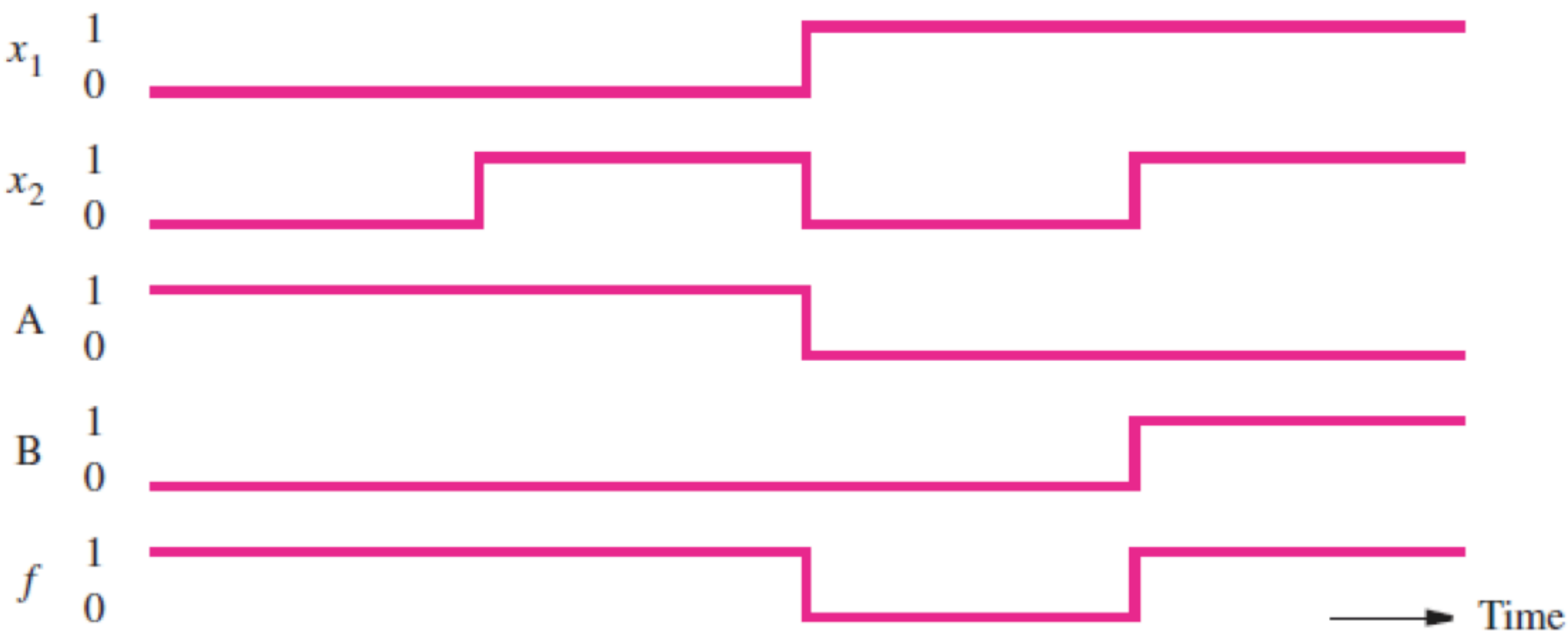


(a) Network that implements $f = \bar{x}_1 + x_1 \cdot x_2$



[Figure 2.10 from the textbook]

Timing Diagram



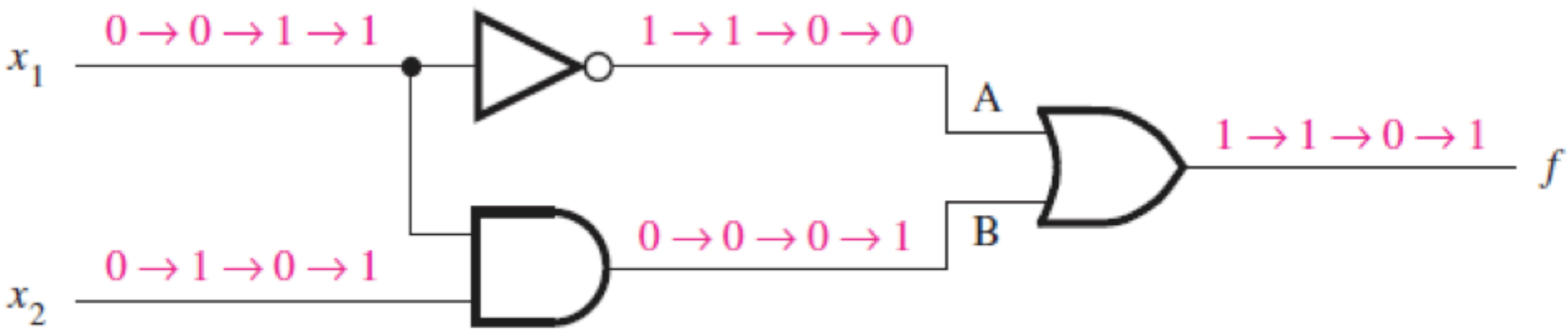
[Figure 2.10 from the textbook]

Truth Table for this Network

x_1	x_2	$f(x_1, x_2)$	A	B
0	0	1	1	0
0	1	1	1	0
1	0	0	0	0
1	1	1	0	1

[Figure 2.10 from the textbook]

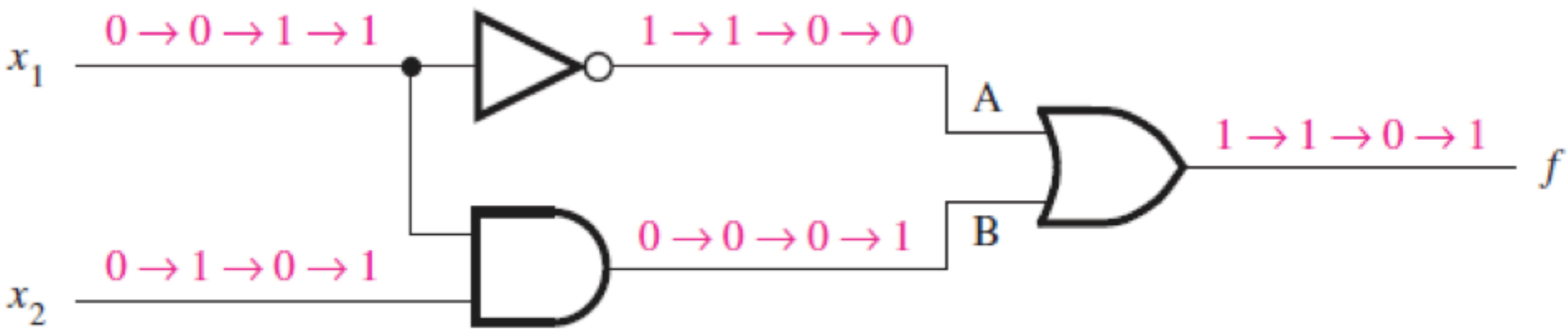
Functionally Equivalent Networks



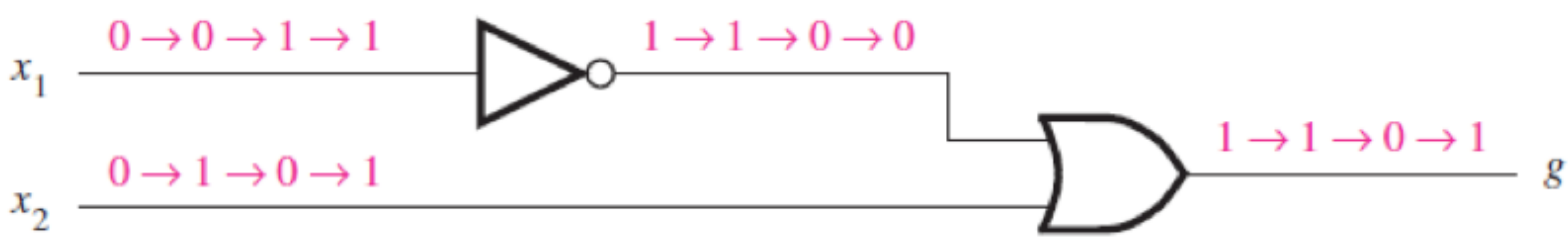
(a) Network that implements $f = \bar{x}_1 + x_1 \cdot x_2$

[Figure 2.10 from the textbook]

Functionally Equivalent Networks



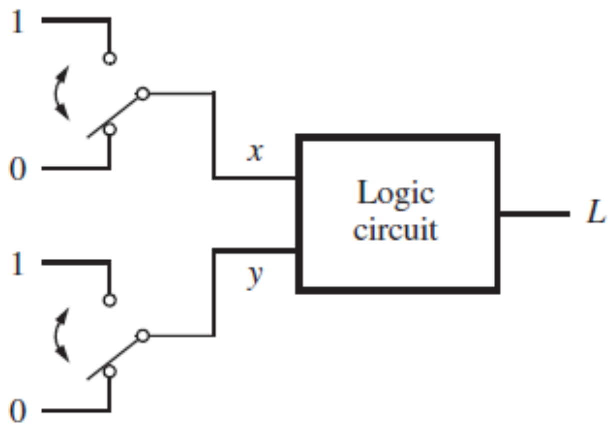
(a) Network that implements $f = \bar{x}_1 + x_1 \cdot x_2$



(d) Network that implements $g = \bar{x}_1 + x_2$

[Figure 2.10 from the textbook]

The XOR Logic Gate



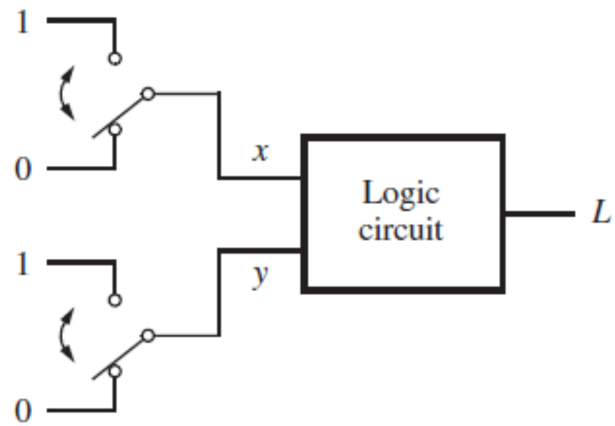
(a) Two switches that control a light

x	y	L
0	0	0
0	1	1
1	0	1
1	1	0

(b) Truth table

[Figure 2.11 from the textbook]

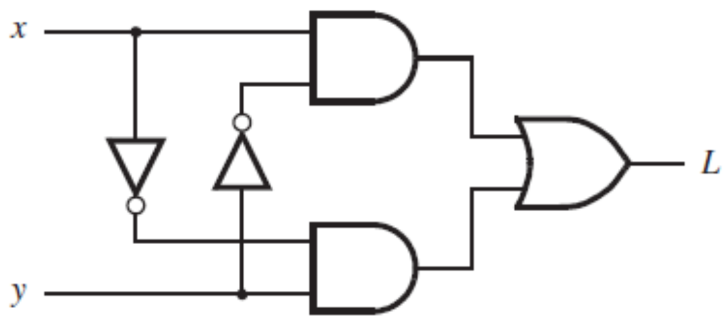
The XOR Logic Gate



(a) Two switches that control a light

x	y	L
0	0	0
0	1	1
1	0	1
1	1	0

(b) Truth table

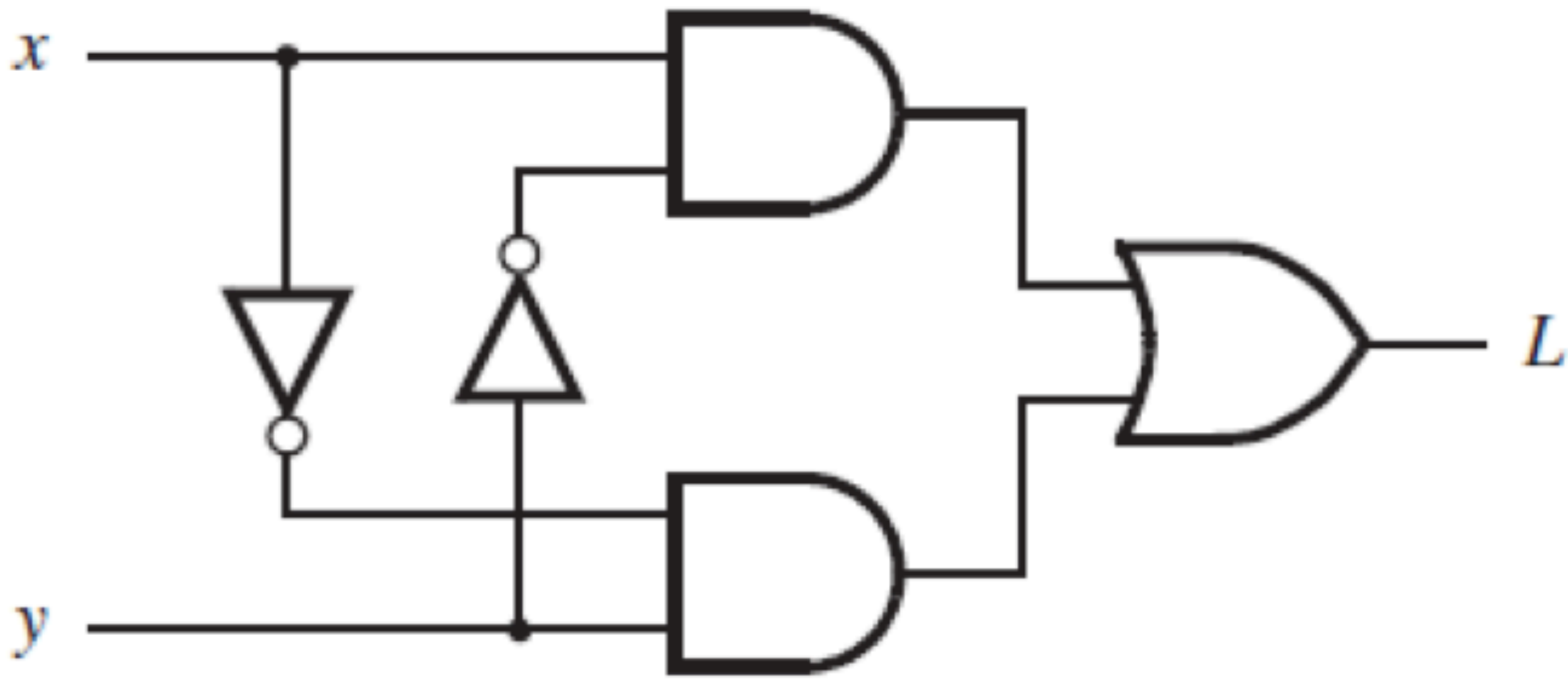


(c) Logic network

(d) XOR gate symbol

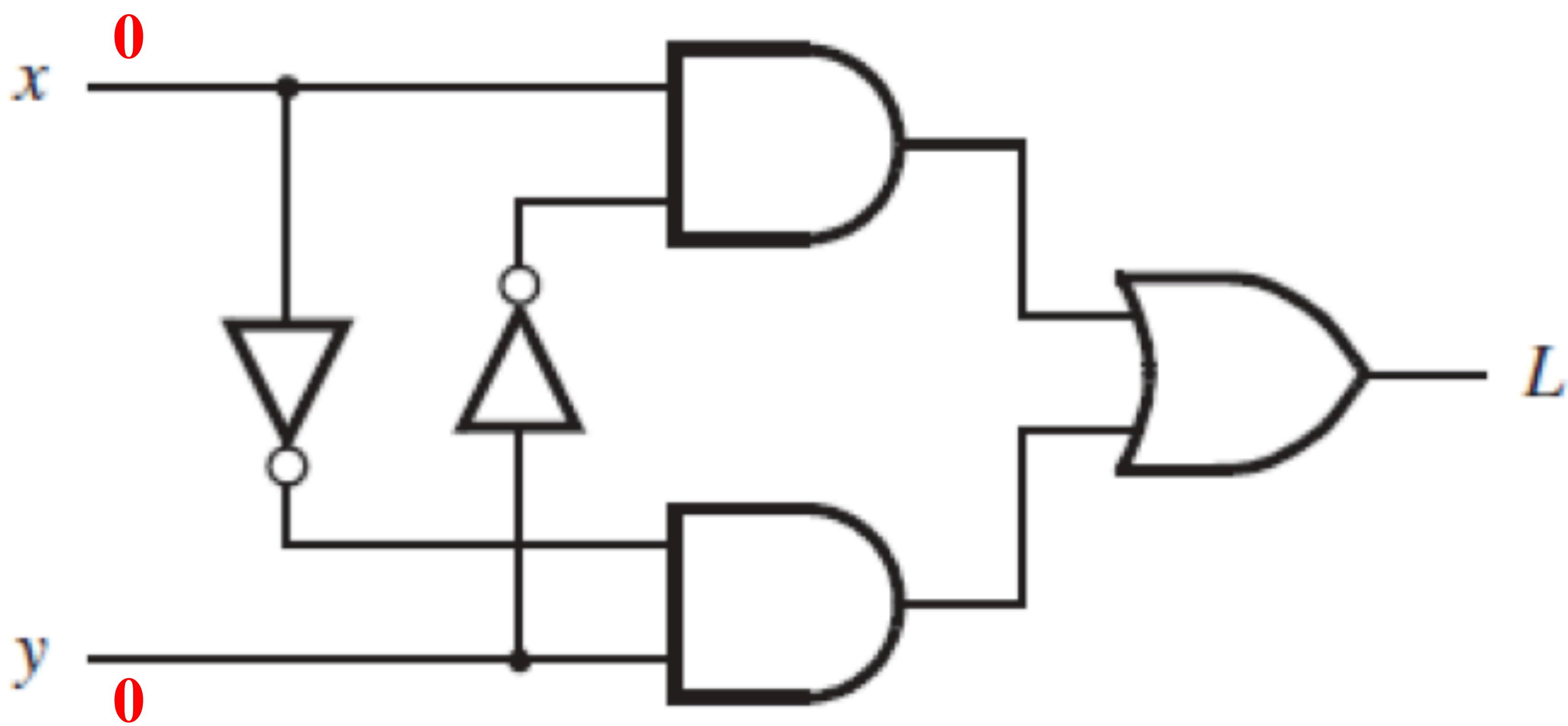
[Figure 2.11 from the textbook]

XOR Analysis

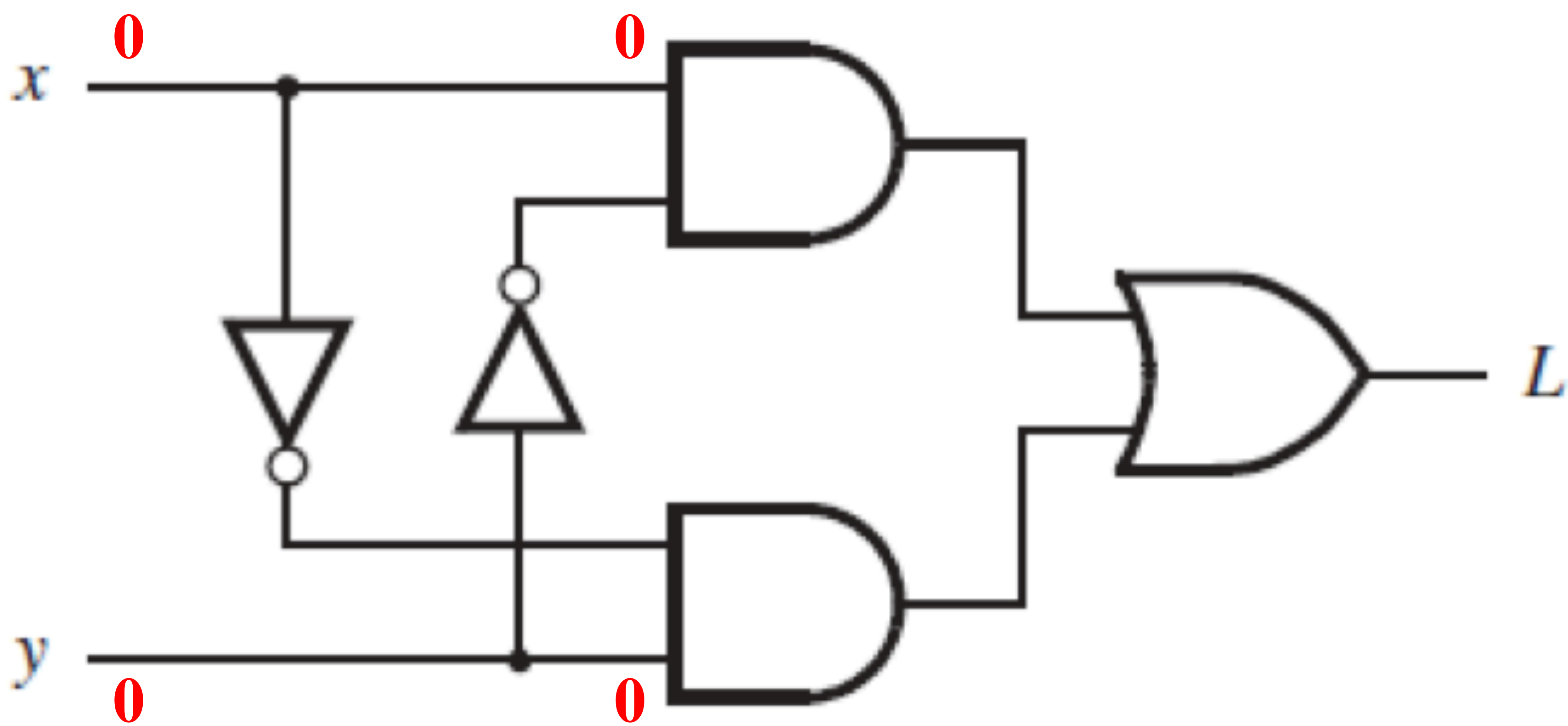


[Figure 2.11c from the textbook]

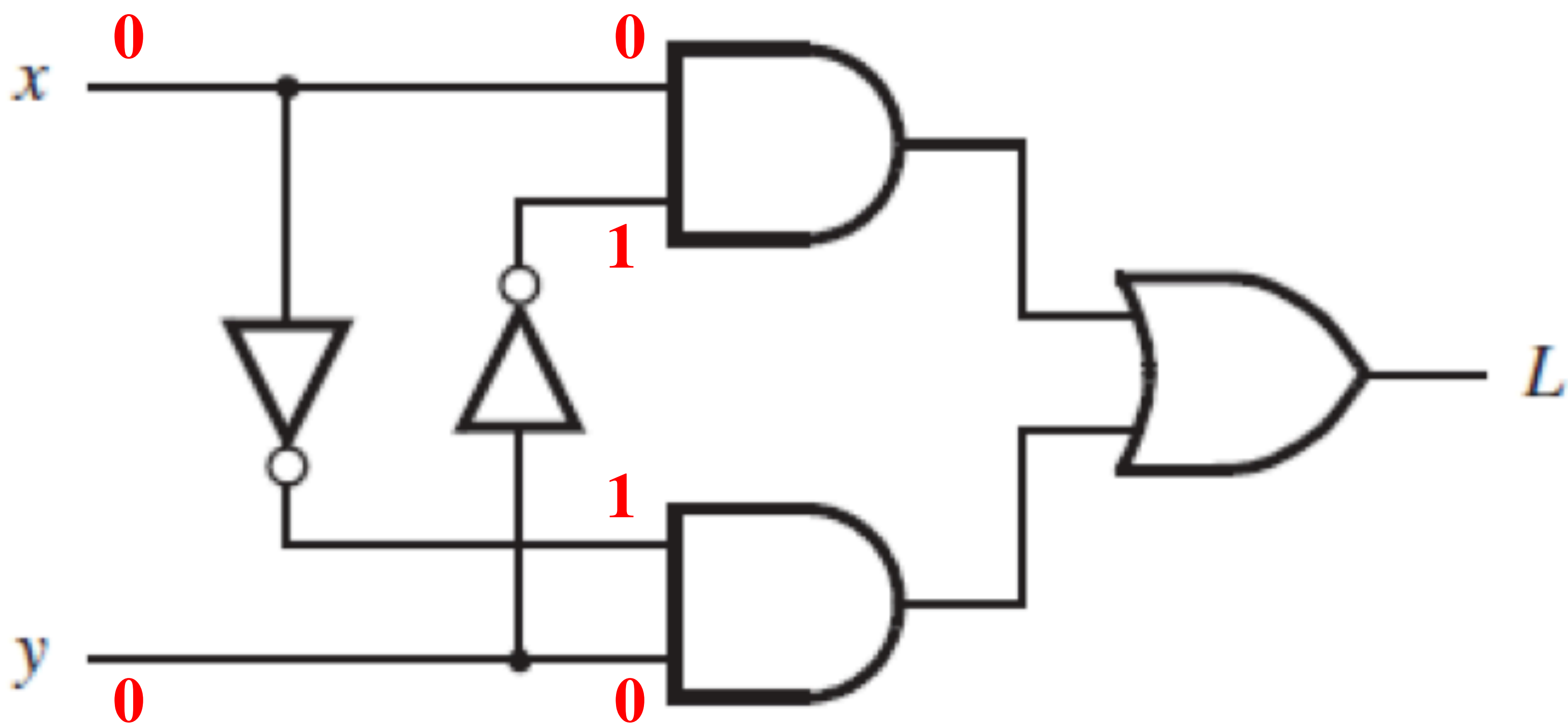
XOR Analysis (x=0, y=0)



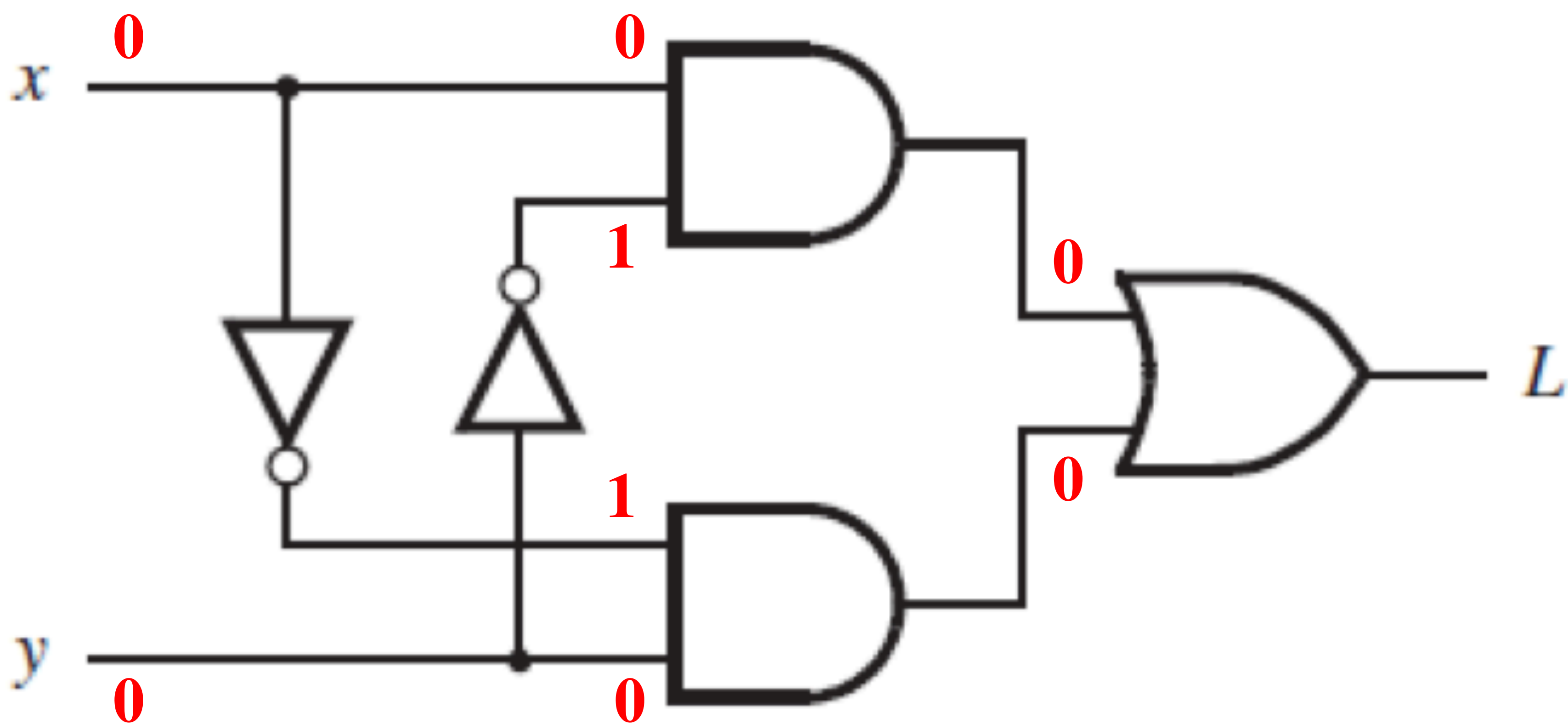
XOR Analysis (x=0, y=0)



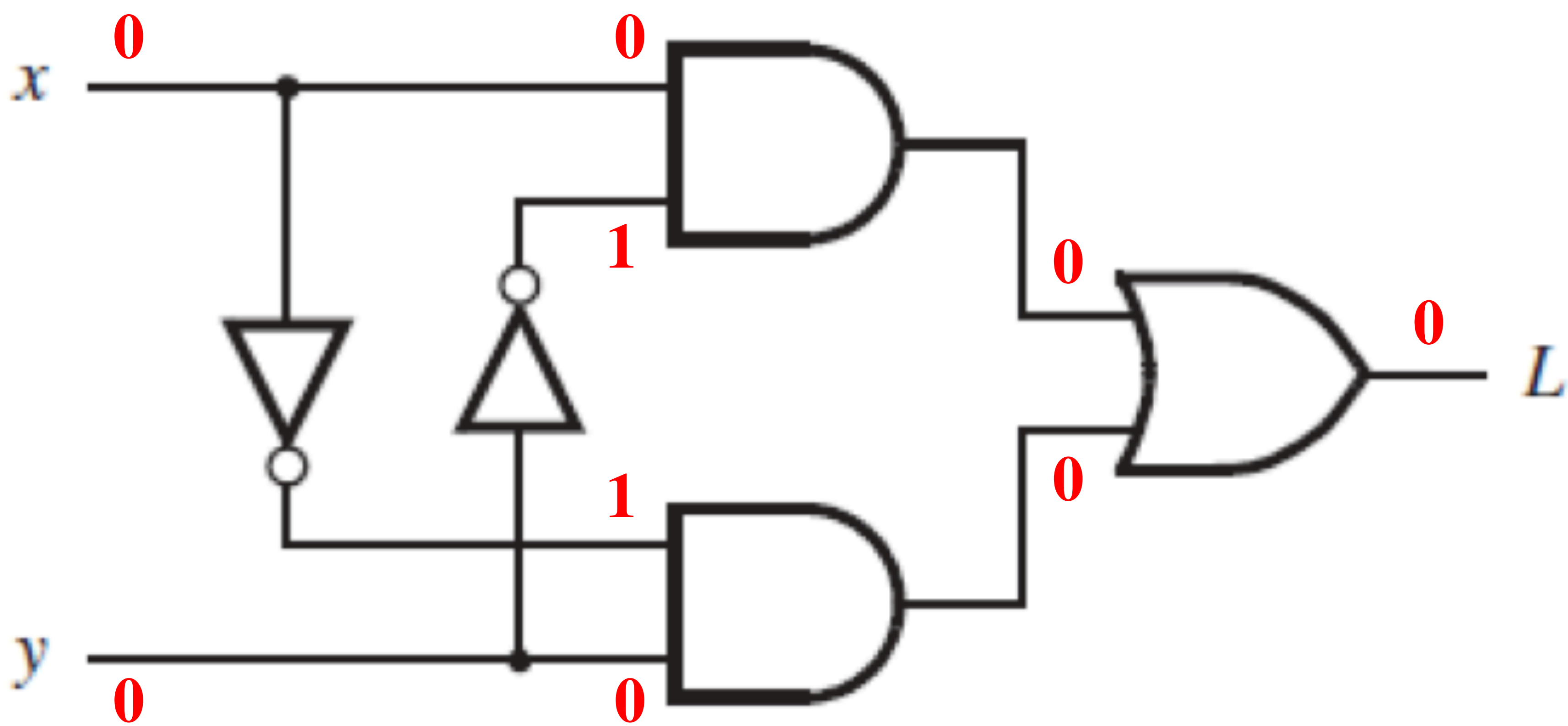
XOR Analysis (x=0, y=0)



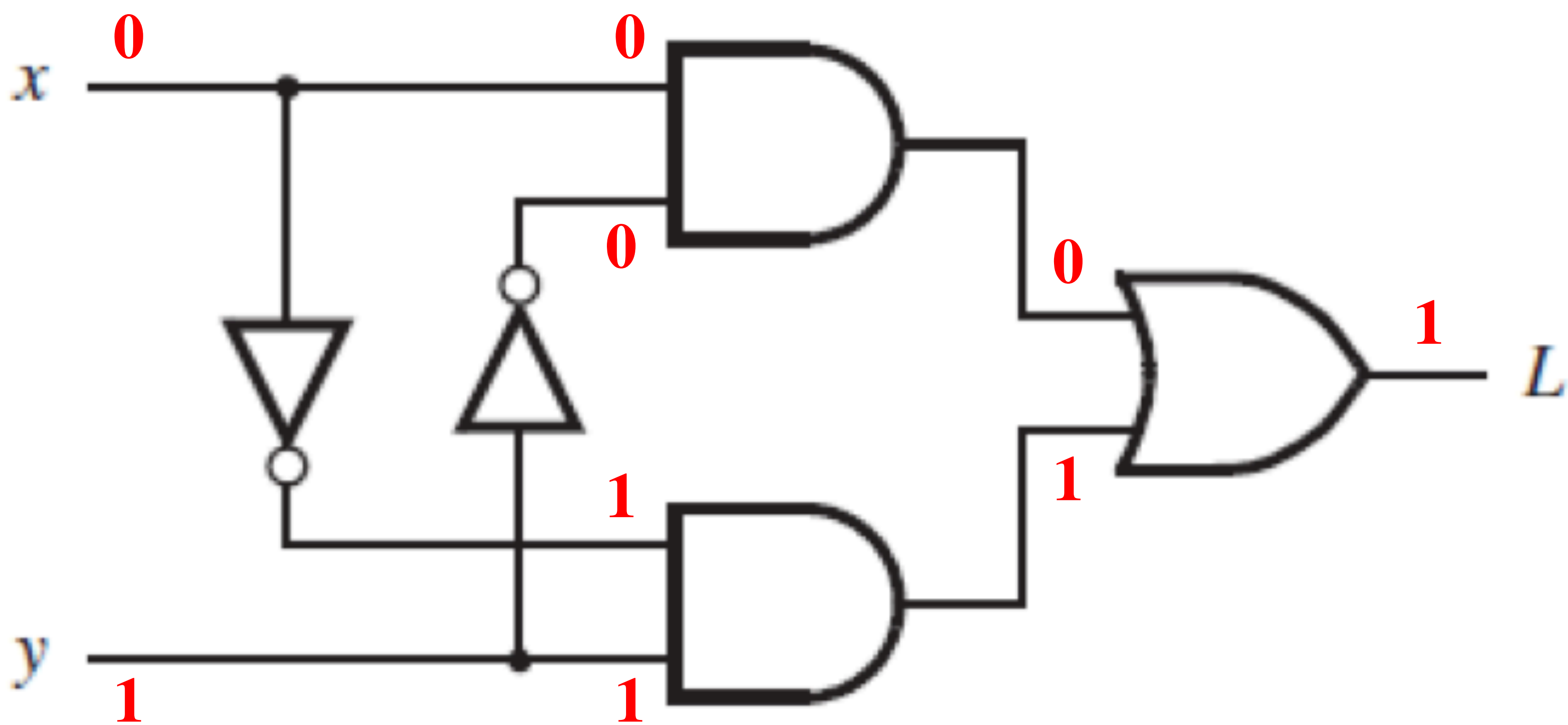
XOR Analysis (x=0, y=0)



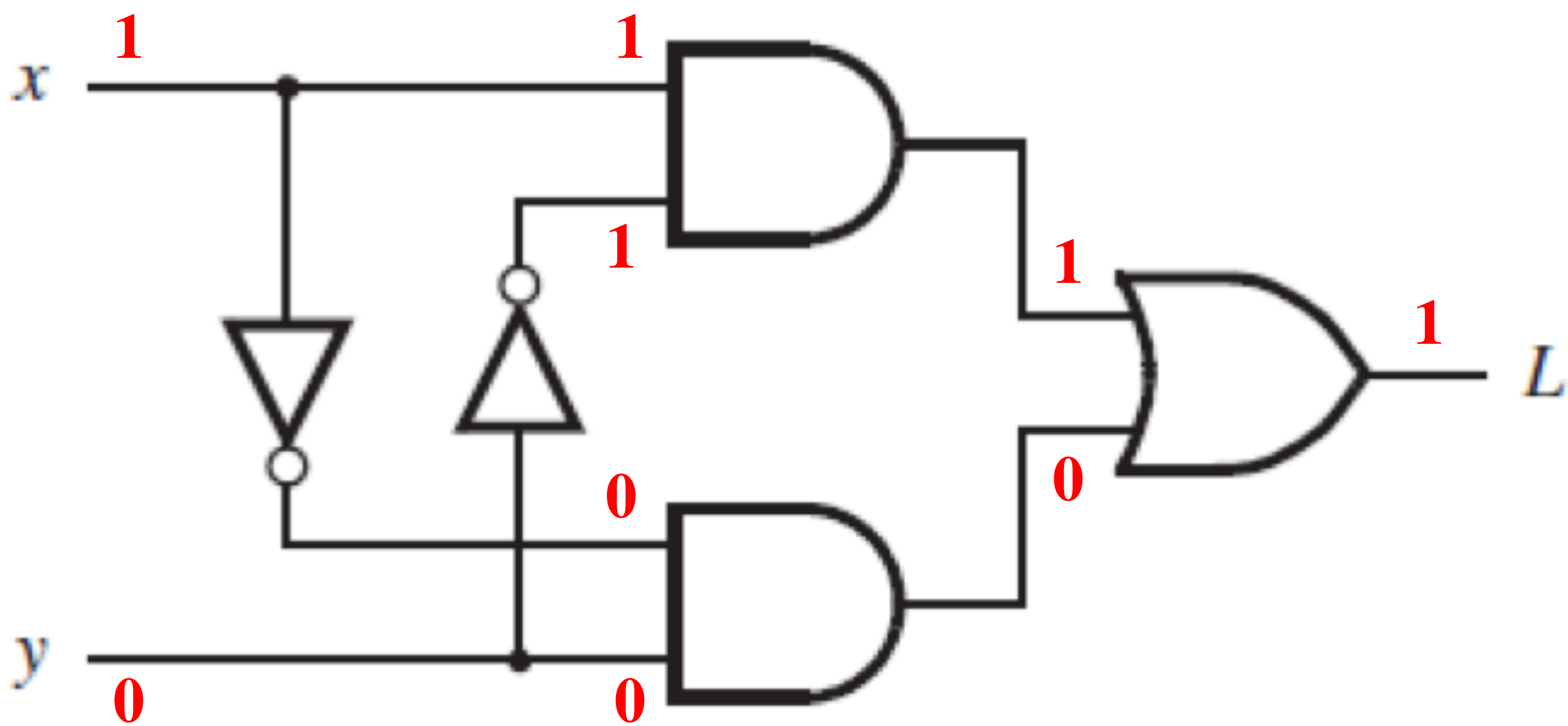
XOR Analysis (x=0, y=0)



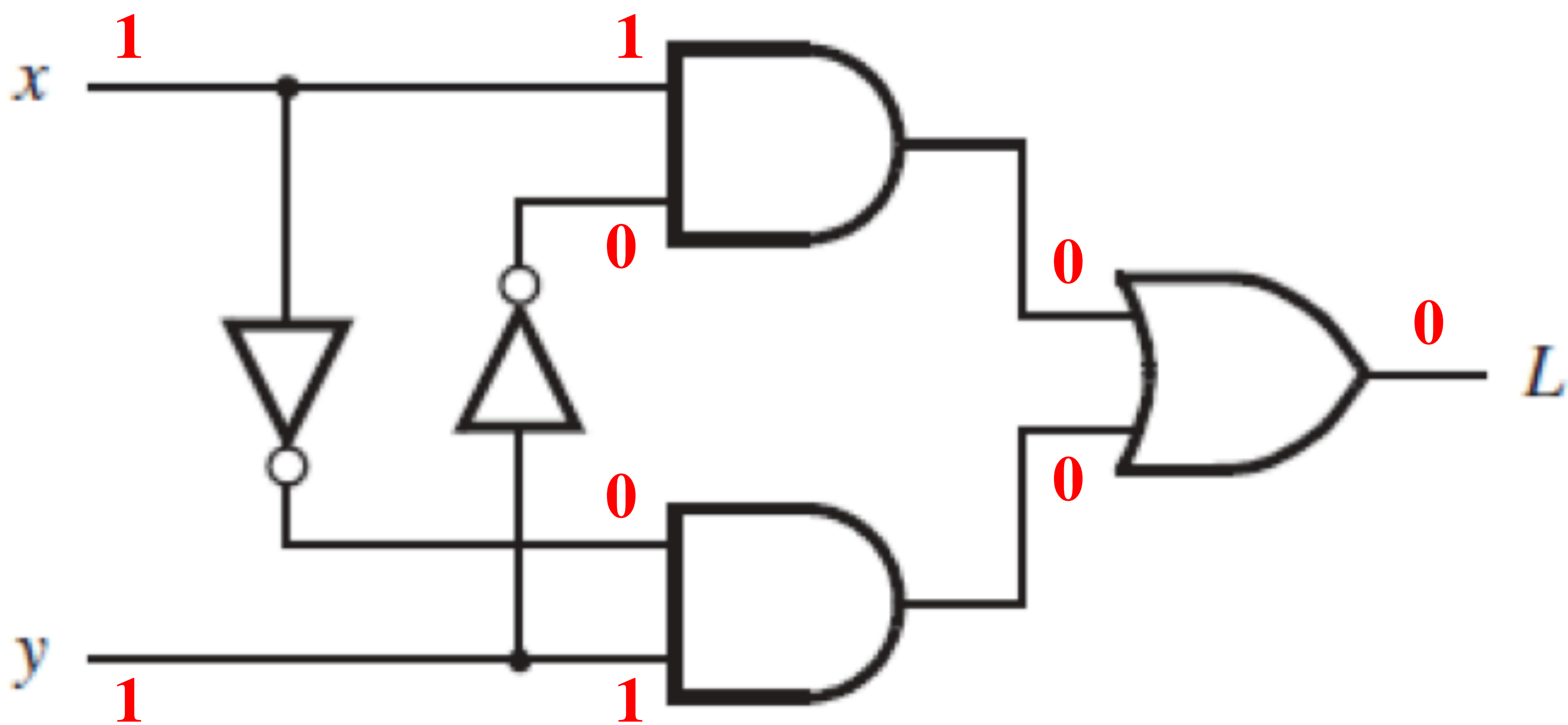
XOR Analysis (x=0, y=1)



XOR Analysis (x=1, y=0)



XOR Analysis (x=1, y=1)



Addition of Binary Numbers

$$
\begin{array}{r}
a \\
+\,b \\
\hline
s_1\,s_0
\end{array}
\qquad\qquad
\begin{array}{r}
0 \\
+\,0 \\
\hline
0\;0
\end{array}
\qquad
\begin{array}{r}
0 \\
+\,1 \\
\hline
0\;1
\end{array}
\qquad
\begin{array}{r}
1 \\
+\,0 \\
\hline
0\;1
\end{array}
\qquad
\begin{array}{r}
1 \\
+\,1 \\
\hline
1\;0
\end{array}
$$

[Figure 2.12 from the textbook]

Addition of Binary Numbers

$$\begin{array}{r} a \\ +\,b \\ \hline s_1\,s_0 \end{array} \qquad \begin{array}{r} 0 \\ +\,0 \\ \hline 0\;0 \end{array} \quad \begin{array}{r} 0 \\ +\,1 \\ \hline 0\;1 \end{array} \quad \begin{array}{r} 1 \\ +\,0 \\ \hline 0\;1 \end{array} \quad \begin{array}{r} 1 \\ +\,1 \\ \hline 1\;0 \end{array}$$

a	b	s_1	s_0
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

[Figure 2.12 from the textbook]

Addition of Binary Numbers

a	0	0	1	1
$+b$	$+0$	$+1$	$+0$	$+1$
$s_1\,s_0$	0 0	0 1	0 1	1 0

a	b	s_1	s_0
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Addition of Binary Numbers

a	0	0	1	1
$+\,b$	$+\,0$	$+\,1$	$+\,0$	$+\,1$
$s_1\,s_0$	0 0	0 1	0 1	1 0

a	b	s_1	s_0
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Addition of Binary Numbers

$$\begin{array}{r} a \\ +\,b \\ \hline s_1\,s_0 \end{array} \qquad \begin{array}{r} 0 \\ +\,0 \\ \hline 0\,0 \end{array} \quad \begin{array}{r} 0 \\ +\,1 \\ \hline 0\,1 \end{array} \quad \begin{array}{r} 1 \\ +\,0 \\ \hline 0\,1 \end{array} \quad \begin{array}{r} 1 \\ +\,1 \\ \hline 1\,0 \end{array}$$

a	b	s_1	s_0
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Addition of Binary Numbers

a	0	0	1	1
$+b$	$+0$	$+1$	$+0$	$+1$
$s_1\, s_0$	0 0	0 1	0 1	1 0

a	b	s_1	s_0
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Addition of Binary Numbers

a	0	0	1	1
$+\,b$	+0	+1	+0	+1
$s_1\,s_0$	0 0	0 1	0 1	1 0

a	b	s_1	s_0
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Addition of Binary Numbers

$$\begin{array}{r} a \\ +\,b \\ \hline s_1\,s_0 \end{array} \qquad \begin{array}{r} 0 \\ +\,0 \\ \hline 0\;0 \end{array} \qquad \begin{array}{r} 0 \\ +\,1 \\ \hline 0\;1 \end{array} \qquad \begin{array}{r} 1 \\ +\,0 \\ \hline 0\;1 \end{array} \qquad \begin{array}{r} 1 \\ +\,1 \\ \hline 1\;0 \end{array}$$

a	b	s_1	s_0
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Addition of Binary Numbers

$$\begin{array}{r} a \\ +\,b \\ \hline s_1\,s_0 \end{array} \qquad \begin{array}{r} 0 \\ +\,0 \\ \hline 0\,0 \end{array} \qquad \begin{array}{r} 0 \\ +\,1 \\ \hline 0\,1 \end{array} \qquad \begin{array}{r} 1 \\ +\,0 \\ \hline 0\,1 \end{array} \qquad \begin{array}{r} 1 \\ +\,1 \\ \hline 1\,0 \end{array}$$

a	b	s_1	s_0
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Addition of Binary Numbers

$$\begin{array}{r} a \\ +\,b \\ \hline s_1\, s_0 \end{array} \qquad \begin{array}{r} 0 \\ +\,0 \\ \hline 0\,0 \end{array} \quad \begin{array}{r} 0 \\ +\,1 \\ \hline 0\,1 \end{array} \quad \begin{array}{r} 1 \\ +\,0 \\ \hline 0\,1 \end{array} \quad \begin{array}{r} 1 \\ +\,1 \\ \hline 1\,0 \end{array}$$

a	b	s_1	s_0
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Addition of Binary Numbers

$$\begin{array}{r} a \\ +\,b \\ \hline s_1\,s_0 \end{array} \qquad \begin{array}{r} 0 \\ +\,0 \\ \hline 0\;0 \end{array} \quad \begin{array}{r} 0 \\ +\,1 \\ \hline 0\;1 \end{array} \quad \begin{array}{r} 1 \\ +\,0 \\ \hline 0\;1 \end{array} \quad \begin{array}{r} 1 \\ +\,1 \\ \hline 1\;0 \end{array}$$

a	b	s_1	s_0
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Addition of Binary Numbers

$$\begin{array}{r} a \\ +\,b \\ \hline s_1\ s_0 \end{array} \qquad \begin{array}{r} 0 \\ +\,0 \\ \hline 0\ 0 \end{array} \qquad \begin{array}{r} 0 \\ +\,1 \\ \hline 0\ 1 \end{array} \qquad \begin{array}{r} 1 \\ +\,0 \\ \hline 0\ 1 \end{array} \qquad \begin{array}{r} 1 \\ +\,1 \\ \hline 1\ 0 \end{array}$$

a	b	s_1	s_0
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Addition of Binary Numbers

$$\begin{array}{r} a \\ +\,b \\ \hline s_1\,s_0 \end{array} \qquad \begin{array}{r} 0 \\ +\,0 \\ \hline 0\,0 \end{array} \qquad \begin{array}{r} 0 \\ +\,1 \\ \hline 0\,1 \end{array} \qquad \begin{array}{r} 1 \\ +\,0 \\ \hline 0\,1 \end{array} \qquad \begin{array}{r} 1 \\ +\,1 \\ \hline 1\,0 \end{array}$$

a	b	s_1	s_0
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Addition of Binary Numbers

$$\begin{array}{r} a \\ +\,b \\ \hline s_1\, s_0 \end{array} \qquad \begin{array}{r} 0 \\ +\,0 \\ \hline 0\;0 \end{array} \qquad \begin{array}{r} 0 \\ +\,1 \\ \hline 0\;1 \end{array} \qquad \begin{array}{r} 1 \\ +\,0 \\ \hline 0\;1 \end{array} \qquad \begin{array}{r} 1 \\ +\,1 \\ \hline 1\;0 \end{array}$$

a	b	s_1	s_0
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Addition of Binary Numbers

a	b	s_1	s_0
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Addition of Binary Numbers

?

a	b	s_1	s_0
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Addition of Binary Numbers

AND

a	b	s_1	s_0
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Addition of Binary Numbers

a	b	s_1	s_0
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Addition of Binary Numbers

?

a	b	s_1	s_0
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Addition of Binary Numbers

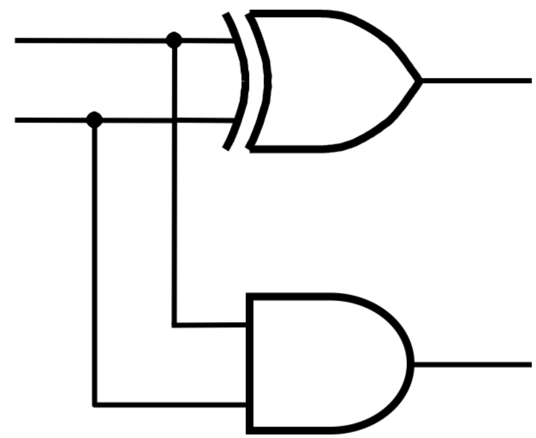
XOR

a	b	s_1	s_0
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Addition of Binary Numbers

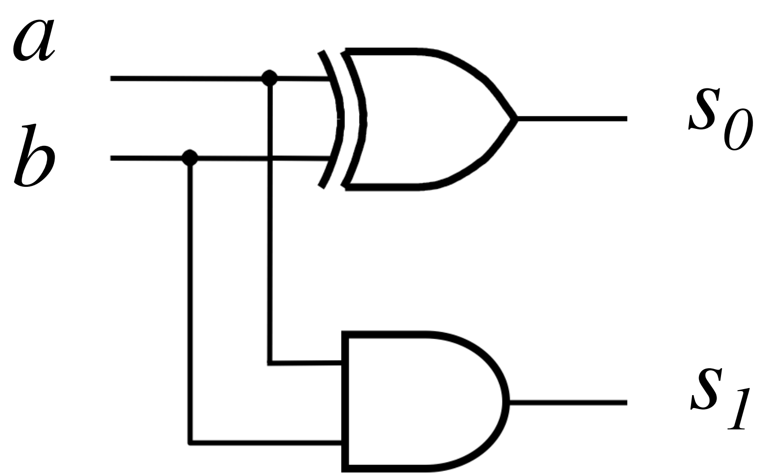
a	b	s_1	s_0
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Addition of Binary Numbers



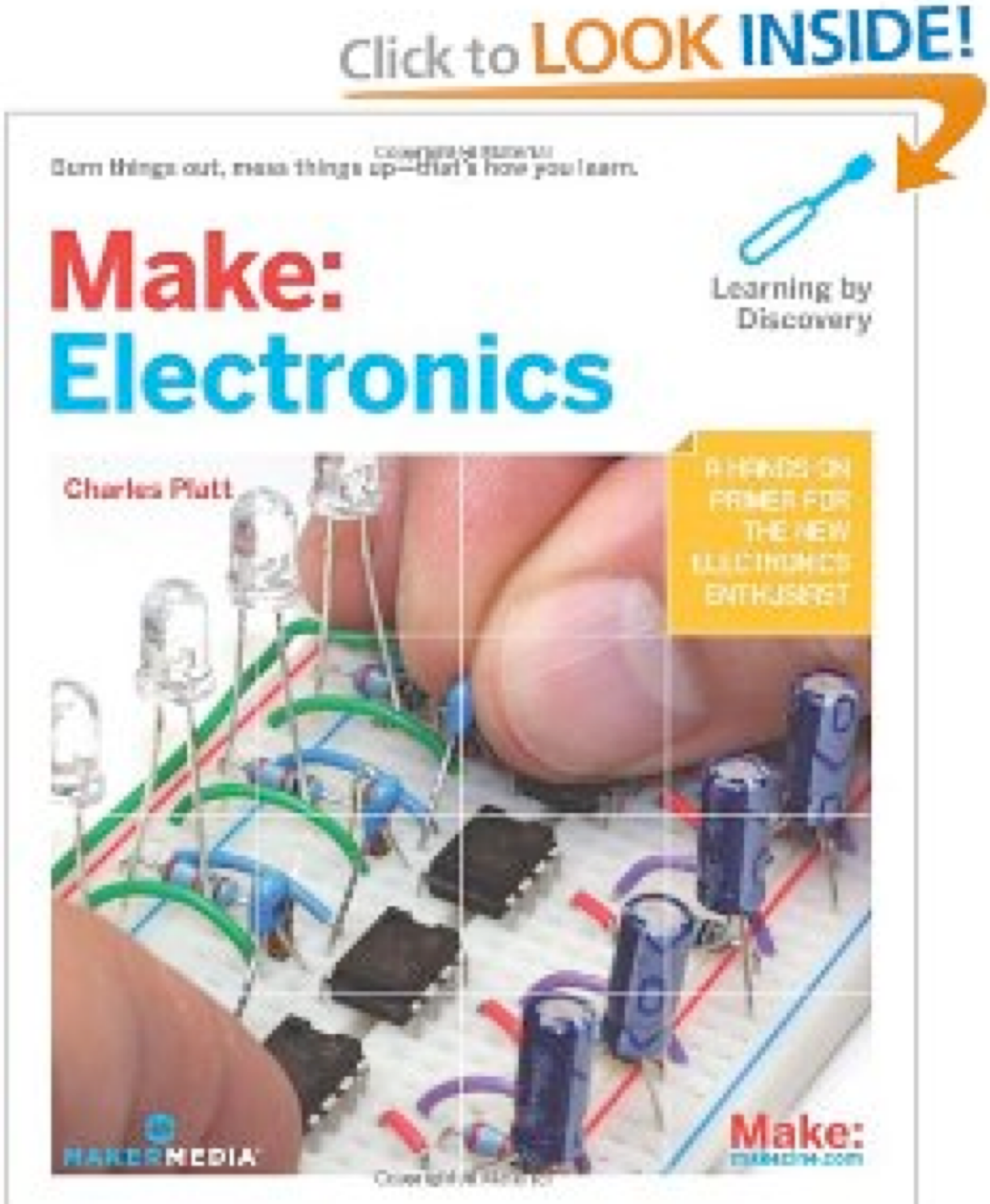
a	b	s_1	s_0
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

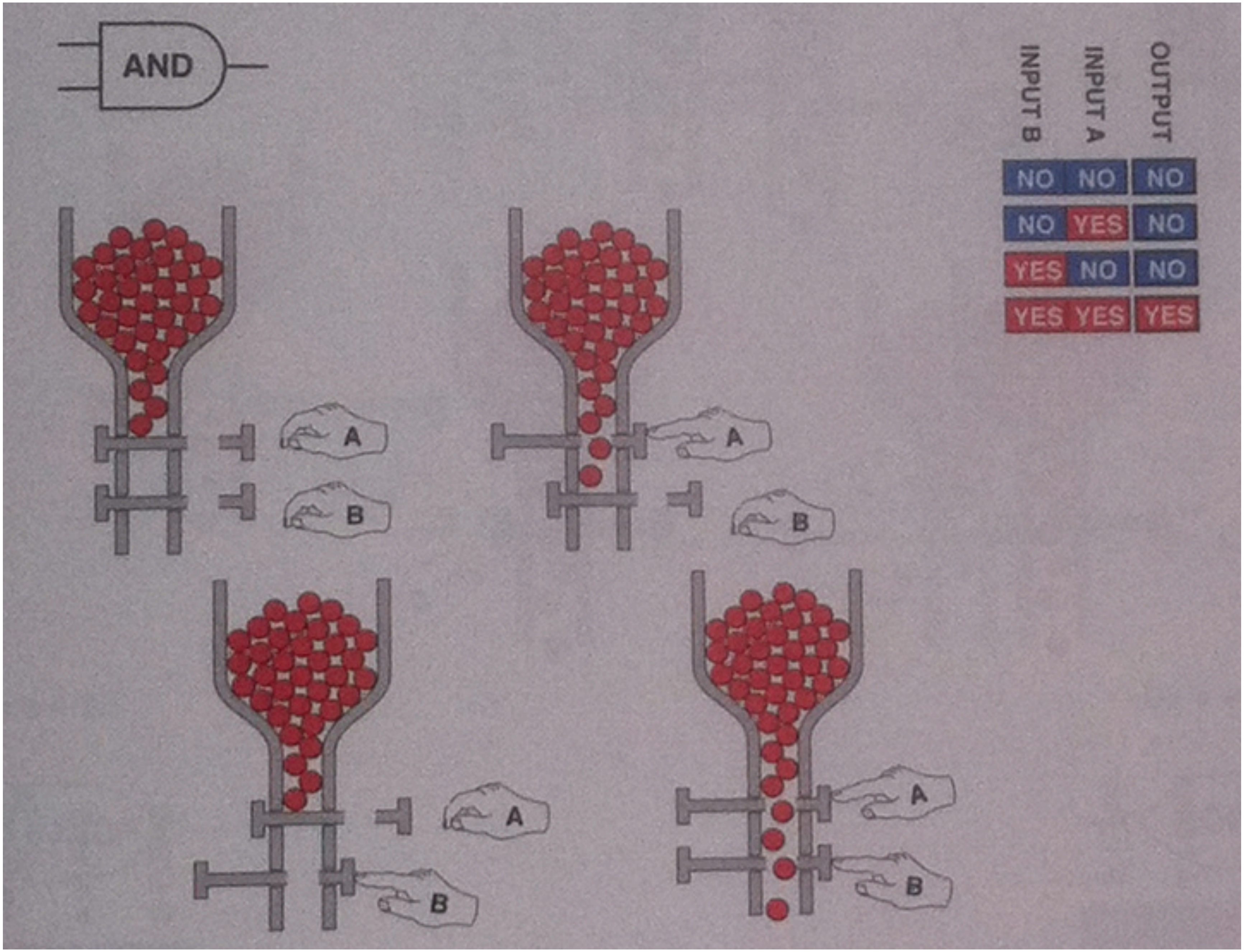
Addition of Binary Numbers



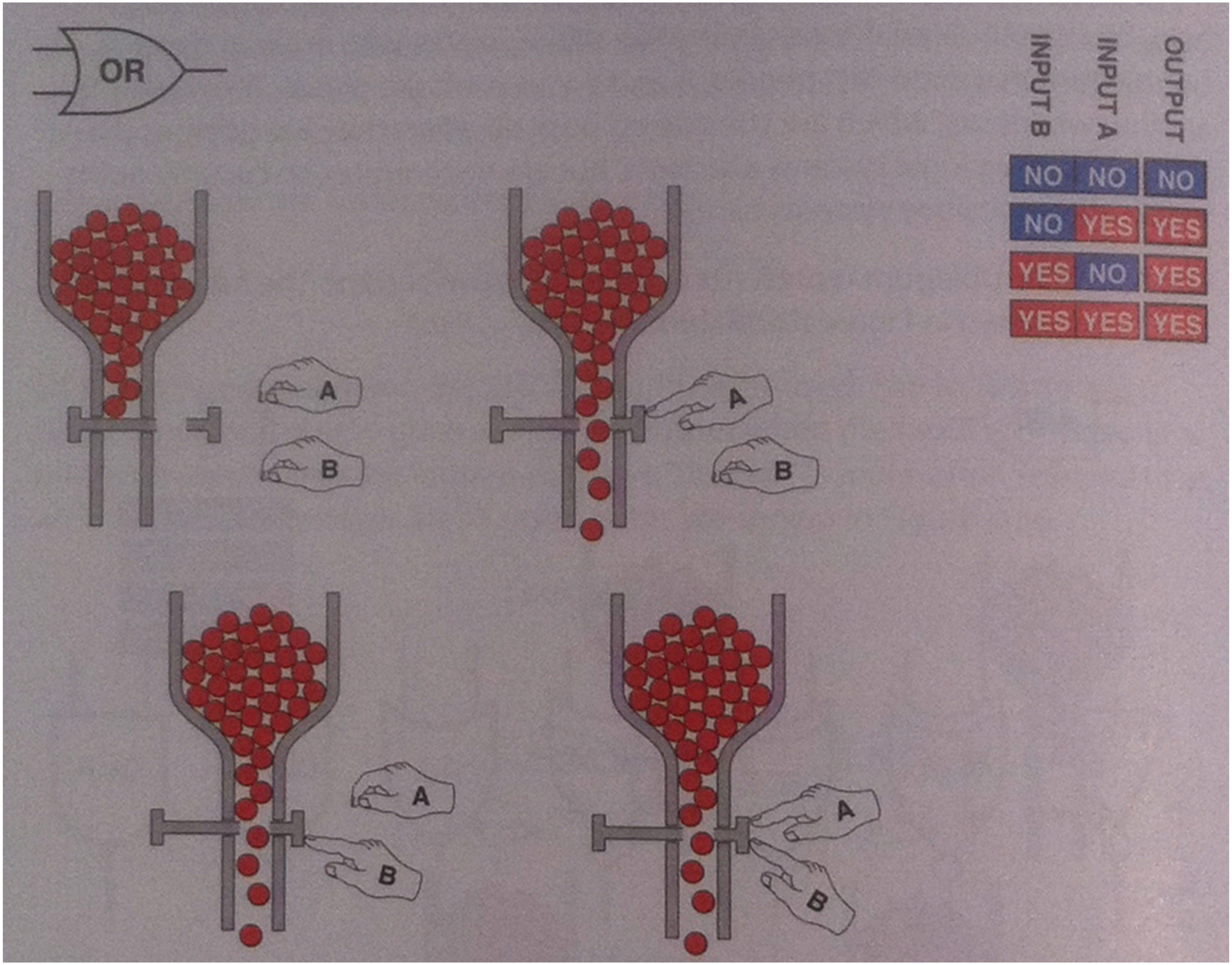
a	b	s_1	s_0
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

The following examples came from this book

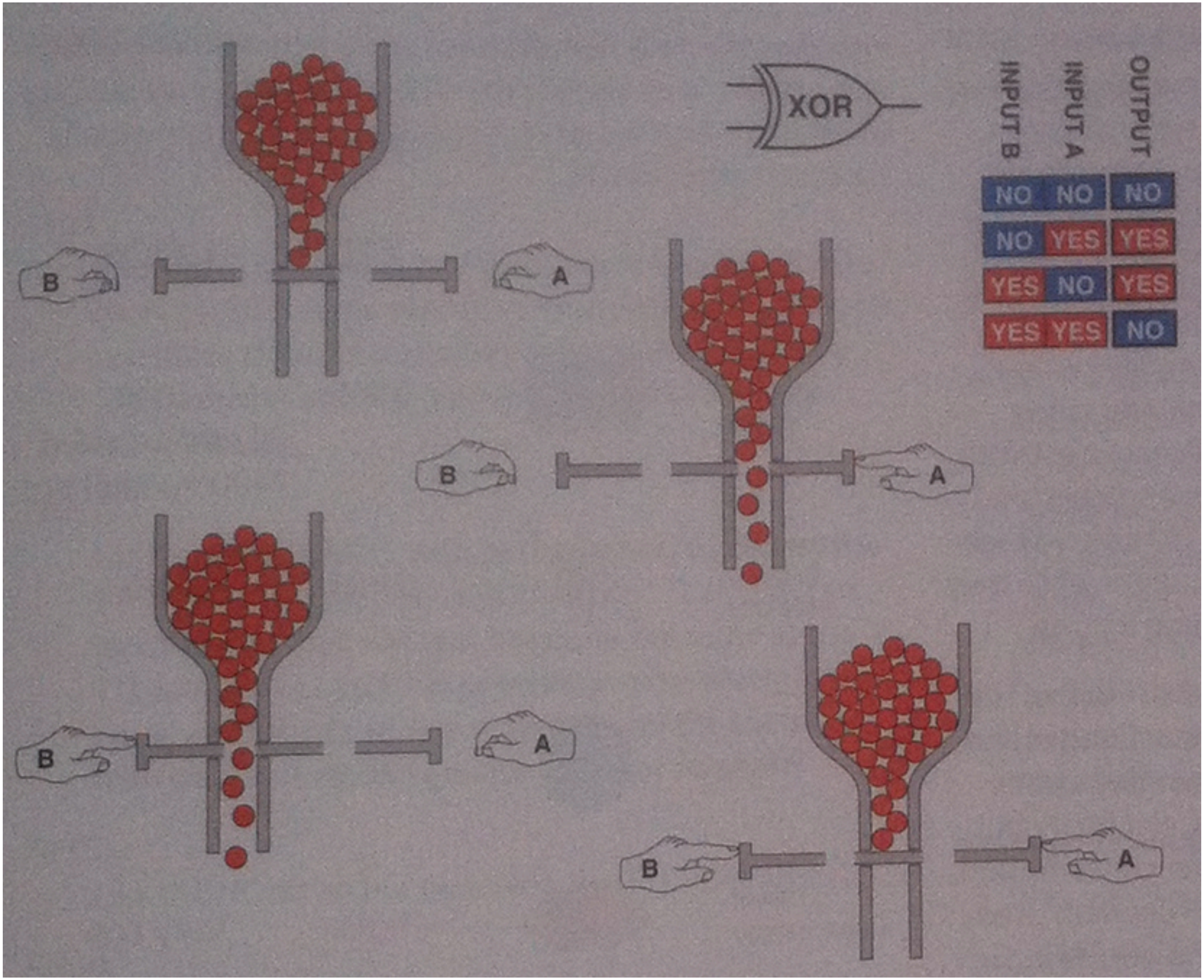



AND
INPUT B
INPUT A
OUTPUT
NO NO NO
NO YES NO
YES NO NO
YES YES YES
A
B
A
B
A
B
A
B

[Platt 2009]


OR
INPUT B
INPUT A
OUTPUT
NO NO NO
NO YES YES
YES NO YES
YES YES YES
A
B

[Platt 2009]


XOR
INPUT B
INPUT A
OUTPUT
NO NO NO
NO YES YES
YES NO YES
YES YES NO
B
A

[Platt 2009]

Questions?

THE END