Sample Solutions

CprE 281: Digital Logic
Midterm 2: Friday Oct. 26, 2018

Student Name: ______________________ **Student ID Number:** ____________

Lab Section: (circle one)	**Mon 12-3(P)**	**Tue 11-2(U)**	**Wed 8-11(J)**	**Thur 11-2(Q)**	**Fri 11-2(G)**
		Tue 2-5(M)	**Wed 11-2(W)**	**Thur 11-2(V)**	
		Tue 2-5(Z)	**Wed 6-9(T)**	**Thur 2-5(L)**	
				Thur 5-8(K)	

1. True/False Questions (10 x 1p each = 10p)

(a) I forgot to write down my name or student ID number or lab section. TRUE / **(FALSE)**

(b) The total delay through a half-adder is 2 gate delays. TRUE / **(FALSE)**

(c) The two inputs of a gated D-latch are called S and R. TRUE / **(FALSE)**

(d) A register file can have more than one read port. **(TRUE)** / FALSE

(e) A JK flip-flop reduces to a T flip-flop when J=K. **(TRUE)** / FALSE

(f) The undesirable state of a basic latch with NAND gates is when $Q = \overline{Q} = 1$. **(TRUE)** / FALSE

(g) A priority encoder has one-hot encoded inputs. TRUE / **(FALSE)**

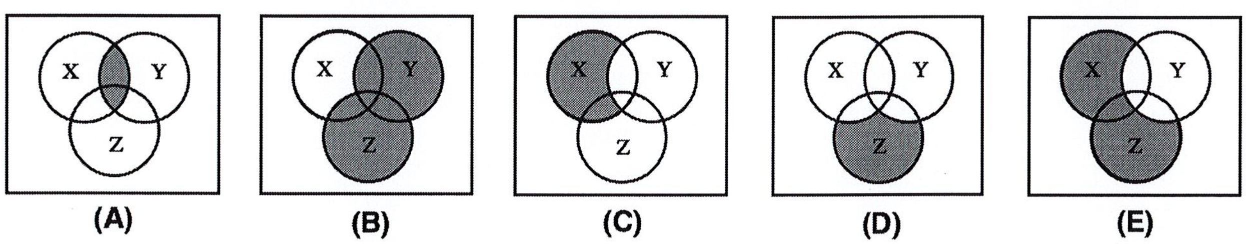
(h) In 32-bit IEEE 754 format, 11000000011000…0 is equal to -3. **(TRUE)** / FALSE

(i) A T flip-flop and an XOR gate can be used to implement a D flip-flop. **(TRUE)** / FALSE

(j) In binary, Yoda is more than 1000000000 years old. **(TRUE)** / FALSE

2. Venn Diagrams (5 x 1p each = 5p)

Write the <u>Boolean expression</u> that corresponds to each Venn diagram below each figure.



(A) $X \cdot Y$

(B) $Y + Z$

(C) $X\overline{Y}$

(D) $\overline{X}\,\overline{Y}Z$ OR $(\overline{X+Y})Z$

(E) $(X+Z)\overline{Y}$

3. **Minimization (3 x 4p each = 12p)**

(a) Draw the truth table for the function f(a, b, c, d) = Σ m (1, 2, 4, 6, 7, 14, 15) + D(5, 10)

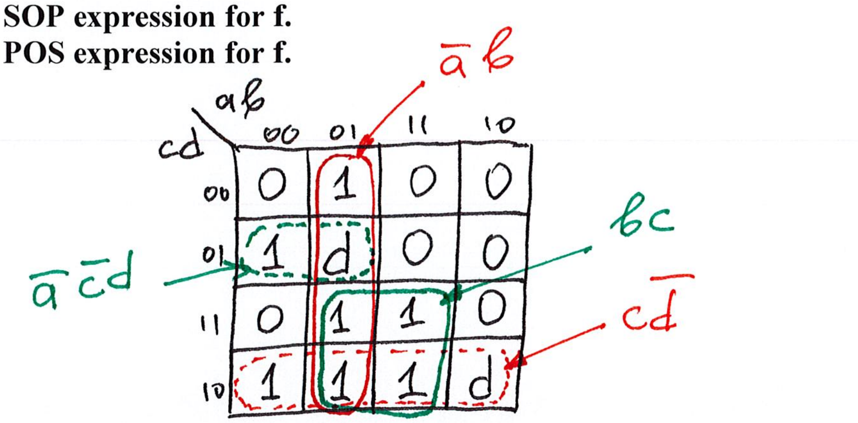
(b) Use a K-Map to derive the minimum cost SOP expression for f.

(c) Use a K-Map to derive the minimum cost POS expression for f.

(a)

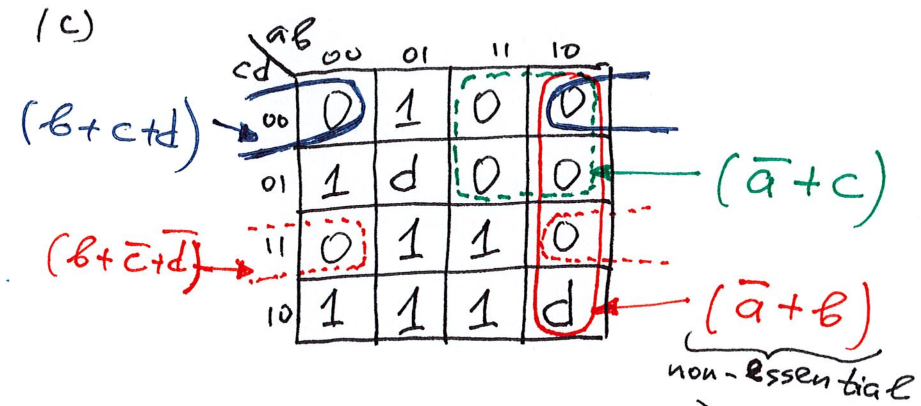
#	a	b	c	d	f
0	0	0	0	0	0
1	0	0	0	1	1
2	0	0	1	0	1
3	0	0	1	1	0
4	0	1	0	0	1
5	0	1	0	1	d
6	0	1	1	0	1
7	0	1	1	1	1
8	1	0	0	0	0
9	1	0	0	1	0
10	1	0	1	0	d
11	1	0	1	1	0
12	1	1	0	0	0
13	1	1	0	1	0
14	1	1	1	0	1
15	1	1	1	1	1

(b)



$$f = \bar{a}\bar{c}d + \bar{a}b + bc + c\bar{d}$$

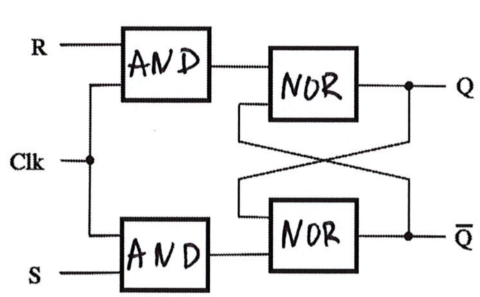
(c)



$$f = (b+c+d)\cdot(b+\bar{c}+\bar{d})\cdot(\bar{a}+c)\cdot\cancel{(\bar{a}+b)}$$

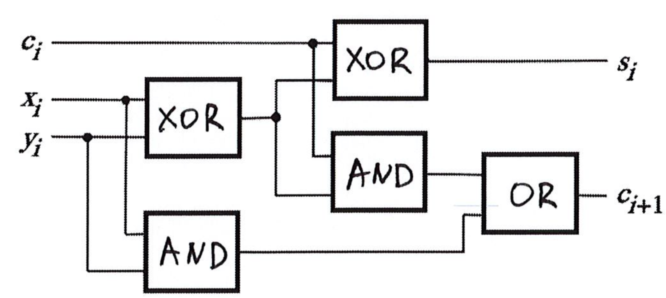
4. **Fill in the Blanks (2 x 4p = 8p).** **Given the inputs, outputs, and wires of a familiar circuit, fill in the names of the logic gates inside the square blocks. Also, write the <u>name</u> of each circuit.**

a)



Circuit name: Gated latch with NOR gates

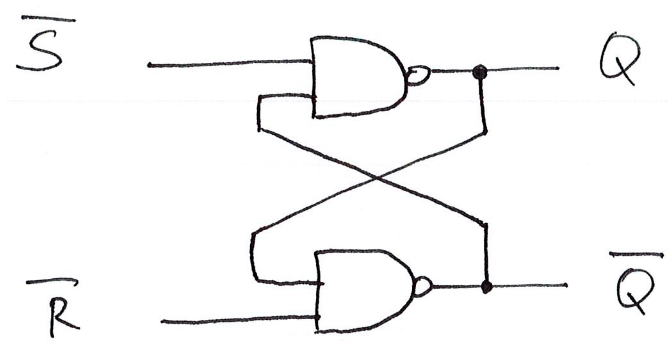
b)



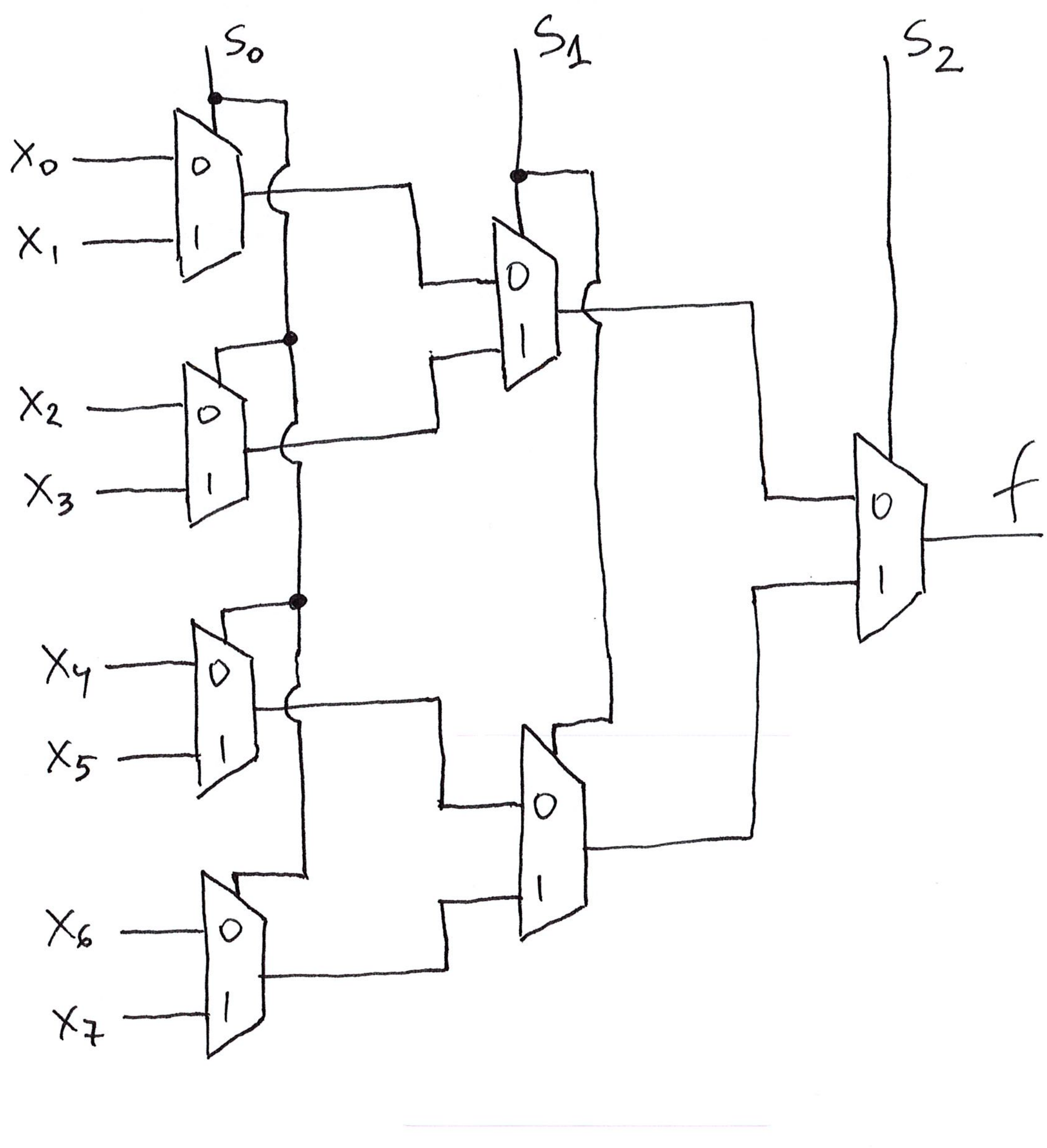
Circuit name: Full adder

5. **Circuits (5p + 10p = 15p).**

(a) Draw the wiring diagram for an $\overline{S}\,\overline{R}$ - Latch. Label all inputs, outputs, and pins.



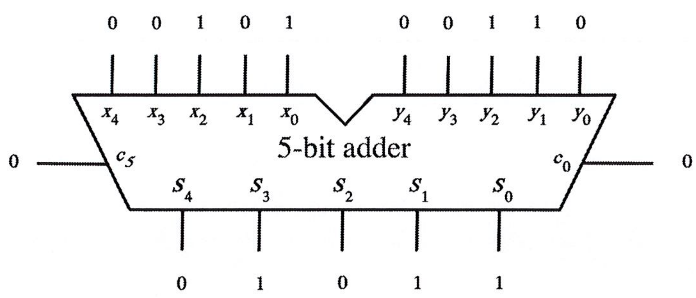
(b) Draw the circuit for an 8-to-1 multiplexer using <u>only</u> 2-to-1 multiplexers. Clearly label all inputs, outputs, and pins. Hint: think of a tree.



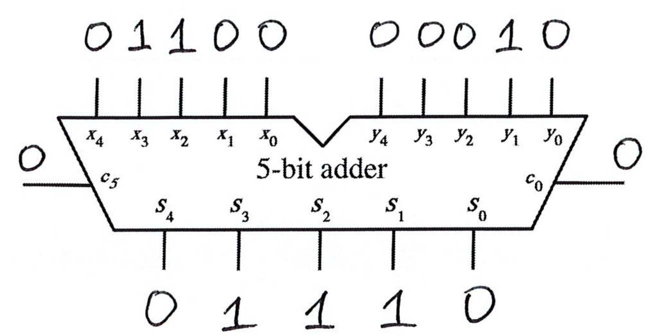
6. **Computations with Adders (5 x 3p each = 15p)**

In all problems below, the binary numbers are stored in <u>2's complement representation</u>. For each of the following, assign either a 0 or a 1 to each input and output of the 5-bit adder such that it computes the given expression. The problem in a) is already solved.

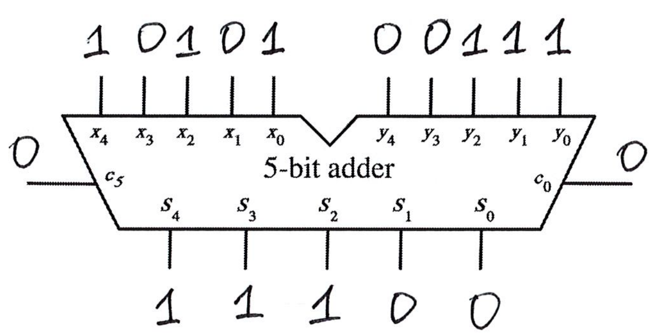
a) (+5) + (+6) = +11



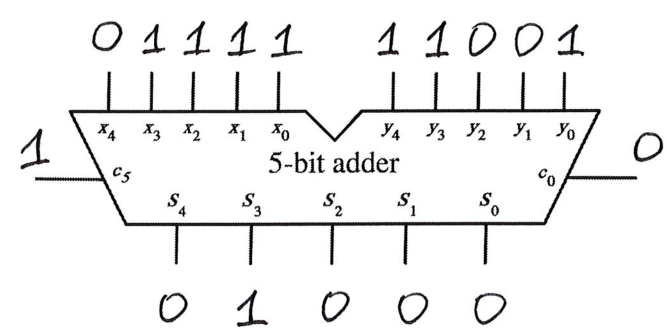
b) (+12) + (+2) = + 14



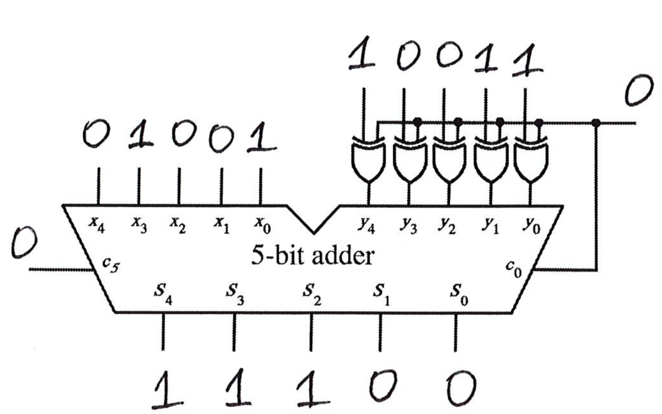
c) (-11) + (+7) = - 4



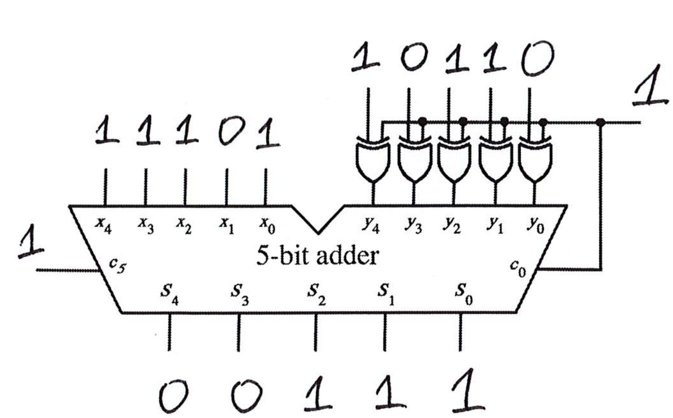
d) (+15) + (-7) = + 8



e) (+9) + (-13) = - 4



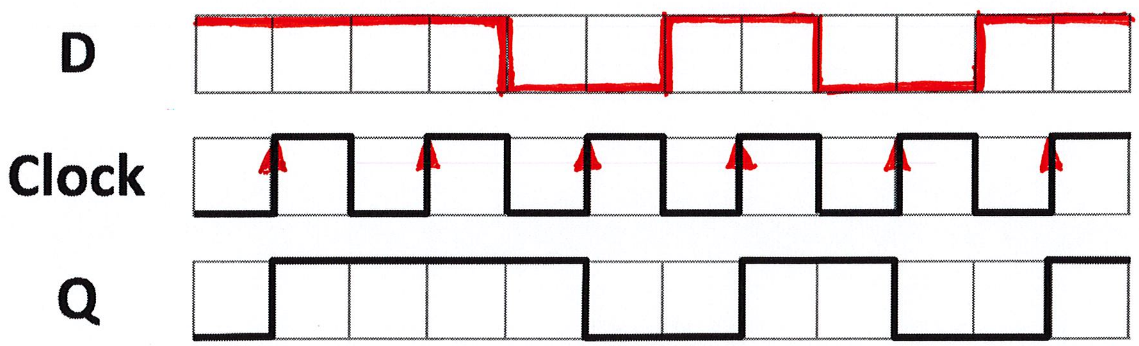
f) (-3) - (-10) = + 7



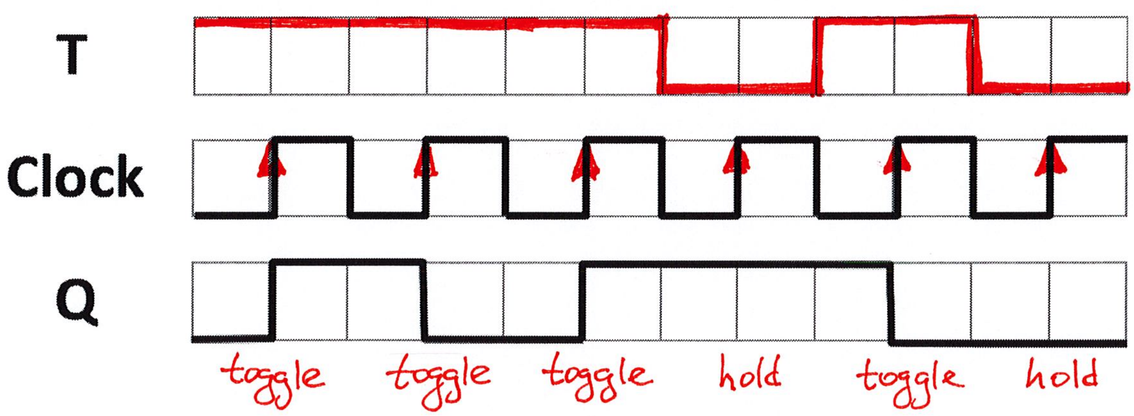
7. **Flip-Flops and Timing Diagrams (3 x 5p = 15p)**

Complete the timing diagram for the specified flip-flop such that the output Q will be as indicated. Assume that the input signal can change only on the <u>vertical lines.</u> Also, assume that the setup time t_{su} and the hold time t_h are <u>each</u> equal to the width of one square.

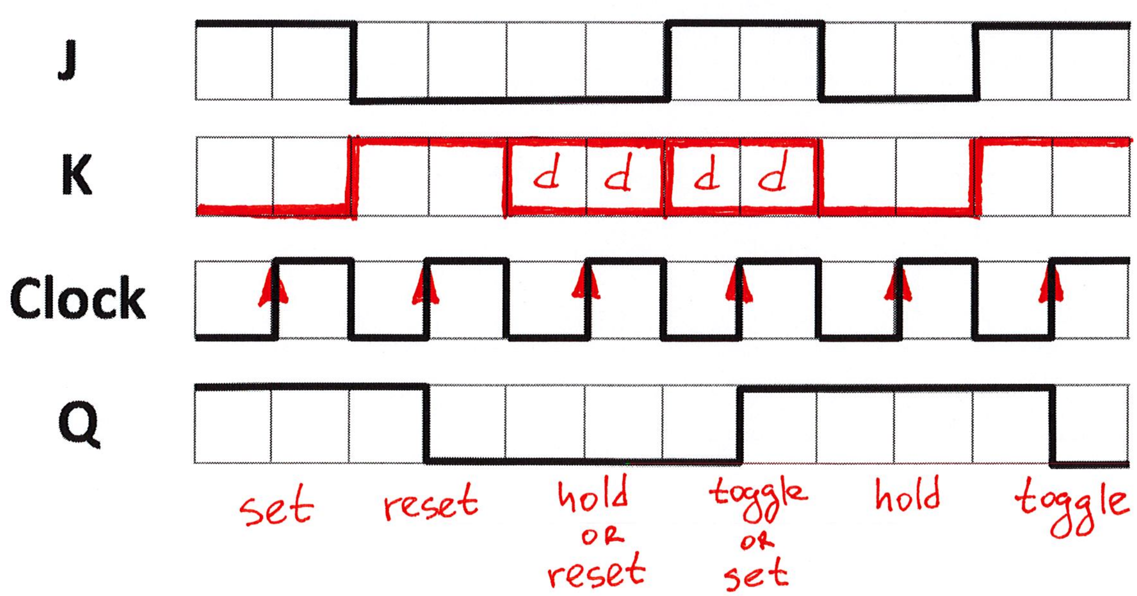
a) Complete the timing diagram for the D input to a <u>positive</u>-edge triggered D flip-flop.



b) Complete the timing diagram for the T input to a <u>positive</u>-edge triggered T flip-flop.



c) Complete the timing diagram for the K input to a <u>positive</u>-edge triggered JK flip-flop.



8. Multiplexers (3 x 5p each = 15p)

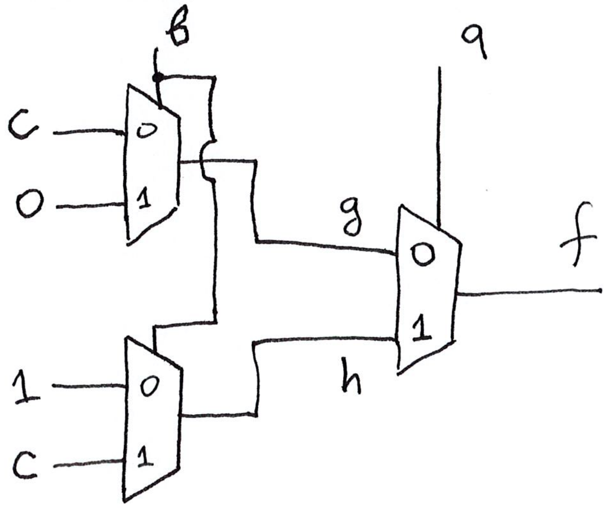
a) **Draw the truth table for the function** $f(a, b, c) = a\,c + a\,\overline{b} + \overline{b}\,c$.

a	b	c	ac	+ $a\overline{b}$	+ $\overline{b}c$	f	
0	0	0	0	0	0	0	g
0	0	1	0	0	1	1	g
0	1	0	0	0	0	0	g
0	1	1	0	0	0	0	g
1	0	0	0	1	0	1	h
1	0	1	1	1	1	1	h
1	1	0	0	0	0	0	h
1	1	1	1	0	0	1	h

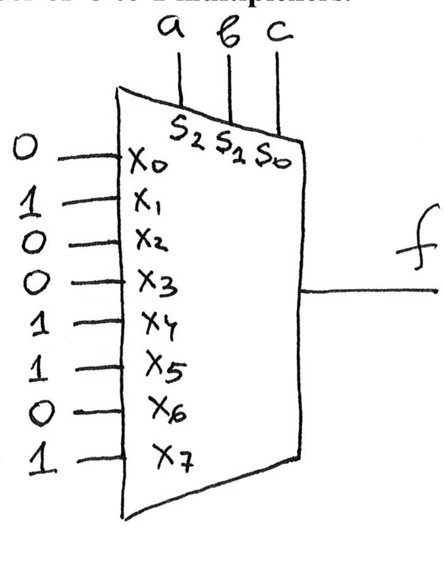
b) **Implement this function using a minimal number of 2-to-1 multiplexers. You must use only 2-to-1 multiplexers and no other logic gates. Assume that the signals a, b, and c are available only in their non-inverted form as well as the constants 0 and 1. Clearly label all inputs, outputs, and pins.**

b	c	g	
0	0	0	c
0	1	1	c
1	0	0	0
1	1	0	0

b	c	h	
0	0	1	1
0	1	1	1
1	0	0	c
1	1	1	c



c) **Implement this function using a minimal number of 8-to-1 multiplexers. Clearly label all inputs, outputs, and pins.**



Some of these problems have more than one solution.

9. Alternative Implementation (10p)

Implement the logic expression in each sub-problem in three different ways: 1) using a 2-to-1 multiplexer; 2) using NAND-NAND logic; and 3) using NOR-NOR logic. In this problem, you are <u>not allowed</u> to use any other logic gates. Assume that a and b are available in both their inverted and non-inverted form, along with the constants 0 and 1. If some implementation is not possible, then indicate that with words. <u>Label all inputs and outputs.</u>

a) Implement in three different ways: f(a,b) = a + b.

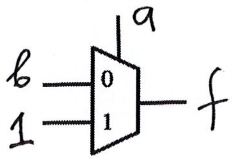
a	b	f	
0	0	0	} b
0	1	1	
1	0	1	} 1
1	1	1	

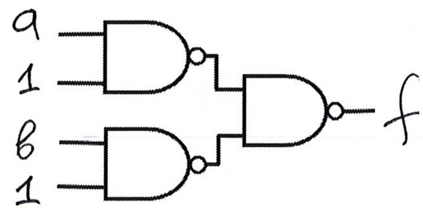
SOP

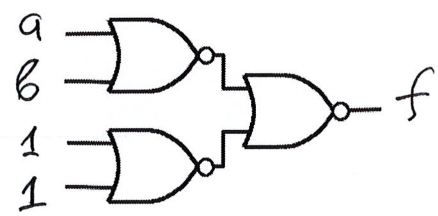
$f = a + b = a \cdot 1 + b \cdot 1$

POS

$f = (a + b)$
$= (a + b) \cdot (1 + 1)$







b) Implement in three different ways: f(a,b) = a $\bar{b}$.

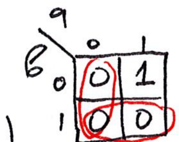
a	b	f	
0	0	0	} 0
0	1	0	
1	0	1	} $\bar{b}$
1	1	0	

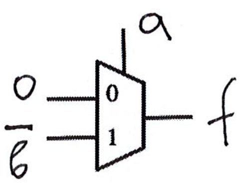
SOP

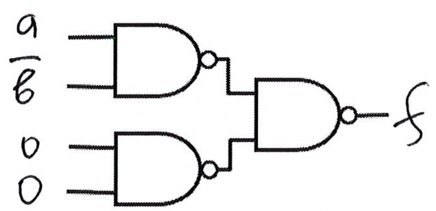
$f = a\bar{b} = a \cdot \bar{b} + 0 \cdot 0$

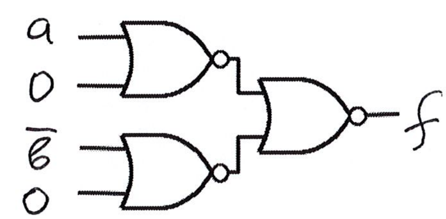
POS

$f = (a) \cdot (\bar{b})$
$= (a + 0) \cdot (\bar{b} + 0)$









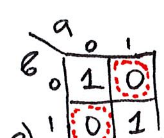
c) Implement in three different ways: f(a,b) = $\bar{a}\,\bar{b}$ + a b.

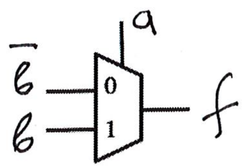
a	b	f	
0	0	1	} $\bar{b}$
0	1	0	
1	0	0	} b
1	1	1	

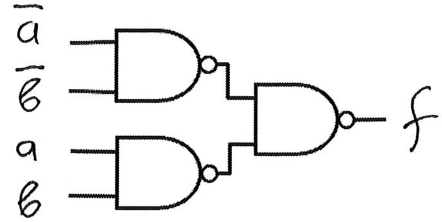
SOP

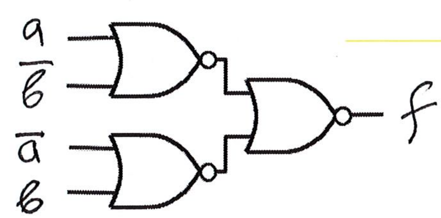
POS

$f = (a + \bar{b}) \cdot (\bar{a} + b)$



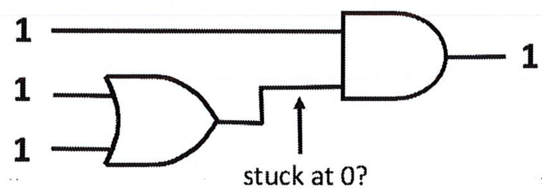




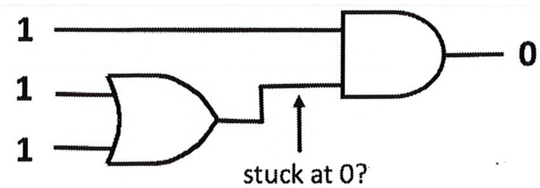


10. Faulty Circuits (3p + 3p + 4p = 10p)

The circuits below have a manufacturing defect such that one of their wires is broken and is permanently stuck to zero volts (ground). Your task is to find a set of input and output patterns that can be used to distinguish between a working circuit and a faulty circuit. The figure below gives an example in which the second input of the AND gate may be faulty.

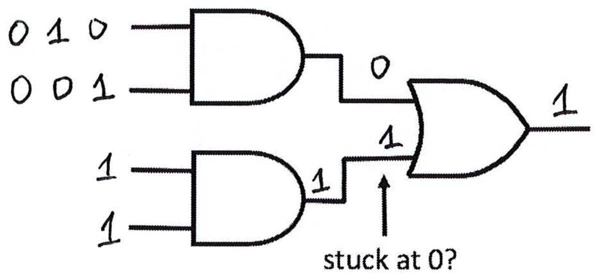


Normal Circuit



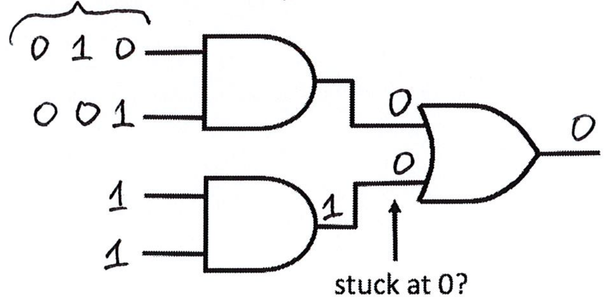
Faulty Circuit

(a)



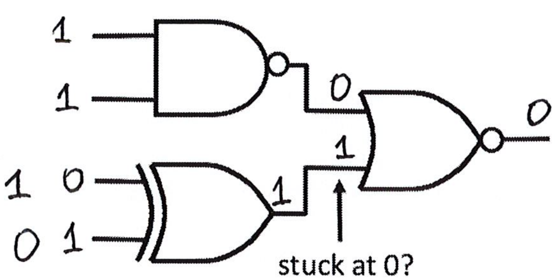
Normal Circuit

3 different solutions

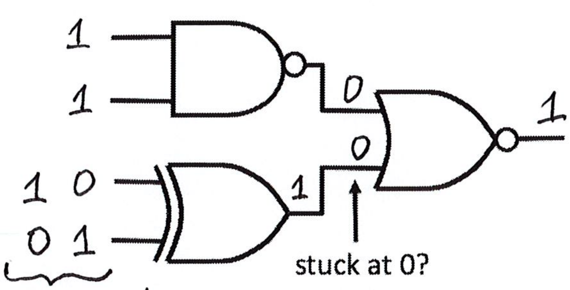


Faulty Circuit

(b)



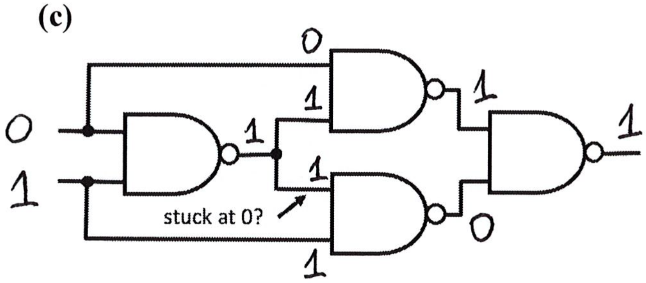
Normal Circuit



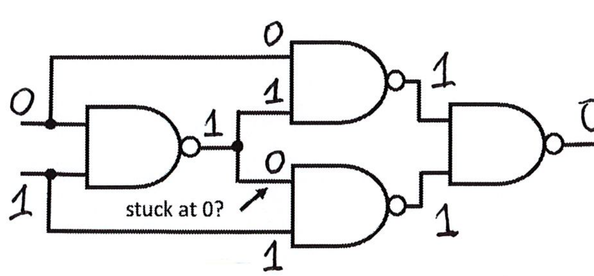
2 different solutions

Faulty Circuit

(c)



Normal Circuit



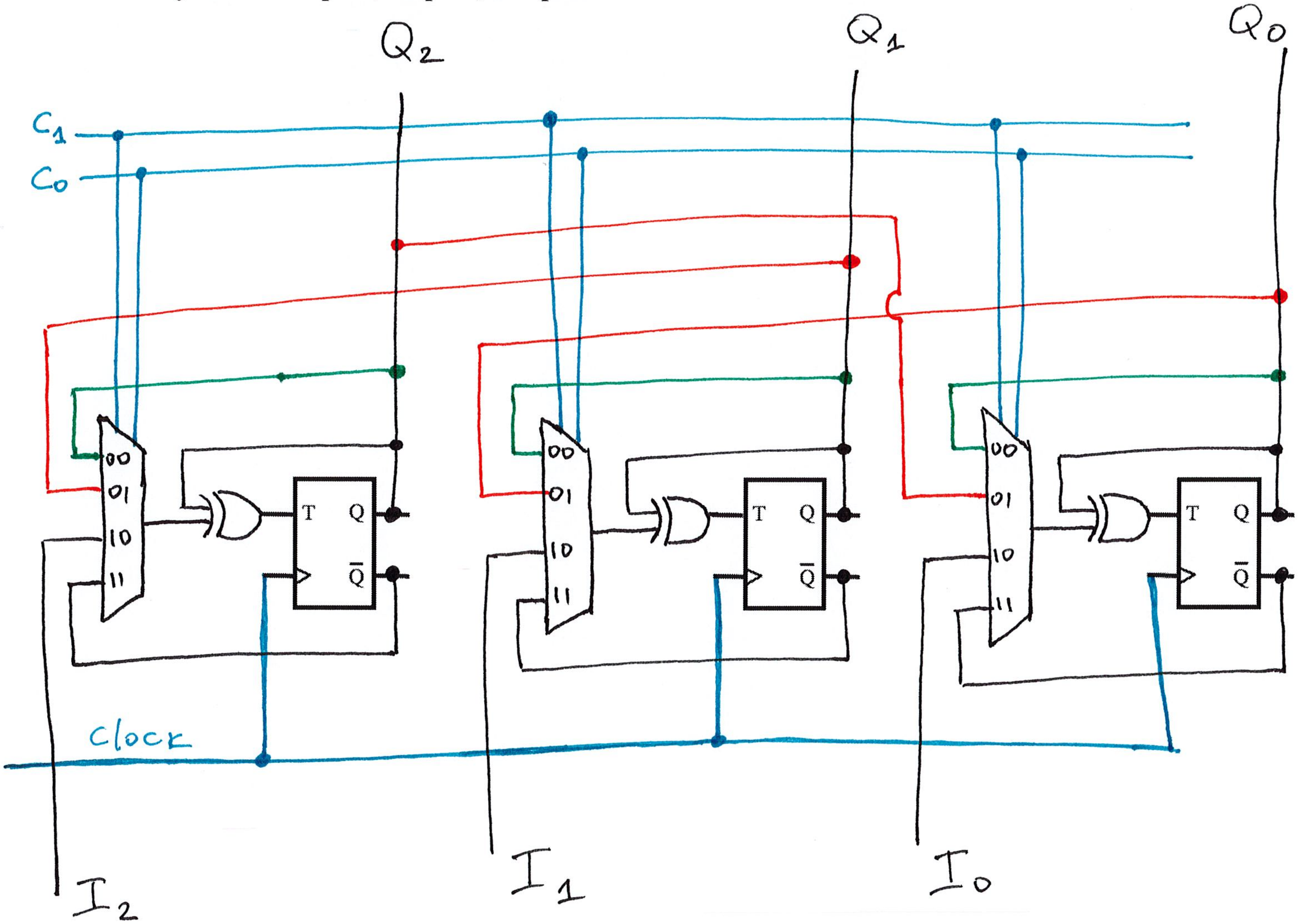
Faulty Circuit

11. **Register (15p)**

Complete the following circuit diagram by drawing wires and adding any other circuits or logic gates to implement a 3-bit register. The register has two control inputs (C_1 and C_0), three parallel input lines (I_2, I_1, and I_0), and three output lines (Q_2, Q_1, and Q_0). Depending on the values of C_1 and C_0, the register performs one of the following four operations:

C_1	C_0	Operation
0	0	Hold the current value (i.e., Q_2 Q_1 Q_0 remain unchanged)
0	1	Cyclic shift left (i.e., new Q_2=Q_1, new Q_1=Q_0, new Q_0=Q_2)
1	0	Load new data (i.e., new Q_2=I_2, new Q_1=I_1, new Q_0=I_0)
1	1	Invert all bits (i.e., new $Q_2=\overline{Q_2}$, new $Q_1=\overline{Q_1}$, new $Q_0=\overline{Q_0}$)

Clearly label all inputs, outputs, and pins.



Note that these are T flip-flops!
Also, note that XOR + T flip-flop => D flip-flop.

Question	Max	Score
1. True/False	10	
2. Venn Diagrams	5	
3. Minimization with K-Maps	12	
4. Fill in the Blanks	8	
5. Circuits	15	
6. Computations with Adders	15	
7. Flip-Flops	15	
8. Multiplexers	15	
9. Alternative Implementation	10	
10. Faulty Circuits	10	
11. Register	15	
TOTAL:	130	