CprE 281: Digital Logic
Midterm 2: Friday Oct. 26, 2018

Student Name: _____ **Student ID Number:** _____

Lab Section:	**Mon 12-3(P)**	**Tue 11-2(U)**	**Wed 8-11(J)**	**Thur 11-2(Q)**	**Fri 11-2(G)**
(circle one)		**Tue 2-5(M)**	**Wed 11-2(W)**	**Thur 11-2(V)**	
		Tue 2-5(Z)	**Wed 6-9(T)**	**Thur 2-5(L)**	
				Thur 5-8(K)	

1. True/False Questions (10 x 1p each = 10p)

(a) I forgot to write down my name or student ID number or lab section. TRUE / FALSE

(b) The total delay through a half-adder is 2 gate delays. TRUE / FALSE

(c) The two inputs of a gated D-latch are called S and R. TRUE / FALSE

(d) A register file can have more than one read port. TRUE / FALSE

(e) A JK flip-flop reduces to a T flip-flop when J=K. TRUE / FALSE

(f) The undesirable state of a basic latch with NAND gates is when $Q = \overline{Q} = 1$. TRUE / FALSE

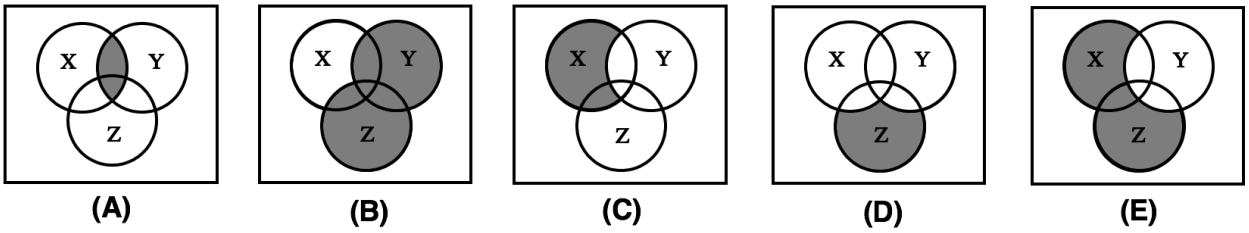
(g) A priority encoder has one-hot encoded inputs. TRUE / FALSE

(h) In 32-bit IEEE 754 format, 11000000011000…0 is equal to -3. TRUE / FALSE

(i) A T flip-flop and an XOR gate can be used to implement a D flip-flop. TRUE / FALSE

(j) In binary, Yoda is more than 1000000000 years old. TRUE / FALSE

2. Venn Diagrams (5 x 1p each = 5p)
Write the <u>Boolean expression</u> that corresponds to each Venn diagram below each figure.



3. Minimization (3 x 4p each = 12p)

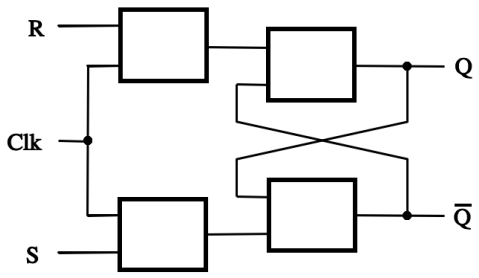
(a) Draw the truth table for the function f(a, b, c, d) = Σ m (1, 2, 4, 6, 7, 14, 15) + D(5, 10)

(b) Use a K-Map to derive the minimum cost SOP expression for f.

(c) Use a K-Map to derive the minimum cost POS expression for f.

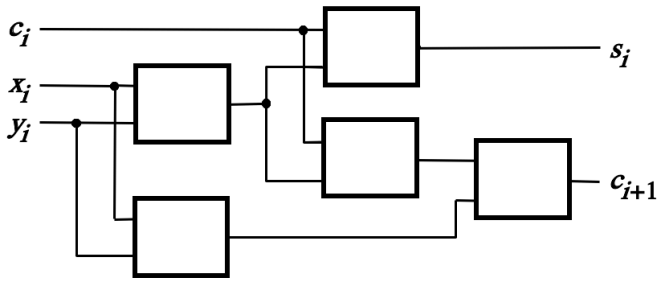
4. Fill in the Blanks (2 x 4p = 8p). Given the inputs, outputs, and wires of a familiar circuit, fill in the names of the logic gates inside the square blocks. Also, write the <u>name</u> of each circuit.

a)



Circuit name:

b)



Circuit name:

5. Circuits (5p + 10p = 15p).

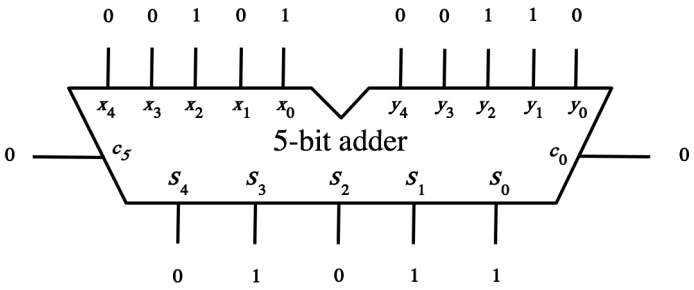
(a) Draw the wiring diagram for an $\overline{S}\,\overline{R}$ - Latch. Label all inputs, outputs, and pins.

(b) Draw the circuit for an 8-to-1 multiplexer using only 2-to-1 multiplexers. Clearly label all inputs, outputs, and pins. Hint: think of a tree.

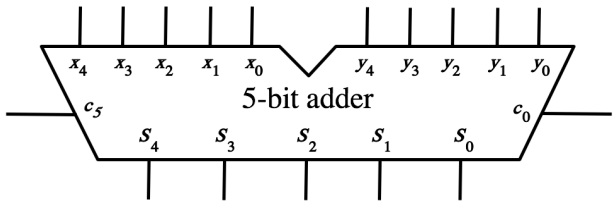
6. Computations with Adders (5 x 3p each = 15p)

In all problems below, the binary numbers are stored in <u>2's complement representation</u>. For each of the following, assign either a 0 or a 1 to each input and output of the 5-bit adder such that it computes the given expression. The problem in a) is already solved.

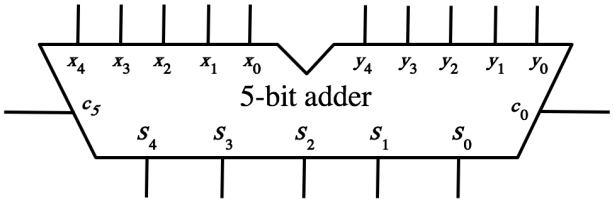
a) (+5) + (+6) = +11



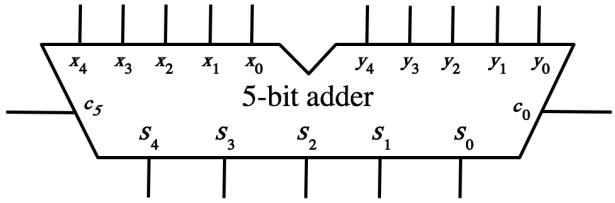
b) (+12) + (+2) =



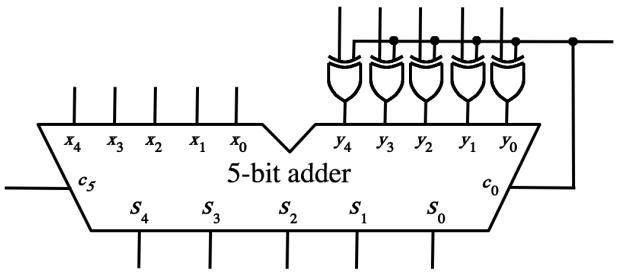
c) (-11) + (+7) =



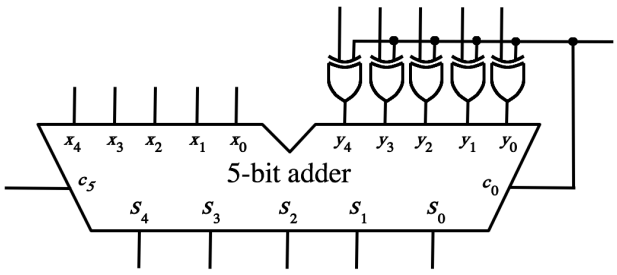
d) (+15) + (-7) =



e) (+9) + (-13) =



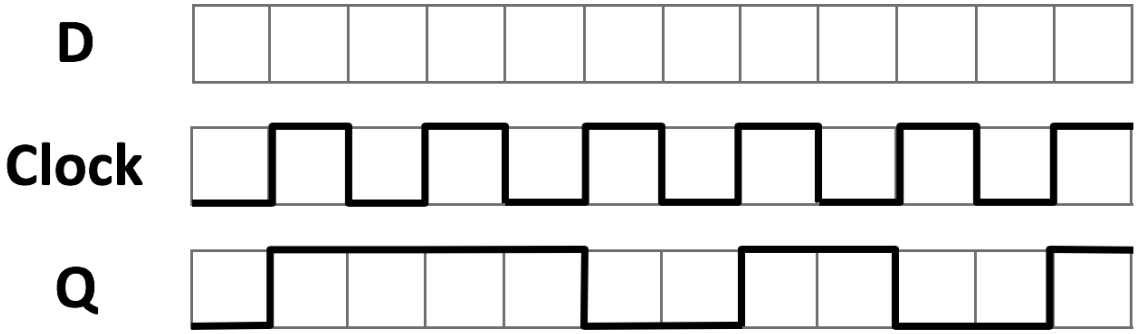
f) (-3) - (-10) =



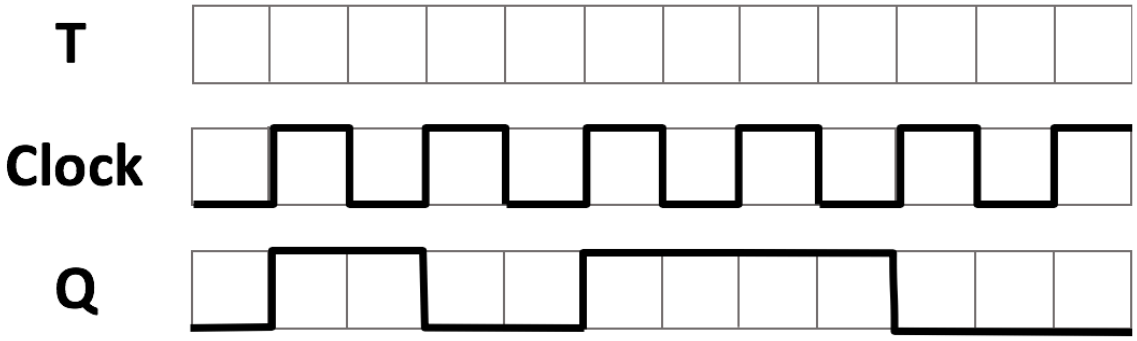
7. Flip-Flops and Timing Diagrams (3 x 5p = 15p)

Complete the timing diagram for the specified flip-flop such that the output Q will be as indicated. Assume that the input signal can change only on the vertical lines. Also, assume that the setup time t_{su} and the hold time t_h are each equal to the width of one square.

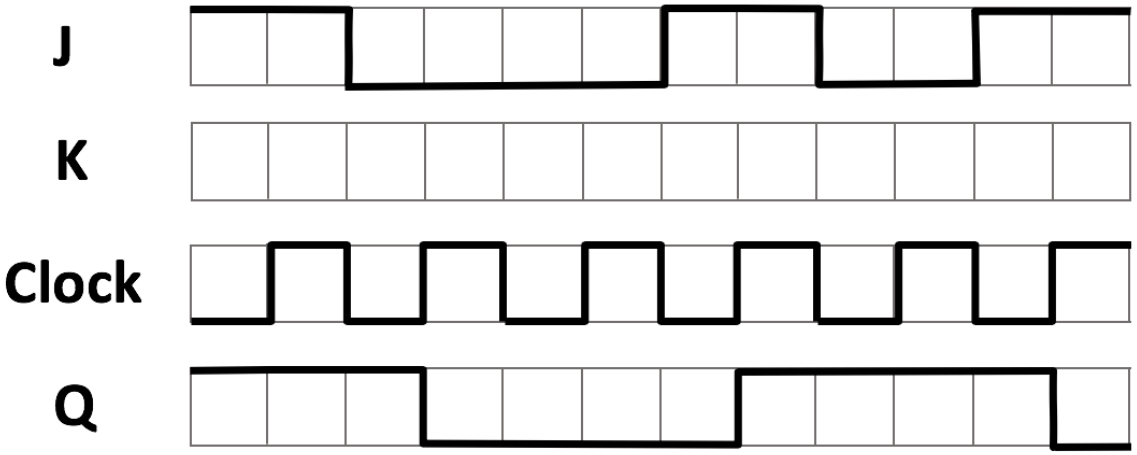
a) Complete the timing diagram for the D input to a positive-edge triggered D flip-flop.



b) Complete the timing diagram for the T input to a positive-edge triggered T flip-flop.



c) Complete the timing diagram for the K input to a positive-edge triggered JK flip-flop.



8. Multiplexers (3 x 5p each = 15p)

a) **Draw the truth table for the function** $f(a, b, c) = a\,c + a\,\overline{b} + \overline{b}\,c$.

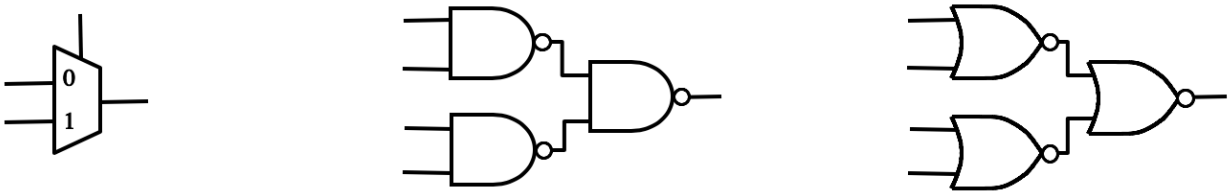
b) **Implement this function using a <u>minimal</u> number of 2-to-1 multiplexers. You must use <u>only</u> 2-to-1 multiplexers and <u>no other logic gates</u>. Assume that the signals a, b, and c are available <u>only</u> in their non-inverted form as well as the constants 0 and 1. Clearly label all inputs, outputs, and pins.**

c) **Implement this function using a <u>minimal</u> number of 8-to-1 multiplexers. Clearly label all inputs, outputs, and pins.**

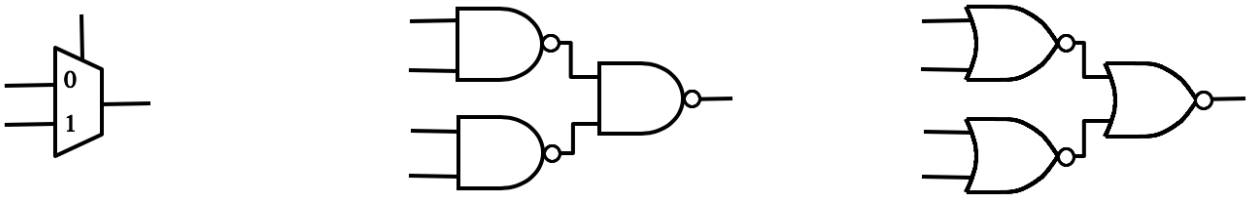
9. Alternative Implementation (10p)

Implement the logic expression in each sub-problem in three different ways: 1) using a 2-to-1 multiplexer; 2) using NAND-NAND logic; and 3) using NOR-NOR logic. In this problem, you are <u>not allowed</u> to use any other logic gates. Assume that a and b are available in both their inverted and non-inverted form, along with the constants 0 and 1. If some implementation is not possible, then indicate that with words. <u>Label all inputs and outputs.</u>

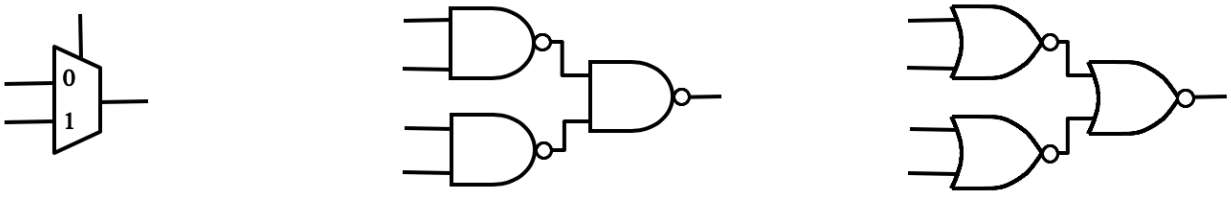
a) Implement in three different ways: f(a,b) = a + b.



b) Implement in three different ways: f(a,b) = a $\overline{b}$.

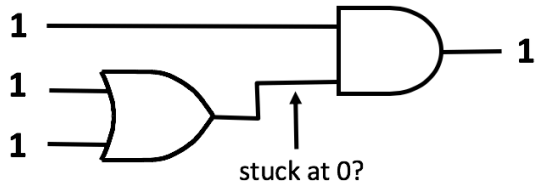


c) Implement in three different ways: f(a,b) = $\overline{a}$ $\overline{b}$ + a b.

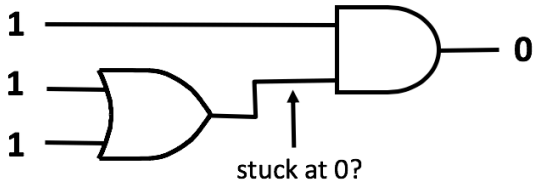


10. Faulty Circuits (3p + 3p + 4p = 10p)

The circuits below have a manufacturing defect such that one of their wires is broken and is permanently stuck to zero volts (ground). Your task is to find a set of input and output patterns that can be used to distinguish between a working circuit and a faulty circuit. The figure below gives an example in which the second input of the AND gate may be faulty.

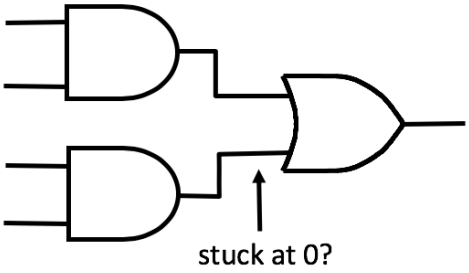


Normal Circuit

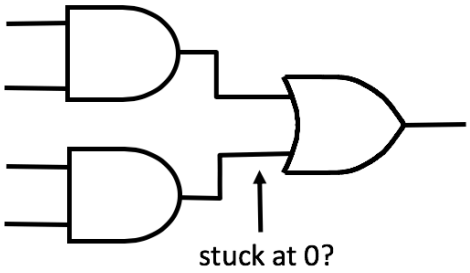


Faulty Circuit

(a)

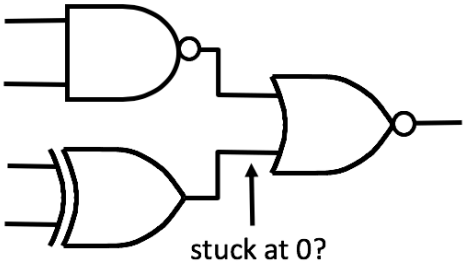


Normal Circuit

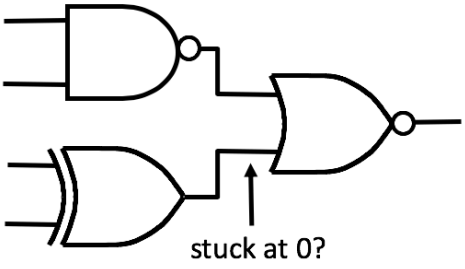


Faulty Circuit

(b)

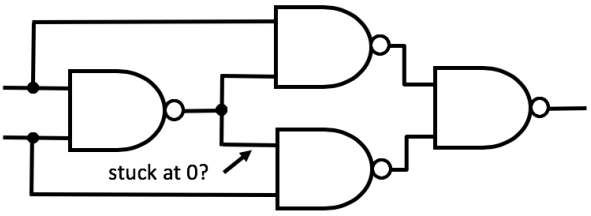


Normal Circuit

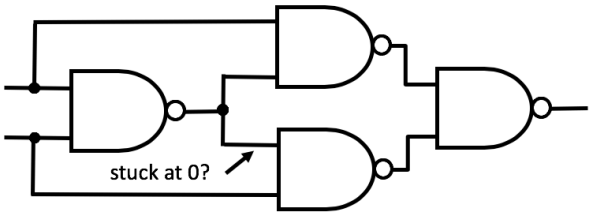


Faulty Circuit

(c)



Normal Circuit



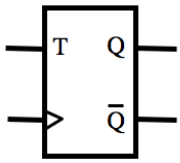
Faulty Circuit

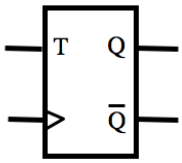
11. Register (15p)

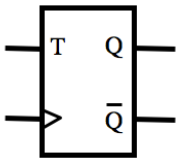
Complete the following circuit diagram by drawing wires and adding any other circuits or logic gates to implement a 3-bit register. The register has two control inputs (C_1 and C_0), three parallel input lines (I_2, I_1, and I_0), and three output lines (Q_2, Q_1, and Q_0). Depending on the values of C_1 and C_0, the register performs one of the following four operations:

C_1	C_0	Operation
0	0	Hold the current value (i.e., Q_2 Q_1 Q_0 remain unchanged)
0	1	Cyclic shift left (i.e., new Q_2=Q_1, new Q_1=Q_0, new Q_0=Q_2)
1	0	Load new data (i.e., new Q_2=I_2, new Q_1=I_1, new Q_0=I_0)
1	1	Invert all bits (i.e., new Q_2=$\overline{Q_2}$, new Q_1=$\overline{Q_1}$, new Q_0=$\overline{Q_0}$)

Clearly label all inputs, outputs, and pins.







Question	Max	Score
1. True/False	10	
2. Venn Diagrams	5	
3. Minimization with K-Maps	12	
4. Fill in the Blanks	8	
5. Circuits	15	
6. Computations with Adders	15	
7. Flip-Flops	15	
8. Multiplexers	15	
9. Alternative Implementation	10	
10. Faulty Circuits	10	
11. Register	15	
TOTAL:	130	