Cpr E 281 HW12
ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

Synchronous Sequential Circuits
Assigned: Week 15
Due Date: Dec. 3, 2018

P1 (27 points): Consider the FSM state-assigned table shown below.

Initial State	w=0		w=1	
	Next	z	Next	z
000 (reset)	001	1	010	0
001	110	0	101	0
010	101	0	100	1
011	001	1	010	0
100	010	0	111	0
101	011	0	000	0
110	111	0	001	1
111	000	0	000	0

A: Show that the inputs to the JKFFs that will be used to implement this FSM will have the following expressions:

$$J_2 = S_1 \oplus S_0, K_2 = S_0 + wS_1 + \bar{w}\bar{S_1}$$

$$J_1 = (\bar{w} + \bar{S_0})(w + S_2 + S_0), K_1 = (w + \bar{S_2} + S_0)(\bar{w} + S_2 + S_0)$$

$$J_0 = (\bar{w} + S_2)(w + \bar{S_2} + S_1), K_0 = (w + \bar{S_2} + S_1)(\bar{w} + S_2 + S_1)(w + S_2 + \bar{S_1})$$

B: Use state minimization to draw a state diagram for an equivalent FSM that uses only four states.

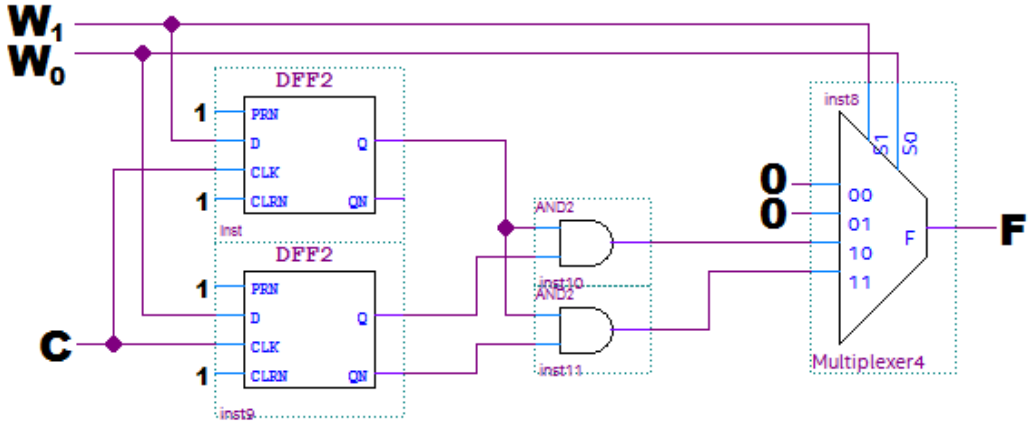
C: With the new state diagram having only four states, assign the values to the states as follows:

The circuit must reset to state 00. While p is held as 1 from the reset state 00, the circuit must enter the next three states in this order: 10, 11, and 01.

Draw a state-assigned table for this new FSM.

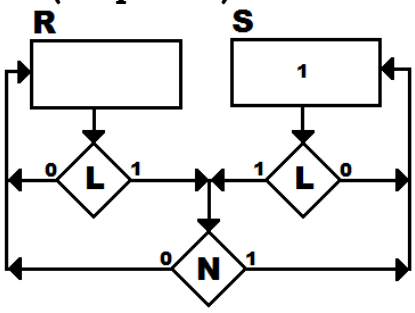
D: Implement this new FSM as a circuit using only two JKFFs and three 4-1 MUXes.

P2 (25 points): The circuit shown below has two bit input W and one bit output F.



A: Draw the state diagram for the FSM. Your state diagram should have four states.
B: Draw the ASM chart for the state diagram you created in part A.
C: Draw an equivalent state diagram for the FSM that has only three states (use state minimization to remove one state from the FSM).
D: Draw the ASM chart for the state diagram that you made in part C.

P3 (18 points): Given the ASM chart shown below, perform the following:



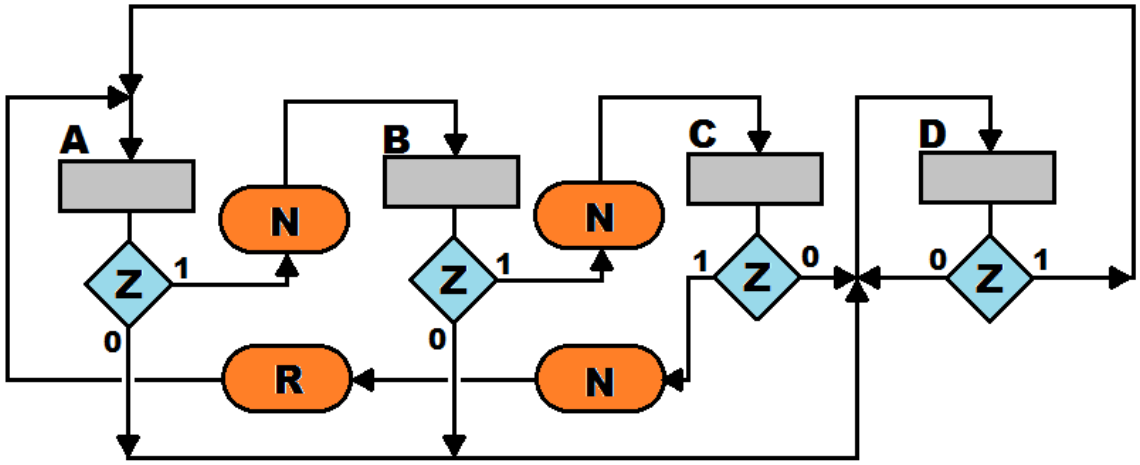
A: Draw the state diagram for this FSM.
B: Draw the circuit which implements this FSM.
C: Next, you will design a circuit that has a 2-bit input L $\{L_1\ L_0\}$ and a 3-bit input N $\{N_3\ N_2\ N_1\}$ where the output Q is as follows.
$Q=N_3$ if L=3, $Q=N_2$ if L=2, and $Q=N_1$ if L=1. If L=0, then Q is unchanged. Draw a circuit that implements this behavior.
D: This circuit has five inputs but only two states. Draw the ASM chart for this circuit.

P4 (10 points): Given the following table for a Mealy FSM with three states, a one-bit input W, and a two-bit output Z:

Time	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
W	0	0	1	1	1	1	0	1	0	1	0	0	1	1	0	1
Z_1	1	1	1	0	0	1	1	0	1	0	1	1	1	0	1	0
Z_0	1	1	0	0	1	0	1	0	1	1	1	1	0	0	1	1

In this table, on each column of time, the input is changed before the output Z is observed. For instance, at time 1, the output Z is observed as 11 only after the input W is set to 0. At time 2, one clock cycle after time 1, the output Z is observed as 10 only after the input W is set to 1.
A: Draw the state diagram for this FSM with three states. Label the states S0, S1, and S2, in the order in which they first appear in the above table.
B: Assign the states as follows: S0 = 001, S1 = 010, S2 = 100. Show the next state variable expressions and the output expressions.

P5 (20 points): This problem concerns the algorithmic state machine (ASM) chart shown below:



A: What are the inputs to this state machine?
B: What are the outputs to this state machine?
C: Draw the state diagram that represents this state machine.
D: Make state assignments as follows: A=00, B=01, C=10, and D=11. Derive output expressions for this ASM chart using DFFs, AND gates, OR gates, and NOT gates.
E: Show that the next state expressions can be written as:

$$S_1^{new} = (\bar{Z} + S_0)\overline{(ZS_1)}, S_0^{new} = (\bar{Z} + \bar{S_0})\overline{(ZS_1)}$$