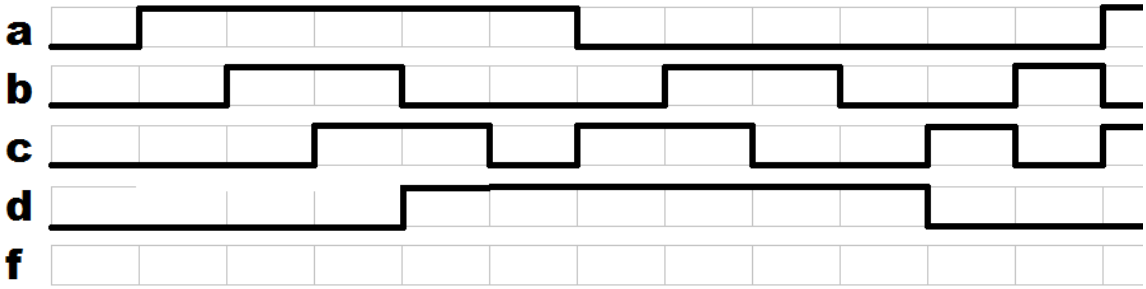
Cpr E 281 HW08
ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

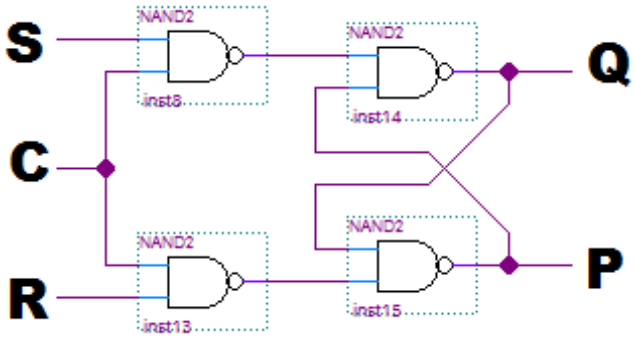
Latches and Flip-Flops
Assigned: Week 9
Due Date: Oct. 22, 2018

P1 (10 points): Given the function $f(a,b,c,d) = \sum m(3,4,5,10,14) + D(6,7)$:
A: Fill in the timing diagram for f.

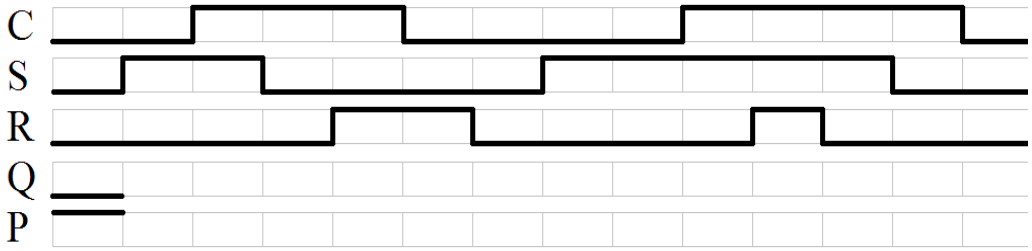


B: Implement f using only 2-1 MUXes. Your circuit should not include more than four 2-1 MUXes. The output f should be produced directly from the output of a 2-1 MUX with d as the select line.
C: Implement f using only two 4-1 MUXes as follows: one of the 4-1 MUXes shall use **a** and **d** as the select line, while the other 4-1 MUX shall use **b** and **c** as the select line.

P2 (10 points): Given the circuit below, answer the following questions:

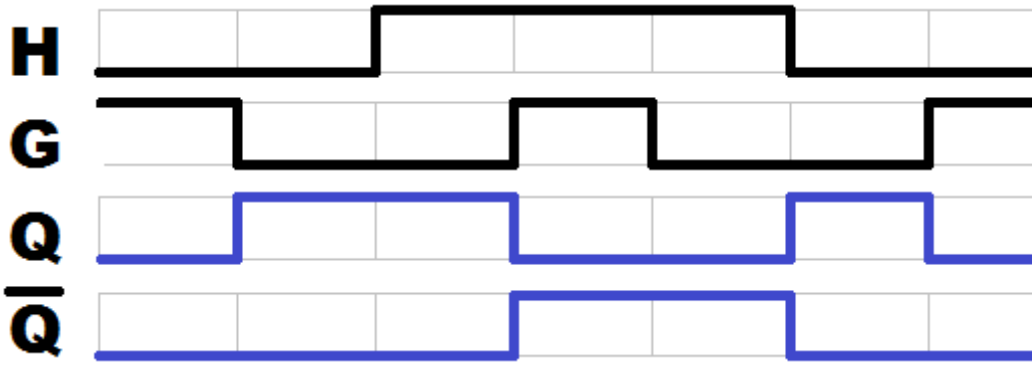


A: What type of circuit is this?
B: Show that this circuit has five combinations for which the output of the circuit is in a memory state.
C: Fill in the following timing diagram.



D: What input combination of C, S, and R leads to an undesirable output?

P3 (12 points): Answer the following questions based on the timing diagram shown below for an HG-NOR Latch.

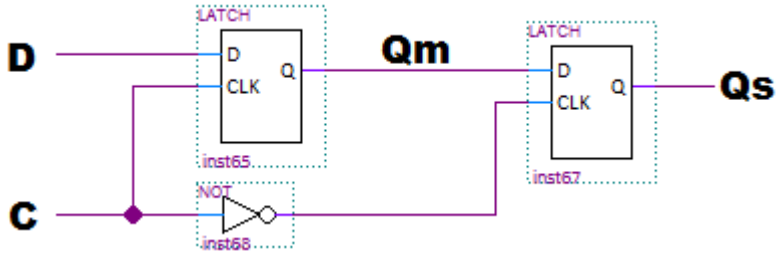


A: What combination of inputs H and G leads to an undesirable output?
B: The inputs H and G are used to drive the inputs to an SR Latch using NOR gates. Fill in the columns of the following table for Q, $\overline{Q}$, S, and R.

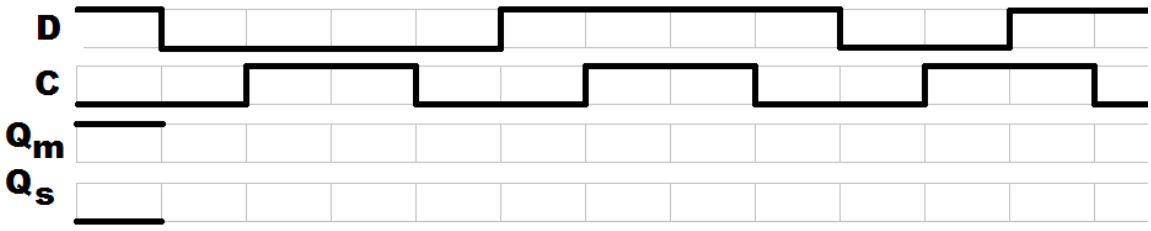
H	G	Q	$\overline{Q}$		S	R
0	0					
0	1					
1	0					
1	1					

C: Write the expression for S and R in terms of H and G.
D: Draw the circuit for the HG NOR Latch

P4 (6 points): Answer the following questions based on the circuit shown below.



A: The latch that appears (twice) in the above circuit is a D Latch. Show the characteristic table for a D Latch.
B: Fill in the timing diagram for the values shown above.

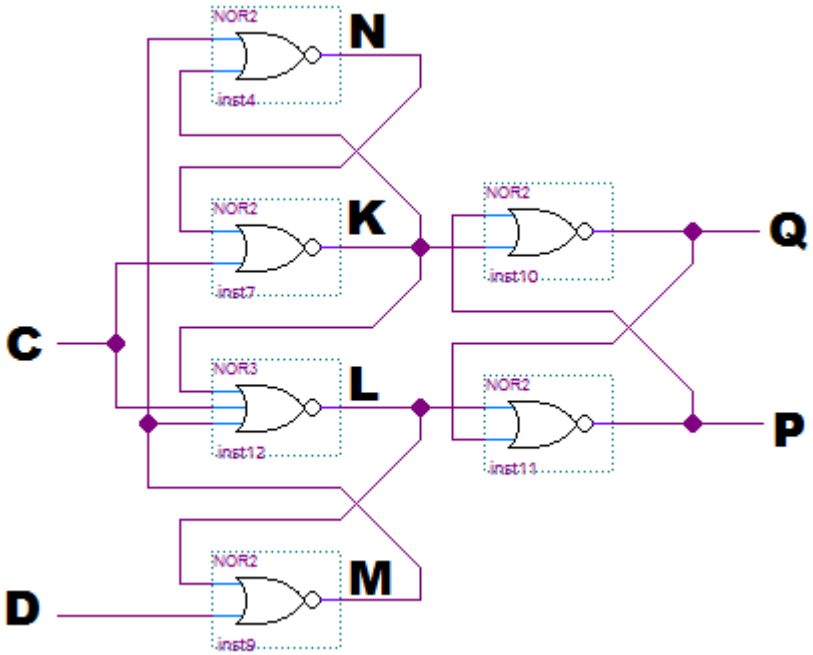


P5 (10 points): Show how a D Flip-Flop (DFF) can be made using a T Flip-Flop (TFF). Your circuit must contain all of the functionality of a DFF (PRESET and CLEAR implementations are not necessary), but must use only one TFF and one 2-1 MUX.

P6 (16 points): Answer the following questions about the Negative-Edge-Triggered Master-Slave DFF with PRESET_N and CLEAR_N connections, as shown in Figure 5.12 from the book. Suppose that D=1 and CLK=0. Answer the following questions about Q.
A: Ignoring PRESET_N and CLEAR_N (assume that they are not connected), what effect does pulsing the clock have on Q in this circuit?
B: What effect does pulsing PRESET_N have on this circuit?
C: What effect does pulsing CLEAR_N have on this circuit?
D: What will be the value of Q if PRESET_N=0 and CLEAR_N=1?
E: What will be the value of Q if PRESET_N=0 and CLEAR_N=0?
F: What will be the value of Q if the clock is pulsed while PRESET_N=0?
G: What will be the value of Q if the clock is pulsed while CLEAR_N=0?
H: What will be the value of Q if the clock is pulsed while CLEAR_N=1 and PRESET_N=1?

P7 (10 points): Show how a DFF can be made using a J-K Flip-Flop (JKFF). You may only use one JKFF and one 2-1 MUX.

P8 (12 points): Given the circuit below, fill out the following table. Use the filled-in values to determine the unknown values from left to right in chronological order. If a value is unknown for the current time, use its value in the previous time step. For instance, if L requires you to know M, but M has not been determined at time t=1, then use the value of M at time t=0

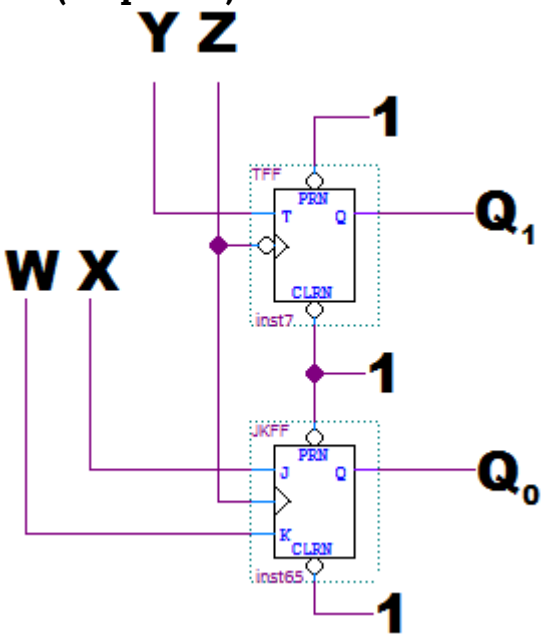


Time	D	C	K	L	M	N	Q	P
t=0	0	0	1		1		1	
t=1	0	1						
t=2	0	0						
t=3	1	0	***1***	***0***	***0***	***0***	***0***	***1***

A: At the end of this table, the value of Q is 0, but D is 1. Describe what must happen to C after time t=3 in order for Q=1, assuming D remains constant.

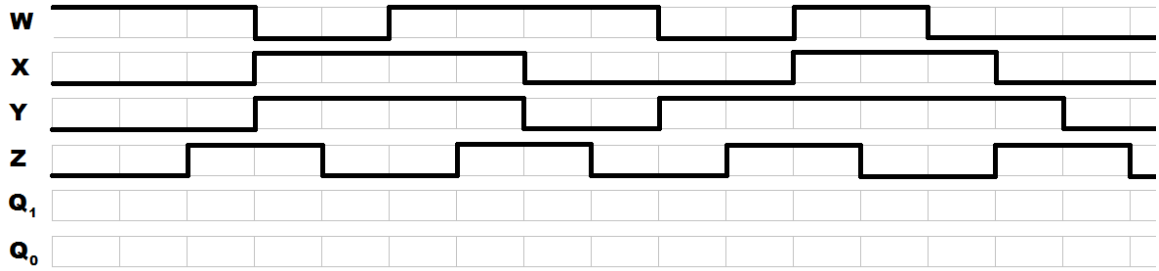
B: What type of circuit is the above circuit?

P9 (14 points): Look at the circuit shown below.



In this circuit, the input Z is connected as the clock to both of the flip-flops shown. The inputs **X and W** go into the JKFF as **J and K**, respectively. The preset and clear connections are both connected to high voltage VCC. The initial value of Q_1=0 and the initial value of Q_0=1.

A: Fill in the following timing diagram. The setup and hold times for both of the flip-flops are equivalent to half the length of a block in the timing diagram.



B: Which input(s) cause a violation of setup time to its flip-flop?

C: In general, what are the implications of a setup time violation?