Cpr E 281 HW07

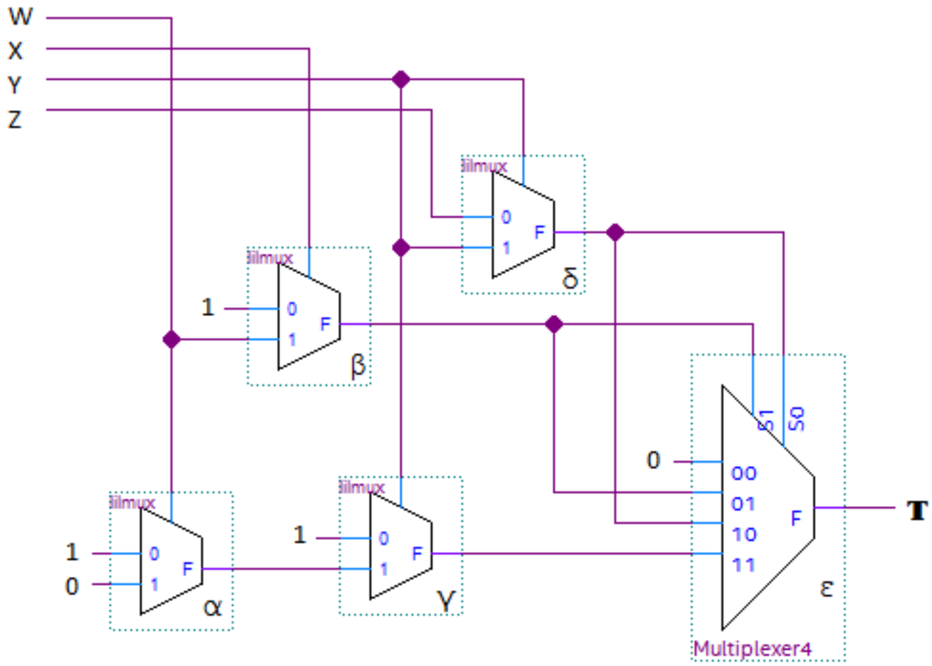
ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

# Combinational Circuit Building Blocks

## Assigned: Week 8

## Due Date: Oct. 15, 2018

**P1 (10 points):** Using the expression for 2-1 multiplexers and 4-1 multiplexers, show that the expression for T in the following circuit is $T = (W + \overline{X})(Y + Z)(\overline{W} + \overline{Y})$.




**P2 (14 points):** Given expression $L = Y \oplus (WZ) \oplus (\overline{W}X)$, perform the following:
A: Draw the truth table for L.
B: Show that L can be implemented using exactly one 16-1 multiplexer (MUX).
C: Show that L can be implemented using exactly one 8-1 MUX and one NOT gate.
D: Show that L can be implemented using exactly one 2-1 MUX and two XOR gates by using the input W as the MUX select line.

**P3 (12 points):** We want to design a circuit that receives six inputs (two-bit input S, which is $S_1$ and $S_0$, along with four inputs A, B, C, and D) and outputs one bit R such that R=A if S=0, R=B if S=1, R=C if S=2, and R=D if S=3.
I: Design this circuit using only one 4-1 MUX and no other logic gates.
II: Design this circuit using only three 2-1 MUXes.
III: Suppose that C is discovered to be equal to D and we wish to take advantage of this equality. Implement the new circuit for R using only two 2-1 MUXes.

# Combinational Circuit Building Blocks
## Assigned: Week 8
## Due Date: Oct. 15, 2018

**P4 (10 points):** We need a circuit with seven inputs and four outputs that operates in accordance with the following abbreviated truth table:

| $V_1$ | $V_0$ | $N_3$ | $N_2$ | $N_1$ | $N_0$ |
|---|---|---|---|---|---|
| 0 | 0 | A | B | A | A |
| 0 | 1 | B | C | B | A |
| 1 | 0 | C | D | C | B |
| 1 | 1 | D | E | D | C |

Show how this truth table can be implemented with just three 4-1 MUXes.

**P5 (10 points):** A 6-bit 2-1 MUX has a 1-bit select input S, one 6-bit data input A, one 6-bit data input B, and one 6-bit data output F. Otherwise, it functions like a regular 1-bit 2-1 MUX except that the data lines are 6-bits wide:
A: What is the fewest number of 1-bit 2-1 MUXes that one can use to produce a 6-bit 2-1 MUX?
B: What is the fewest number of 1-bit 2-1 MUXes that one can use to produce a 1-bit 8-1 MUX?
C: What is the fewest number of 1-bit 2-1 MUXes that one can use to produce a 6-bit 8-1 MUX?
D: What is the fewest number of 1-bit 2-1 MUXes that one can use to produce an n-bit m-1 MUX?

**P6 (10 points):** Given a large supply of 1-2 decoders (with enable), show how you can create a 2-4 decoder.

**P7 (14 points):** Using the specified decoder(s), implement the following:
A: One NOT gate using only one 1-2 decoder.
B: One **3**-input AND gate using only two 1-2 decoders.
C: One 2-input OR gate using only four 1-2 decoders.
D: One 2-input NOR gate using only one 2-4 decoder.

**P8 (20 points):** Given $Z(a, b, c) = \sum m(2,3,4,6,7)$, implement function Z using only the following components:
A: One 3-to-8 decoder and one 6-input OR gate.
B: One 3-to-8 decoder and one 16-to-4 encoder.
C: One 4-2 priority encoder.
D: One 3-to-8 decoder and one 8-to-3 binary encoder.