Cpr E 281 HW06
ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

# Representation and Arithmetic
## Assigned: Week 7
## Due Date: Oct. 8, 2018

**P1 (9 points):** Given the number N=$1010011_2$ as a 7-bit binary number expressed in 2's complement, write the following:
A: N as a decimal number.
B: N as a 7-bit binary number in Sign and Magnitude representation.
C: The absolute value of N, expressed as a 7-bit binary number in Sign and Magnitude.
D: N as a 9-bit binary number expressed in 2's complement.
E: 4N as a 9-bit binary number expressed in 2's complement.

**P2 (6 points):** Negate the following 2's complement numbers.

| | |
|---|---|
| A: 0110101 | B: 1111110 |
| C: 1010100 | D: 0010000 |
| E: 1110111 | F: 0000000 |

**P3 (8 points):** Using the minimum number of bits:
A: Write +18 as an unsigned binary number.
B: Write +13 as a 2's complement binary number.
C: Write -9 as a 2's complement binary number.
D: Write -7 as a 1's complement binary number.

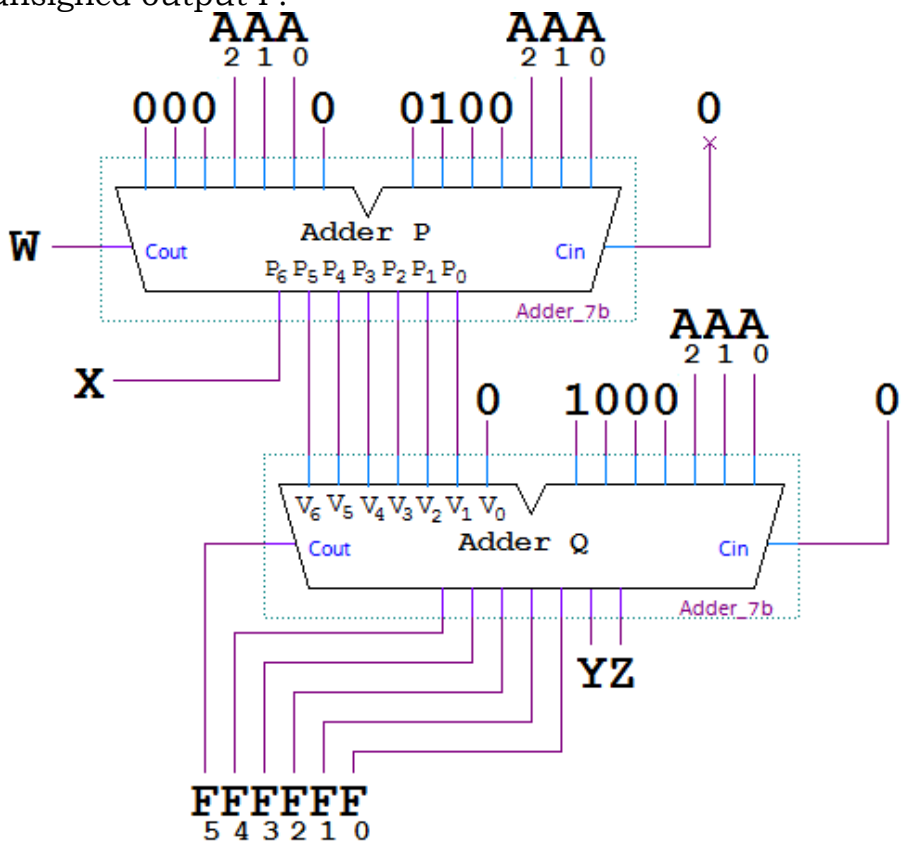
**P4 (18 points):** Perform the requested mathematical operations below, which use 5-bit 2's complement operands and produce a 5-bit 2's complement result. State both the value of carryout and if there is an overflow. For all cases, the carry-in bit is zero.

| | |
|---|---|
| A: 00011 + 00111 | B: 00111 – 00011 |
| C: 01100 + 01001 | D: 01001 + 11011 |
| E: 11100 – 11101 | F: 10111 – 01010 |

**P5 (7 points):** As previously discussed, a Half Adder takes two inputs (X and Y) and produces two outputs ($C_{out}$ and S).
A: Show that the Half Adder is **commutative**; that is, show that swapping the inputs to the Half Adder yields the same output.
B: Write an expression for the outputs of a Half Adder if precisely one of its inputs is fixed at 0.
C: Showing that a Full Adder is commutative would require inspecting six possible permutations. We will simply state for now that the Full Adder is also commutative. Show that a Full Adder with one of its inputs fixed at 0 has the same functionality as a Half Adder.

**P6 (12 points):** Using only one 7-bit full-adder and NOT gates, if necessary, derive a circuit that performs the following operations on unsigned 3-bit number X. Note that the output may be assumed as unsigned, unless it is possible for the operation to produce a negative answer, in which case, the output must be correct in 2's complement:
A: 3X + 1
B: 8X - 21
C: 17X + 3
D: 17 - 2X

**P7 (10 points):** Consider the following circuit, which uses two 7-bit ripple-carry adders "Adder P" and "Adder Q", a 3-bit unsigned input A, and a 6-bit unsigned output F:




A: What is the expression for outputs W and X in this circuit? Why?
B: Describe P, the 7-bit output of "Adder P", algebraically, in terms of A. Note that the output of "Adder P" differs from the left addend of "Adder Q".
C: Describe V, the left 7-bit input to "Adder Q", algebraically in terms of A.
D: Considering that the output bits Y and Z are ignored by F, describe F algebraically in terms of A.
E: Show that the largest possible decimal value for F in this circuit is 44.

**P8 (12 points):** Given a 6-bit multiplication circuit, 2's complement multiplicand M, and 2's complement multiplier Q, answer the following questions:
A: What is the product of $M=001001_2$ and $Q=010010_2$?
B: What is the product of $M=111110_2$ and $Q=001011_2$?
C: What is the product of $M=111011_2$ and $Q=100001_2$?

**P9 (9 points):** Convert the following 32-bit binary numbers from IEEE-754 single-precision floating format into a decimal number.
A: 0100 0011 1000 1100 1000 0000 0000 0000
B: 1011 1110 1100 0100 0000 0000 0000 0000
C: 1111 1111 1000 0000 0000 0000 0000 0000

**P10 (9 points):** Convert the following numbers into IEEE-754 single-precision floating format:
A: 3.234375 = 3 + 15/64
B: -133
C: 0