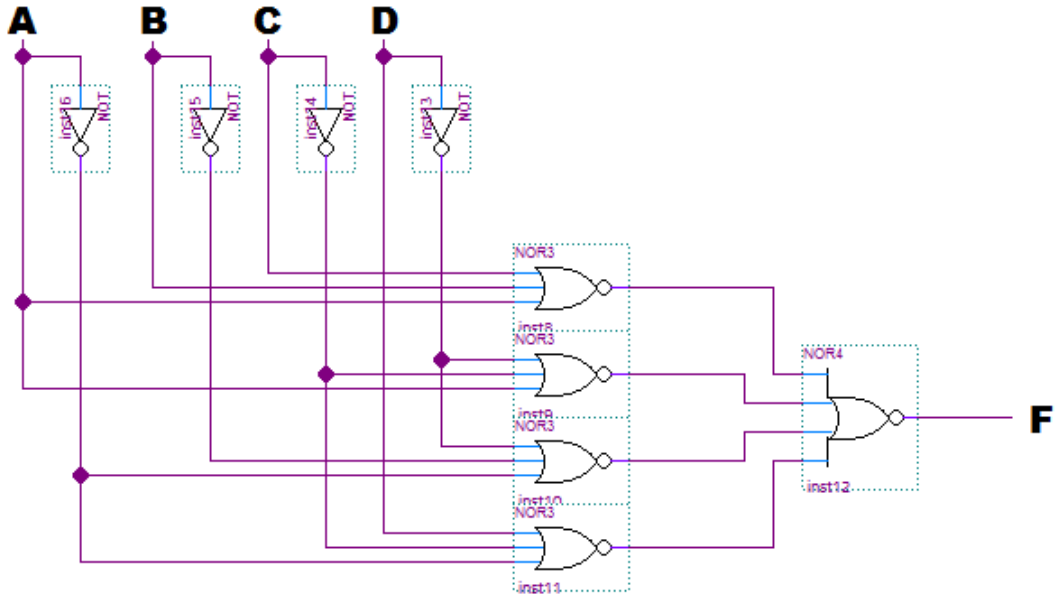
Cpr E 281 HW03
ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

NAND/NOR Gates with Synthesis
Assigned: Week 3
Due Date: Sep. 10, 2018

P1 (5 points): Draw the truth table for the following circuit.



P2 (11 points): Given the expression $F(a,b,c) = \sum m(1,5,6,7)$:
I: Use Boolean Algebra to reduce this expression to a simplified SOP expression (show all steps).
II: Draw the circuit for F using only NAND gates. Your circuit should not use more than four NAND gates to produce F.

P3 (11 points): Given the expression $G(x_2,x_1,x_0) = \prod M(1,2,3,7)$, draw the circuit for G using only NOR gates. Your circuit should not use more than six NOR gates to replicate the output of G.

P4 (12 points): Implement a NOT gate using:
A: One 2-input NAND gate. The two inputs of the NAND gate cannot both be connected to the input signal.
B: One 2-input NOR gate. Again, the two inputs cannot be connected to the same input signal.
C: One 2-input XOR gate.
D: One 3-input XOR gate.
Note: all logic gates can be connected to receive logical values 0 ("GND" or "0") or 1 ("VCC" or "1") as one of their inputs.

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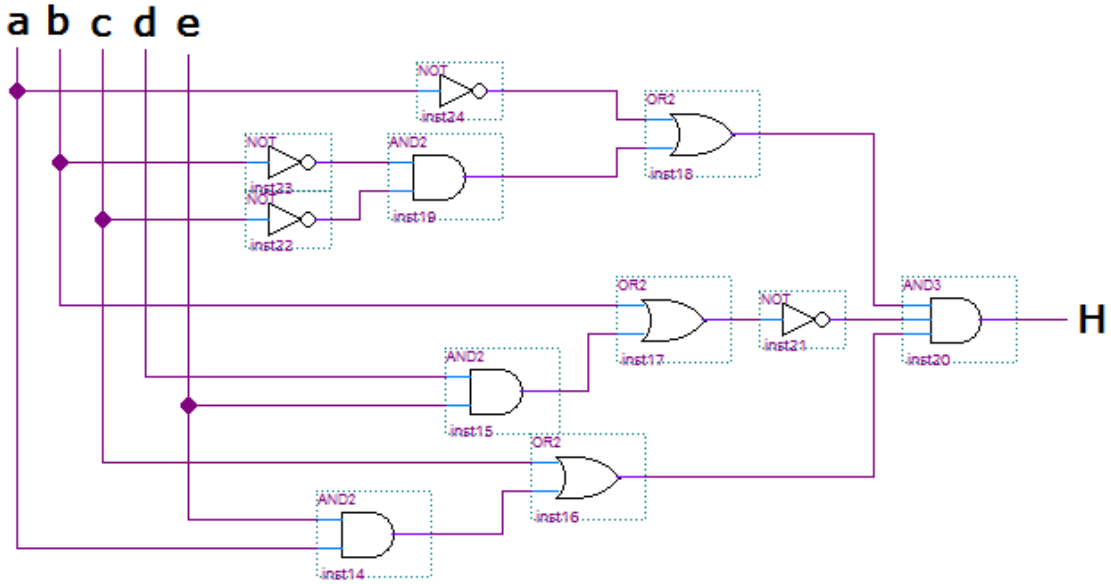
P5 (16 points): We want to convert the circuit shown below into a small number of NAND gates.
A: Write the expression for H, then use Boolean algebra to produce a simplified SOP expression for H.
B: Write the shorthand expression for H.
C: Derive a circuit for H that uses exactly nine NAND gates and no other gates.



P6 (20 points): You have been tasked to produce a circuit that takes three inputs and creates two outputs Y_1 and Y_0. Of the three inputs, one (W) is produced by the output of a button, while the two others (X_1 and X_0) are produced from "sophisticated hardware". You need to provide circuitry that produces output reflected in the truth table shown below.

W	X_1	X_0	Y_1	Y_0
0	0	0	0	1
0	0	1	1	1
0	1	0	0	0
0	1	1	1	0
1	0	0	1	0
1	0	1	0	0
1	1	0	1	1
1	1	1	0	1

A: Derive simplified SOP expressions for both Y_1 and Y_0.
B: Using only NOT, AND, and OR gates, create the circuit for your expressions in A.
C: Implement the circuit in A using only NAND gates.

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P7 (20 points): A **Full Adder** is a circuit that adds three bits (X, Y, and Z) together and returns two bits (C and S) to represent the total as a 2-bit binary number, where C is the most significant bit (MSB) and S is the least significant bit (LSB). For example, let X=1, Y=0, and Z=1. Here, the total should be $2_{10} = 10_2$, and the outputs are, correspondingly, C=1 and S=0.
A: Derive the truth tables for C and S.
B: Write the functions C and S in shorthand notation using minterms.
C: Repeat part B but use maxterms instead.
D: Obtain the simplest SOP expressions for the functions C and S and draw a circuit which implements the **Full Adder**.

P8 (5 points): Convert the following circuit into a circuit that uses only NOR gates. You must use only a minimal number of NOR gates to implement this circuit.