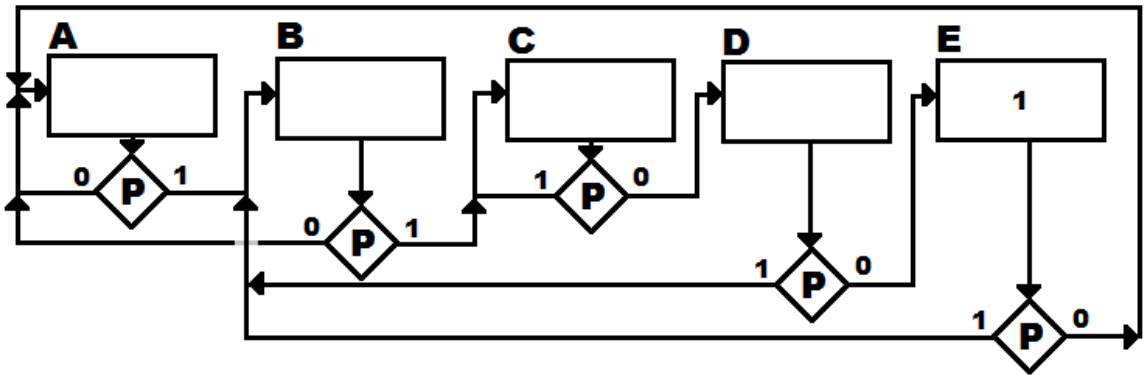
Cpr E 281 EC-HW
ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

Extra Credit Homework
Assigned: Week 15
Due Date: Dec. 5, 2018

Extra Credit Questions (extra 1.5%)

P1 (20 points): Given the ASM chart shown below:



A: Draw the state diagram for this ASM chart.
B: Assign states as follows: A=000, B=001, C=010, D=011, and E=111. Use K-maps to show that the next state expressions are:

$$Y_2^{new} = \bar{P}\bar{Y}_2 Y_1 Y_0$$
$$Y_1^{new} = P\bar{Y}_1 Y_0 + Y_1\bar{Y}_0 + H$$
$$Y_0^{new} = P\bar{Y}_1\bar{Y}_0 + PY_1 Y_0 + H$$
$$H = \bar{P}\bar{Y}_2 Y_1$$

C: Draw the circuit that implements this FSM using only DFFs and NAND gates. Your circuit should not have more than twelve NAND gates.

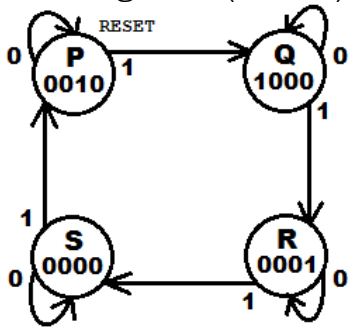
P2 (30 points): The following Moore FSM state table is incomplete. The clock for this FSM (FSM 1) has a period of 100 microseconds such that the button for the input X, controlled by the user, cannot be pressed for only one clock cycle. In addition, button X, when pressed, will output X=0.

Current State	Next State		Output
	X=0	X=1	W
A (reset)	B	A	0
B	B	C	0
C	D	C	0
D	E	--	1
E	F	--	1
F	G	--	1
G	G	A	0

I: Draw a state diagram for this state table.
II: How many full button press cycles (push and release) will cause this FSM to pass through all seven states and return to state A?
III: Use the following state assignments: A=000, B=001, C=010, D=100, E=101, F=110, G=111. Use a K-map to show that the next state expressions for FSM 1 are:
$Y_2^{new} = (\bar{X})(Y_2 + Y_1), Y_1^{new} = (Y_1 + Y_0)(X + Y_2)(\bar{X} + \bar{Y}_2), Y_0^{new} = (\bar{X})(\bar{Y}_2 + Y_1 + \bar{Y}_0)(Y_2 + \bar{Y}_1)$
Assume that DFFs are used to hold the state values.

Current State	Next State		Output
	X=0	X=1	W
A: 000	B: 001	A: 000	0
B: 001	B: 001	C: 010	0
C: 010	D: 100	C: 010	0
D: 100	E: 101	--	1
E: 101	F: 110	--	1
F: 110	G: 111	--	1
G: 111	G: 111	A: 000	0

IV: The output from this FSM (FSM 1) is then used as an input to the following FSM (FSM 2) with input W and 4-bit output L:



Notice that the output of FSM 2 after reset is 2 (0010_2). What will be the output of this FSM 2 after FSM 1 cycles through all seven states and return to state A?

V: How many button presses on X will cycle through all four states of FSM 2 and return to state P?

VI: What sequence of numbers will be observed on the output of FSM 2 as button X is pressed continuously?

VII: Use the following state assignments: P=00, Q=01, R=11, S=10. Show that the next state expressions for FSM 2 are:

P3 (10 points): Input A provides a stream of bits, LSB first, into a Moore FSM. This Moore FSM will output the 2's complement negative of the given number. Reminder of 2's complement: $00110100_2 = 52_{10}$. $-52_{10} = 11001100_2$.

Time	0	1	2	3	4	5	6	7	8
W	0	0	1	0	1	1	0	0	--
N	--	0	0	1	1	0	0	1	1

Draw the state diagram for this FSM. This FSM has a state with **zero indegree** (a state with no transition leading to it), so remember to add the reset so that you can return to this state at the beginning!

P4 (15 points): Design a one-bit parallel-access register using a TFF, an XOR gate, and an AND gate. Hint: Use an FSM approach to design the parallel-access register.